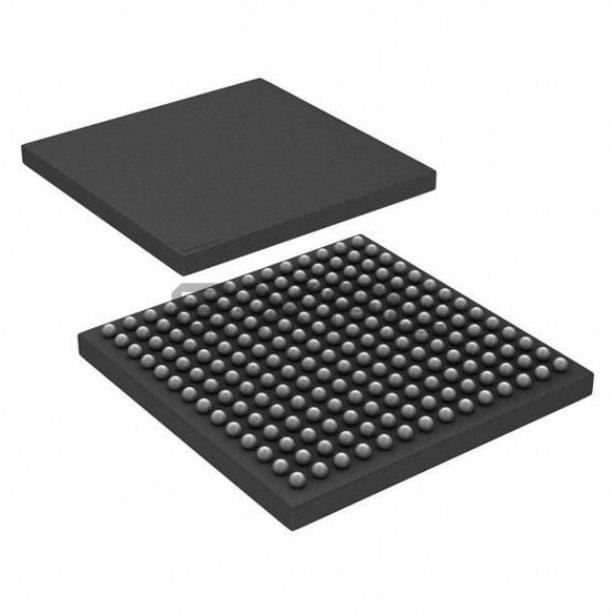

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	600MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	127
Program Memory Size	-
Program Memory Type	External Program Memory
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 20x12b
Oscillator Type	External, Internal
Operating Temperature	0°C ~ 95°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LFBGA
Supplier Device Package	196-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mimxrt1051dvl6a

The i.MX RT1050 is specifically useful for applications such as:

- Industrial Human Machine Interfaces (HMI)
- Motor Control
- Home Appliance

1.1 Features

The i.MX RT1050 processors are based on Arm Cortex-M7 MPCore™ Platform, which has the following features:

- Supports single Arm Cortex-M7 MPCore with:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Full featured Floating Point Unit (FPU) with support of the VFPv5 architecture
  - Support the Armv7-M Thumb instruction set
- Integrated MPU, up to 16 individual protection regions
- Up to 512 KB I-TCM and D-TCM in total
- Frequency of 600 MHz
- Cortex M7 CoreSight™ components integration for debug
- Frequency of the core, as per Table 9, "Operating ranges," on page 19.

The SoC-level memory system consists of the following additional components:

  - Boot ROM (96 KB)
  - On-chip RAM (512 KB)
    - Configurable RAM size up to 512 KB shared with M7 TCM
- External memory interfaces:
  - 8/16-bit SDRAM, up to SDRAM-166
  - 8/16-bit SLC NAND FLASH, with ECC handled in software
  - SD/eMMC
  - SPI NOR FLASH
  - Parallel NOR FLASH with XIP support
  - Single/Dual channel Quad SPI FLASH with XIP support
- Timers and PWMs:
  - Two General Programmable Timers (GPT)
    - 4-channel generic 32-bit resolution timer
    - Each support standard capture and compare operation
  - Four Periodical Interrupt Timer (PIT)
    - Generic 16-bit resolution timer
    - Periodical interrupt generation
  - Four Quad Timers (QTimer)

Table 58. SD/eMMC4.3 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns
uSDHC Input/Card Outp uts SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.9.3.2 eMMC4.4/4.41 (dual data rate) AC timing

Figure 39 depicts the timing of eMMC4.4/4.41. Table 59 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).