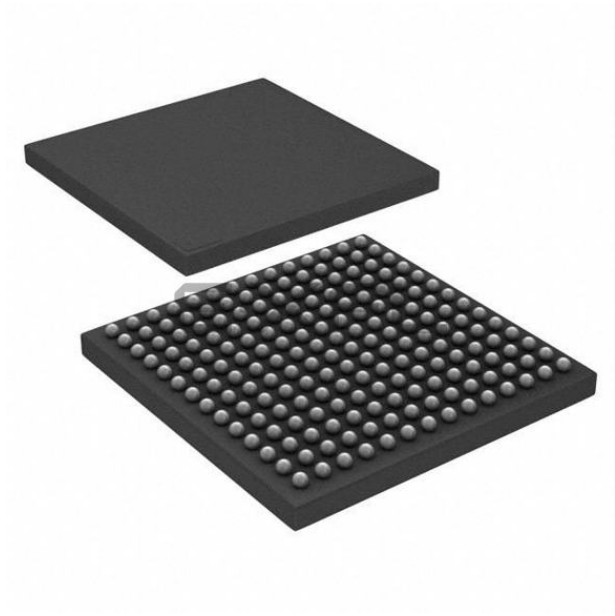

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	600MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	127
Program Memory Size	-
Program Memory Type	External Program Memory
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 20x12b
Oscillator Type	External, Internal
Operating Temperature	0°C ~ 95°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LFBGA
Supplier Device Package	196-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mimxrt1051dvl6b

3 Modules list

The i.MX RT1050 processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX RT1050 modules list

Block Mnemonic	Block Name	Subsystem	Brief Description
ACMP1 ACMP2 ACMP3 ACMP4	Analog Comparator	Analog	The comparator (CMP) provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail-to-rail operation).
ADC1 ADC2	Analog to Digital Converter	Analog	The ADC is a 12-bit general purpose analog to digital converter.
AOI	And-Or-Inverter	Cross Trigger	The AOI provides a universal boolean function generator using a four team sum of products expression with each product term containing true or complement values of the four selected inputs (A, B, C, D).
Arm	Arm Platform	Arm	The Arm Core Platform includes one Cortex-M7 core. It includes associated sub-blocks, such as Nested Vectored Interrupt Controller (NVIC), Floating-Point Unit (FPU), Memory Protection Unit (MPU), and CoreSight debug modules.
BEE	Bus Encryption Engine	Security	On-The-Fly FlexSPI Flash Decryption
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	Parallel CSI	Multimedia Peripherals	The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit Bayer data input.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX RT1050 platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-M7 Core Platform.

Table 2. i.MX RT1050 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LCDIF	LCD interface	Multimedia Peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capabilities. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
LPI2C1 LPI2C2 LPI2C3 LPI2C4	Low Power Inter-integrated Circuit	Connectivity and Communications	The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master. The I2C provides a method of communication between a number of external devices. More detailed information, see Section 4.9.2, “LPI2C module timing parameters.
LPSPI1 LPSPI2 LPSPI3 LPSPI4	Low Power Serial Peripheral Interface	Connectivity and Communications	The LPSPI is a low power Serial Peripheral Interface (SPI) module that support an efficient interface to an SPI bus as a master and/or a slave. • It can continue operating while the chip is in stop modes, if an appropriate clock is available • Designed for low CPU overhead, with DMA off loading of FIFO register access
LPUART1 LPUART2 LPUART3 LPUART4 LPUART5 LPUART6 LPUART7 LPUART8	UART Interface	Connectivity Peripherals	Each of the UART modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 Mbps.
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
PXP	Pixel Processing Pipeline	Multimedia Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications.
QuadTimer1 QuadTimer2 QuadTimer3 QuadTimer4	QuadTimer	Timer Peripherals	The quad-timer provides four time channels with a variety of controls affecting both individual and multi-channel features.Specific features include up/down count, cascading of counters, programmable module, count once/repeated, counter preload, compare registers with preload, shared use of input signals, prescaler controls, independent capture/compare, fault input control, programmable input filters, and multi-channel synchronization.

Table 2. i.MX RT1050 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
Temp Monitor	Temperature Monitor	Analog	The temperature sensor implements a temperature sensor/conversion function based on a temperature-dependent voltage to time conversion.
TSC	Touch Screen	Human Machine Interfaces	With touch controller to support 4-wire and 5-wire resistive touch panel.
USBO2	Universal Serial Bus 2.0	Connectivity Peripherals	USBO2 (USB OTG1 and USB OTG2) contains: • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX RT1050 specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 Two ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)
WDOG1 WDOG2	Watch Dog	Timer Peripherals	The watchdog (WDOG) Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
XBAR	Cross BAR	Cross Trigger	Each crossbar switch is an array of muxes with shared inputs. Each mux output provides one output of the crossbar. The number of inputs and the number of muxes/outputs are user configurable and registers are provided to select which of the shared inputs are routed to each output.

Table 3. Special signal considerations (continued)

Signal Name	Remarks
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the non-connected condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX RT1050 reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be disconnected by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	ONOFF can be configured in debounce, off to on time, and max time-out configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 ms. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max time-out configuration supports 5, 10, 15 seconds and disable. Max time-out configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time.
TEST_MODE	TEST_MODE is for NXP factory use. The user must tie this pin directly to GND.
WAKEUP	A GPIO powered by SNVS domain power supply which can be configured as wakeup source in SNVS mode.

Table 4. JTAG Controller interface summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended connections for unused analog interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 7. Absolute maximum ratings (continued)

IO supply for GPIO in SDIO1 bank (3.3 V mode)	NVCC_SD0	3	3.6	V
IO supply for GPIO in SDIO1 bank (1.8 V mode)		1.65	1.95	V
IO supply for GPIO in SDIO2 bank (3.3 V mode)	NVCC_SD1	3	3.6	V
IO supply for GPIO in SDIO2 bank (1.8 V mode)		1.65	1.95	V
IO supply for GPIO in EMC bank (3.3 V mode)	NVCC_EMC	3	3.6	V
IO supply for GPIO in EMC bank (1.8 V mode)		1.65	1.95	V
ESD damage Immunity: Human Body Model (HBM) Charge Device Model (CDM)	Vesd	 — —	 1000 500	V
Input/Output Voltage range	$V_{in/Vout}$	-0.5	OVDD + 0.3[1]	V
Storage Temperature range	$T_{STORAGE}$	-40	150	°C

1 OVDD is the I/O supply voltage.

4.1.2 10 x 10 MM (VM) thermal resistance

Table 8 displays the 10 x 10 MM (VM) package thermal resistance data.

Table 8. 10 x 10 MM (VM) thermal resistance data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural convection	Single-layer board (1s)	$R_{\theta JA}$	72.1	°C/W	1,2
Junction to Ambient Natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	43.9	°C/W	1,2,3
Junction to Ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	57.5	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	39.0	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	26.1	°C/W	4
Junction to Case	—	$R_{\theta JC}$	19.1	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	0.6	°C/W	6
Junction to Package Bottom	Natural Convection	$R_{\theta JB\_CSB}$	22.3	°C/W	7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

The typical values shown in Table 10 are required for use with NXP SDK to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  - Approximately 25 μA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum supply currents

The data shown in Table 11 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention were to specifically show the worst case power consumption.

See the i.MX RT1050 Power Consumption Measurement Application Note for more details on typical power consumption under various use case definitions.

Table 11. Maximum supply currents

Power Rail	Conditions	Max Current	Unit
DCDC_IN	Max power for FF chip at 95 °C	100	mA
VDD_HIGH_IN	Include internal loading in analog	50	mA
VDD_SNVS_IN	—	250	μA
USB_OTG1_VBUS USB_OTG2_VBUS	25 mA for each active USB interface	50	mA
VDDA_ADC_3P3	3.3 V power supply for 12-bit ADC, 600 μA typical, 750 μA max, for each ADC. 100 Ohm max loading for touch panel, cause 33 mA current.	40	mA
NVCC_GPIO NVCC_SD0 NVCC_SD1 NVCC_EMC	Imax = N x C x V x (0.5 x F) Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F) In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.		

4.1.6 Low power mode supply currents

Table 12 shows the current core consumption (not including I/O) of i.MX RT1050 processors in selected low power modes.

Table 12. Low power mode current and power consumption

Mode	Test Conditions	Supply	Typical[1]	Units
SYSTEM IDLE	• LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • 24 MHz XTAL is ON • 528 PLL is active, other PLLs are power down • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	4.0	mA
		VDD_HIGH_IN (3.3 V)	4.7	
		VDD_SNVS_IN (3.3 V)	0.036	
		Total	27.63	mW
LOW POWER IDLE	• LDO_2P5 and LDO_1P1 are set to Weak mode • WFI, half FlexRAM power down in power gate mode • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	2.2	mA
		VDD_HIGH_IN (3.3 V)	0.3	
		VDD_SNVS_IN (3.3 V)	0.042	
		Total	7.73	mW
SUSPEND (DSM)	• LDO_2P5 and LDO_1P1 are shut off • CPU in Power Gate mode • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC is off • All clocks are shut off, except 32 kHz RTC • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	0.2[2]	mA
		VDD_HIGH_IN (3.3 V)	0.037	
		VDD_SNVS_IN (3.3 V)	0.02	
		Total	0.788	mW
SNVS (RTC)	• All SOC digital logic, analog module are shut off • 32 kHz RTC is alive	DCDC_IN (0 V)	0	mA
		VDD_HIGH_IN (0 V)	0	
		VDD_SNVS_IN (3.3 V)	0.02	
		Total	0.066	mW

1 Typical process material in fab

2 Average current

4.1.7 USB PHY current consumption

4.1.7.1 Power down mode

In power down mode, everything is powered down, including the USB VBUS valid detectors in typical condition. Table 13 shows the USB interface current consumption in power down mode.

Table 13. USB PHY current consumption in power down mode

	VDD_USB_CAP (3.0 V)	VDD_HIGH_CAP (2.5 V)	NVCC_PLL (1.1 V)
Current	5.1 μA	1.7 μA	< 0.5 μA

4.2.1.2 Power-down sequence

The following restrictions must be followed:

- VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off.

4.2.1.3 Power supplies usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see "Power Rail" columns in pin list tables of Section 6, "Package information and contact assignments."

4.2.2 Integrated LDO voltage regulator parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO operation only.

4.2.2.1 Digital regulators (LDO_SNVS)

There are one digital LDO regulator ("Digital", because of the logic loads that they drive, not because of their construction). The advantages of the regulator is to reduce the input supply variation because of its input supply ripple rejection and its on-die trimming. This translates into more stable voltage for the on-chip logics.

The regulator has two basic modes:

- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the target voltage.

For additional information, see the *i.MX RT1050 Reference Manual* (IMXRT1050_RM).

4.2.2.2 Regulators for analog modules

4.2.2.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 9 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V

4.3.1.3 LVDS I/O DC parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 22 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 22. LVDS I/O DC characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS	—	1.125	1.2	1.375	V

4.3.2 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)

Figure 4 shows load circuit for output, and Figure 5 show the output transition time waveform.

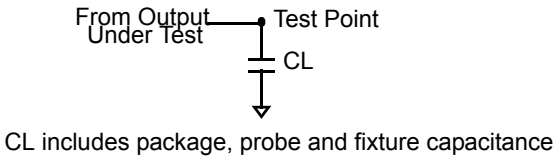


Figure 4. Load circuit for output

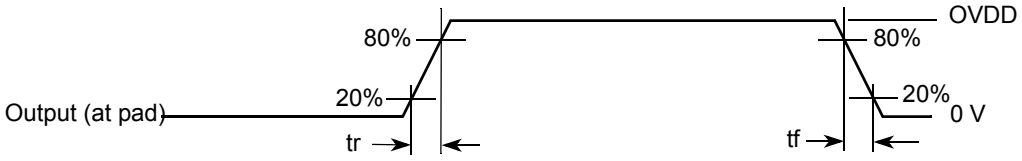


Figure 5. Output transition time waveform

4.3.2.1 General purpose I/O AC parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 23 and Table 24, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

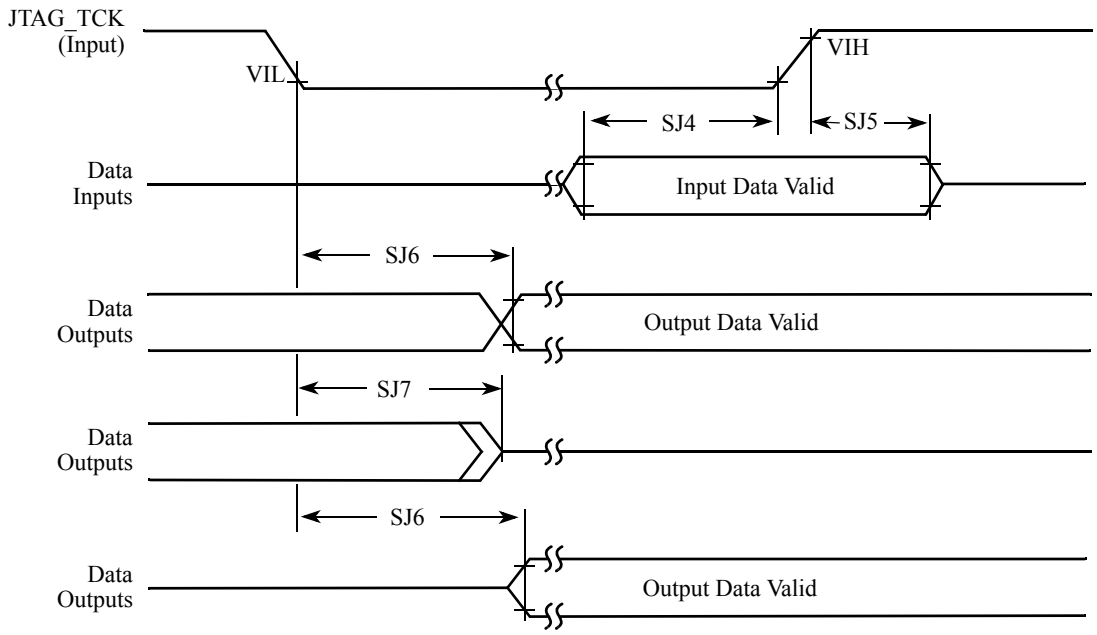


Figure 10. Boundary Scan (JTAG) timing diagram

1 Address output hold time is configurable by SEMC_*CR0.AH. AH field setting value is 0x0 in above table. When AH is set with value N, T_{AHO} min time should be ((N + 1) x T_{CK}). See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for more detail about SEMC_*CR0.AH register field.

2 ADV# low time is configurable by SEMC_*CR0.AS. AS field setting value is 0x0 in above table. When AS is set with value N, T_{ADL} min time should be ((N + 1) x T_{CK} - 1). See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for more detail about SEMC_*CR0.AS register field.

3 Data output hold time is configurable by SEMC_*CR0.WEH. WEH field setting value is 0x0 in above table. When WEH is set with value N, T_{DHO} min time should be ((N + 1) x T_{CK}). See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for more detail about SEMC_*CR0.WEH register field.

4 WE# low time is configurable by SEMC_*CR0.WEL. WEL field setting value is 0x0 in above table. When WEL is set with value N, T_{WEL} min time should be ((N + 1) x T_{CK} - 1). See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for more detail about SEMC_*CR0.WEL register field.

Figure 13 shows the output timing in ASYNC mode.

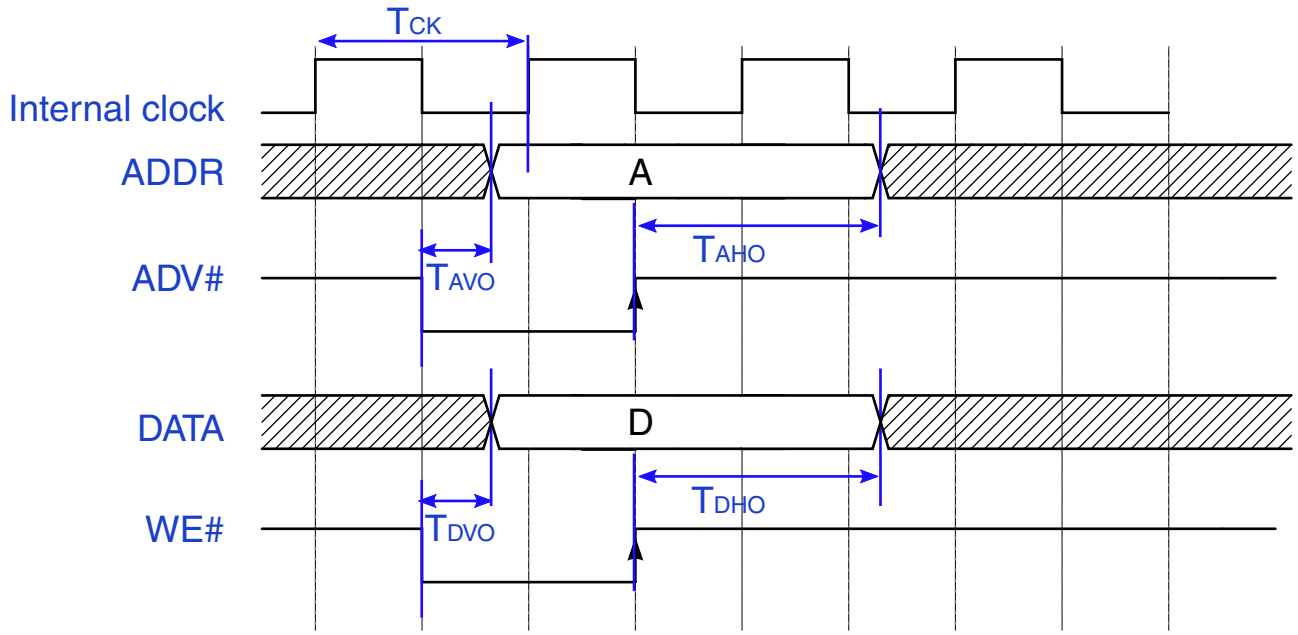


Figure 13. SEMC output timing in ASYNC mode

4.5.1.1.2 SEMC output timing in SYNC mode

Table 31 shows SEMC output timing in SYNC mode.

Table 31. SEMC output timing in SYNC mode

Symbol	Parameter	Min.	Max.	Unit	Comment
	Frequency of operation	—	166	MHz	—
T_{CK}	Internal clock period	6	—	ns	—

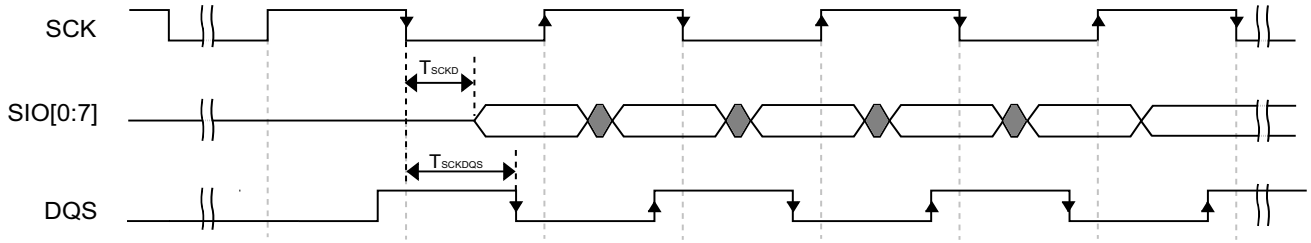


Figure 21. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B1)

Table 42. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B2)

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	166	MHz
T_{SCKD}	Time from SCK to data valid	—	—	ns
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-1	1	ns

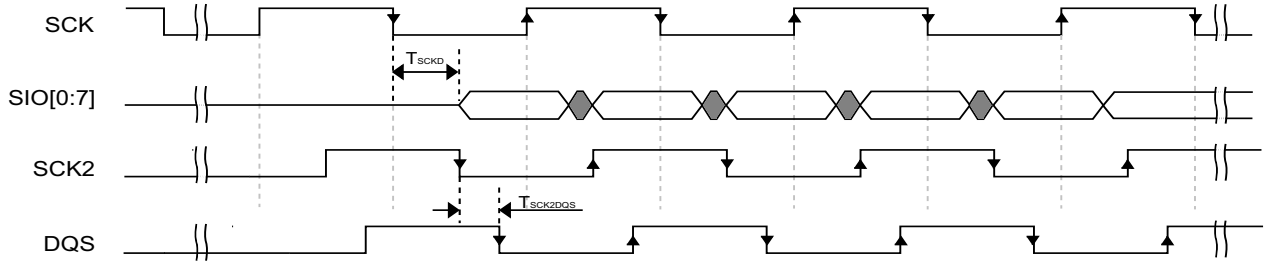


Figure 22. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B2)

4.5.2.2 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

4.5.2.2.1 SDR mode

Table 43. FlexSPI output timing in SDR mode

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	166[1]	MHz
T_{ck}	SCK clock period	6.0	—	ns
T_{DVO}	Output data valid time	—	1	ns
T_{DHO}	Output data hold time	-1	—	ns

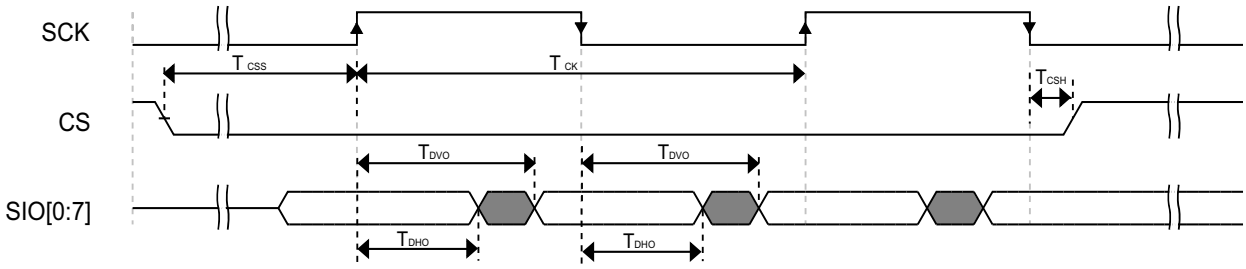


Figure 24. FlexSPI output timing in DDR mode

4.6 Display and graphics

The following sections provide information on display and graphic interfaces.

4.6.1 CMOS Sensor Interface (CSI) timing parameters

The following sections describe the CSI timing in gated and ungated clock modes.

4.6.1.0.1 Gated clock mode timing

Figure 25 and Figure 26 shows the gated clock mode timings for CSI, and Table 45 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on CSI_VSYNC (VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

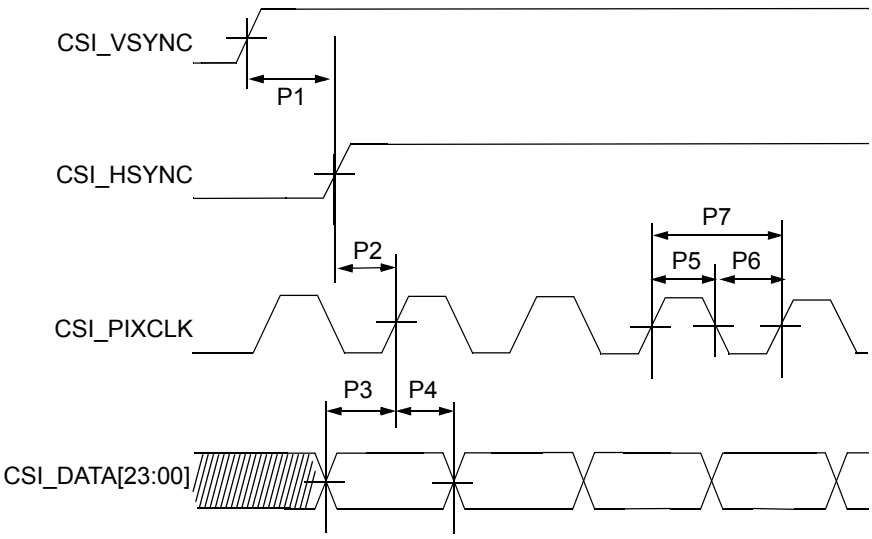


Figure 25. CSI Gated clock mode—sensor data at falling edge, latch data at rising edge

Table 48. Master mode SAI timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	2 x t_{sys}	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	4 x t_{sys}	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	15	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

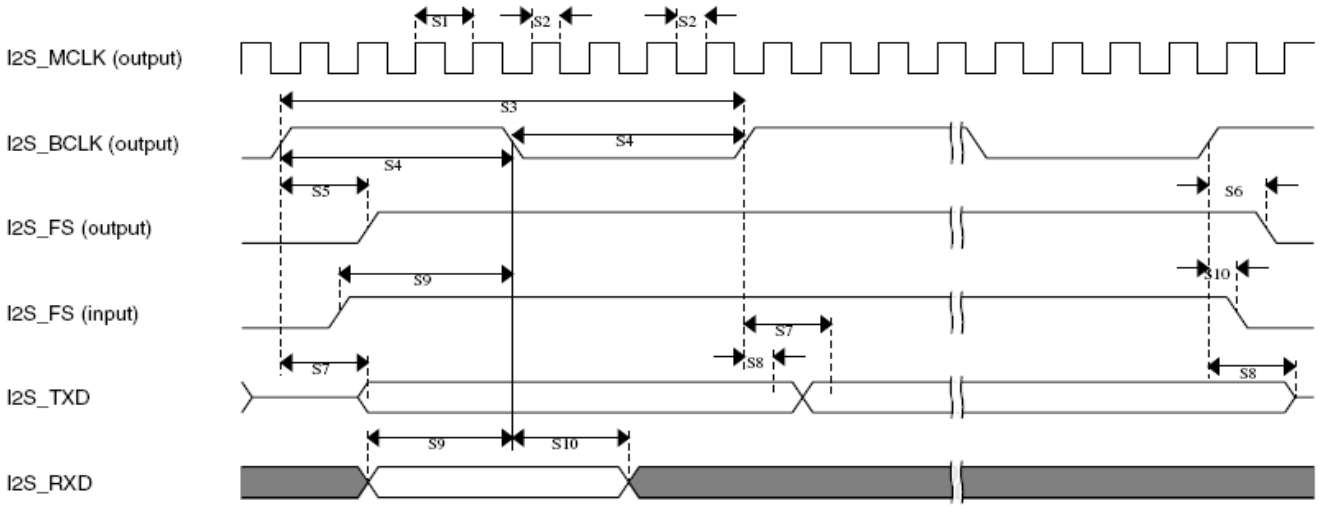


Figure 29. SAI timing—Master modes

Table 49. Slave mode SAI timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	4 x t_{sys}	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns

Table 50. SPDIF timing parameters (continued)

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

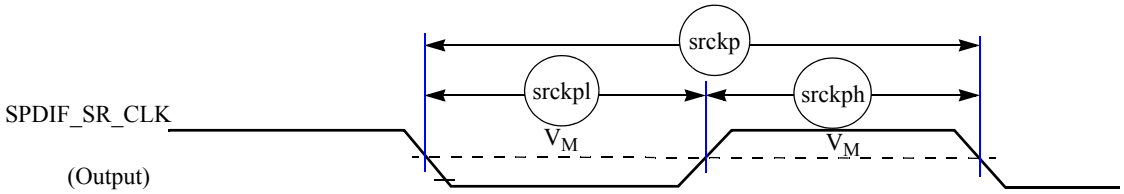


Figure 31. SPDIF_SR_CLK timing diagram

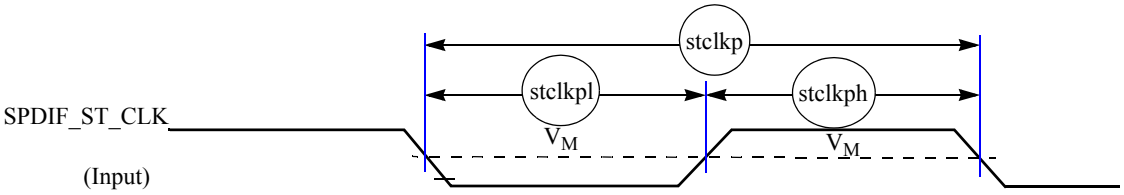


Figure 32. SPDIF_ST_CLK timing diagram

4.8 Analog

The following sections provide information about analog interfaces.

4.8.1 DCDC

Table 51 introduces the DCDC electrical specifications.

Table 51. DCDC electrical specifications

Mode	Buck mode, one output	Notes
Input voltage	2.9 V (A0); 3.3 V (A1)	Min = 2.8 V Max = 3.0 V (A0) and 3.6 V A1)
Output voltage	1.1 V	Configurable 0.8 ~ 1.575 V with 25 mV one step in the Run mode
Max loading	500 mA	—

Table 51. DCDC electrical specifications (continued)

Mode	Buck mode, one output	Notes
Loading in low power modes	200 μA ~ 30 mA	—
Efficiency	90% max	@150 mA
Low power mode	Open loop mode	Ripple is about 15 mV in Run mode
Run mode	• Always continuous mode • Support discontinuous mode	Configurable by register
Inductor	4.7 μH	—
Capacitor	33 μF	—
Over voltage protection	1.55 V	Detect VDDSOC, when the voltage is higher than 1.6 V, shutdown DCDC.
Over Current protection	1 A	Detect the peak current • Run mode: when the current is larger than 1 A, shutdown DCDC.
Low DCDC_IN detection	2.6 V	Detect the DCDC_IN, when battery is lower than 2.6 V, shutdown DCDC.

4.8.2 A/D converter

This section introduces information about A/D converter.

4.8.2.1 12-bit ADC electrical characteristics

The section provide information about 12-bit ADC electrical characteristics.

4.8.2.1.1 12-bit ADC operating conditions

Table 52. 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	3.0	-	3.6	V	—
	Delta to VDD (VDD-VDDA)[2]	ΔV_{DDA}	-100	0	100	mV	—
Ground voltage	Delta to VSS (VSS-VSSAD)	ΔV_{SSAD}	-100	0	100	mV	—
Ref Voltage High	—	V_{DDA}	1.13	V_{DDA}	V_{DDA}	V	—
Ref Voltage Low	—	V_{SS}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	—
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	8/10/12 bit modes	C_{ADIN}	—	1.5	2	pF	—

12-bit ADC characteristics

Table 53. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSAD})

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
Supply Current	ADLPC=1, ADHSC=0	I_{DDA}	—	350	—	μA	ADLSMP=0 ADSTS=10 ADCO=1
	ADLPC=0, ADHSC=0			460			
	ADLPC=0, ADHSC=1			750			
Supply Current	Stop, Reset, Module Off	I_{DDA}	—	1.4	2	μA	—
ADC Asynchronous Clock Source	ADHSC=0	f_{ADACK}	—	10	—	MHz	t_{ADACK} = $1/f_{ADACK}$
	ADHSC=1		—	20	—		
Sample Cycles	ADLSMP=0, ADSTS=00	Csamp	—	2	—	cycles	—
	ADLSMP=0, ADSTS=01			4			
	ADLSMP=0, ADSTS=10			6			
	ADLSMP=0, ADSTS=11			8			
	ADLSMP=1, ADSTS=00			12			
	ADLSMP=1, ADSTS=01			16			
	ADLSMP=1, ADSTS=10			20			
	ADLSMP=1, ADSTS=11			24			

Table 53. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv	—	28	—	cycles	—
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			
Conversion Time	ADLSMP=0 ADSTS=00	Tconv	—	0.7	—	µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
Total Unadjusted Error	12 bit mode	TUE	—	3.4	—	LSB 1 LSB = (V_{REFH} - V_{REFL})/2 N	AVGE = 1, AVGS = 11
	10 bit mode		—	1.5	—		
	8 bit mode		—	1.2	—		
Differential Non-Linearity	12 bit mode	DNL	—	0.76	—	LSB	AVGE = 1, AVGS = 11
	10bit mode		—	0.36	—		
	8 bit mode		—	0.14	—		

Table 76. Boot through SPI-2

PAD Name	IO Function	Mux Mode	Comments
GPIO_SD_B1_07	lpspi2.SCK	ALT 4	—
GPIO_SD_B1_08	lpspi2.SDO	ALT 4	—
GPIO_SD_B1_09	lpspi2.SDI	ALT 4	—
GPIO_SD_B1_06	lpspi2.PCS0	ALT 4	—

Table 77. Boot through SPI-3

PAD Name	IO Function	Mux Mode	Comments
GPIO_AD_B0_00	lpspi3.SCK	ALT 7	—
GPIO_AD_B0_01	lpspi3.SDO	ALT 7	—
GPIO_AD_B0_02	lpspi3.SDI	ALT 7	—
GPIO_SD_B0_03	lpspi3.PCS0	ALT 7	—

Table 78. Boot through SPI-4

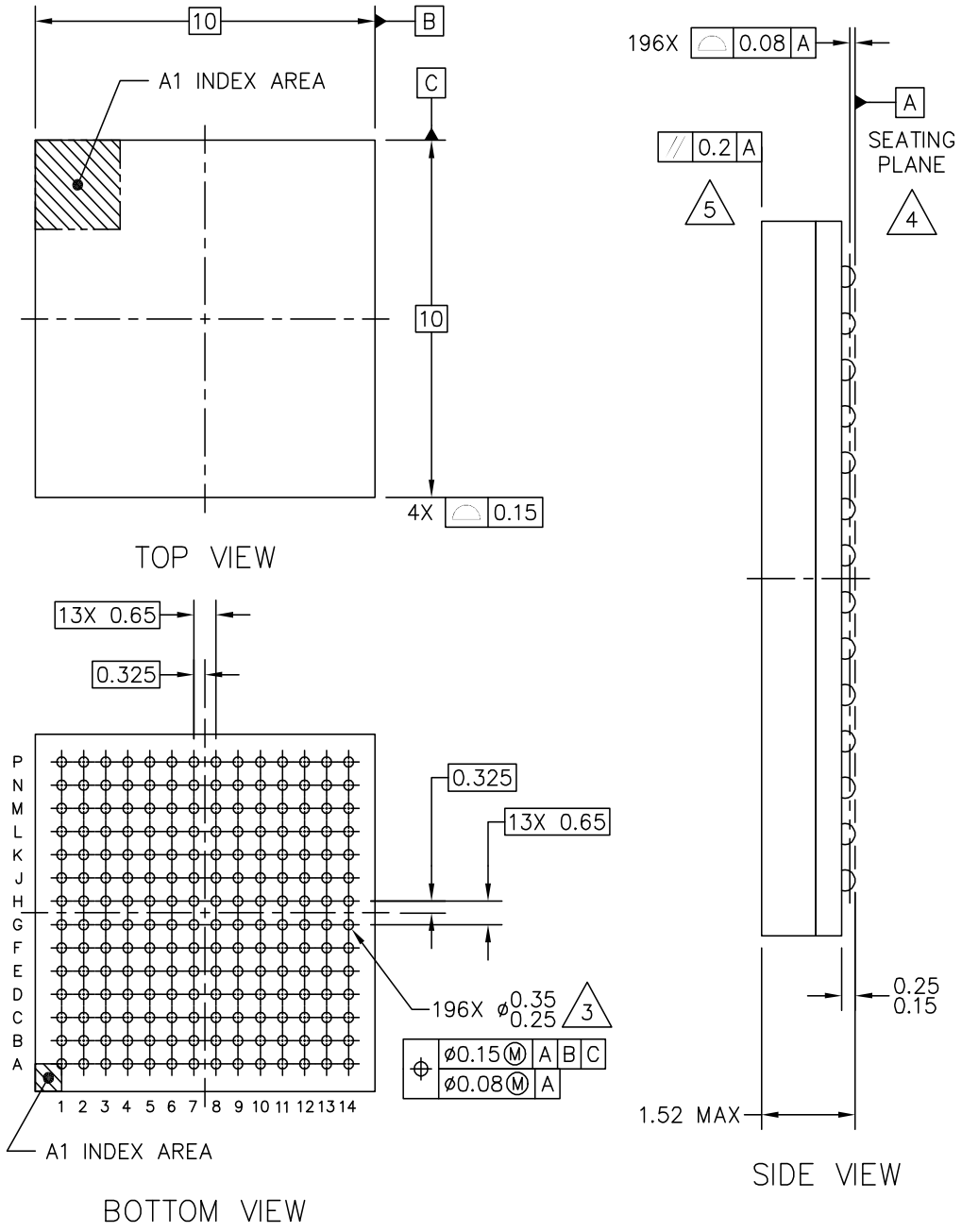
PAD Name	IO Function	Mux Mode	Comments
GPIO_B0_03	lpspi4.SCK	ALT 3	—
GPIO_B0_02	lpspi4.SDO	ALT 3	—
GPIO_B0_01	lpspi4.SDI	ALT 3	—
GPIO_B0_00	lpspi4.PCS0	ALT 3	—

Table 79. Boot through UART1

PAD Name	IO Function	Mux Mode	Comments
GPIO_AD_B0_12	lpuart1.TX	ALT 2	—
GPIO_AD_B0_13	lpuart1.RX	ALT 2	—
GPIO_AD_B0_14	lpuart1.CTS_B	ALT 2	—
GPIO_AD_B0_15	lpuart1.RTS_B	ALT 2	—

Table 80. Boot through UART2

PAD Name	IO Function	Mux Mode	Comments
GPIO_AD_B1_00	lpuart2.CTS_B	ALT 2	—
GPIO_AD_B1_01	lpuart2.RTS_B	ALT 2	—
GPIO_AD_B1_02	lpuart2.TX	ALT 2	—
GPIO_AD_B1_03	lpuart2.RX	ALT 2	—



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	STANDARD: NON-JEDEC	
	SOT1546-1	05 JAN 2016

Figure 48. 10 x 10 mm BGA, case x package top, bottom, and side Views