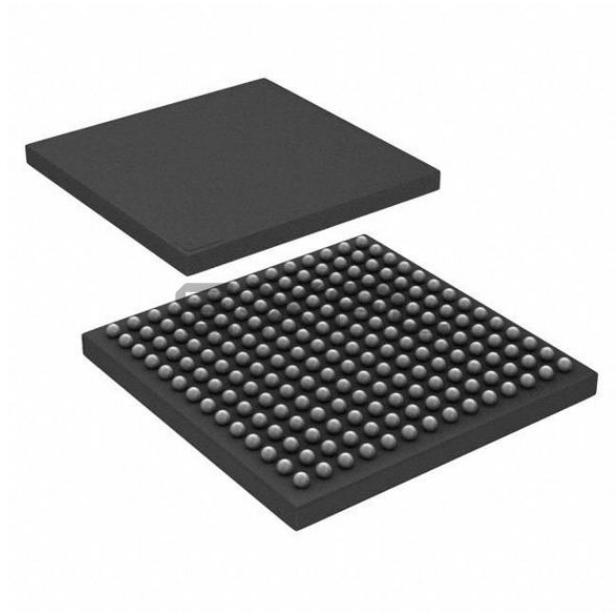

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	600MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	-
Program Memory Type	External Program Memory
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 20x12b
Oscillator Type	External, Internal
Operating Temperature	0°C ~ 95°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LFBGA
Supplier Device Package	196-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mimxrt1052dvl6a

Table 2. i.MX RT1050 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DCDC	DCDC Converter	Analog	The DCDC module is used for generating power supply for core logic. Main features are: • Adjustable high efficiency regulator • Supports 3.0 V input voltage for A0 and 3.3 V input voltage for A1 • Supports nominal run and low power standby modes • Supports at 0.9 ~ 1.3 V output in run mode • Supports at 0.9 ~ 1.0 V output in standby mode • Over current and over voltage detection
eDMA	enhanced Direct Memory Access	System Control Peripherals	There is an enhanced DMA (eDMA) engine and two DMA_MUX. • The eDMA is a 32 channel DMA engine, which is capable of performing complex data transfers with minimal intervention from a host processor. • The DMA_MUX is capable of multiplexing up to 128 DMA request sources to the 32 DMA channels of eDMA.
ENC	Quadrature Encoder/Decoder	Timer Peripherals	The enhanced quadrature encoder/decoder module provides interfacing capability to position/speed sensors. There are five input signals: PHASEA, PHASEB, INDEX, TRIGGER, and HOME. This module is used to decode shaft position, revolution count, and speed.
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
EWM	External Watchdog Monitor	Timer Peripherals	The EWM modules is designed to monitor external circuits, as well as the software flow. This provides a back-up mechanism to the internal WDOG that can reset the system. The EWM differs from the internal WDOG in that it does not reset the system. The EWM, if allowed to time-out, provides an independent trigger pin that when asserted resets or places an external circuit into a safe mode.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.

3.1 Special signal considerations

Table 3 lists special signal considerations for the i.MX RT1050 processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package information and contact assignments." Signal descriptions are provided in the *i.MX RT1050 Reference Manual* (IMXRT1050_RM).

Table 3. Special signal considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N	One general purpose differential high speed clock Input/output (LVDS I/O) is provided. It can be used: • To feed external reference clock to the PLLs and further to the modules inside SoC. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the *i.MX RT1050 Reference Manual* (IMX6ULRM) for details on the respective clock trees. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. After initialization, the CLK1 input/output can be disabled (if not used). If unused either or both of the CLK1_N/P pairs may remain unconnected.
DCDC_PSWITCH	PAD is in DCDC_IN domain and connected the ground to bypass DCDC. To enable DCDC function, assert to DCDC_IN with at least 1ms delay for DCDC_IN rising edge.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO unconnected.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. NXP SDK software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI mounted with 18 pF capacitor. The logic level of this forcing clock cannot exceed NVCC_PLL level. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.
GPANAIO	This signal is reserved for NXP manufacturing use only. This output must remain unconnected.

Table 5. Recommended connections for unused analog interfaces

Module	Pad Name	Recommendations if Unused
CCM	CCM_CLK1_N, CCM_CLK1_P	Not connected
USB	USB_OTG1_CHD_B, USB_OTG1_DN, USB_OTG1_DP, USB_OTG1_VBUS, USB_OTG2_DN, USB_OTG2_DP, USB_OTG2_VBUS	Not connected
ADC	VDDA_ADC_3P3	VDDA_ADC_3P3 must be powered even if the ADC is not used.

4.1.6 Low power mode supply currents

Table 12 shows the current core consumption (not including I/O) of i.MX RT1050 processors in selected low power modes.

Table 12. Low power mode current and power consumption

Mode	Test Conditions	Supply	Typical[1]	Units
SYSTEM IDLE	• LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • 24 MHz XTAL is ON • 528 PLL is active, other PLLs are power down • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	4.0	mA
		VDD_HIGH_IN (3.3 V)	4.7	
		VDD_SNVS_IN (3.3 V)	0.036	
		Total	27.63	mW
LOW POWER IDLE	• LDO_2P5 and LDO_1P1 are set to Weak mode • WFI, half FlexRAM power down in power gate mode • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	2.2	mA
		VDD_HIGH_IN (3.3 V)	0.3	
		VDD_SNVS_IN (3.3 V)	0.042	
		Total	7.73	mW
SUSPEND (DSM)	• LDO_2P5 and LDO_1P1 are shut off • CPU in Power Gate mode • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC is off • All clocks are shut off, except 32 kHz RTC • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	0.2[2]	mA
		VDD_HIGH_IN (3.3 V)	0.037	
		VDD_SNVS_IN (3.3 V)	0.02	
		Total	0.788	mW
SNVS (RTC)	• All SOC digital logic, analog module are shut off • 32 kHz RTC is alive	DCDC_IN (0 V)	0	mA
		VDD_HIGH_IN (0 V)	0	
		VDD_SNVS_IN (3.3 V)	0.02	
		Total	0.066	mW

1 Typical process material in fab

2 Average current

4.1.7 USB PHY current consumption

4.1.7.1 Power down mode

In power down mode, everything is powered down, including the USB VBUS valid detectors in typical condition. Table 13 shows the USB interface current consumption in power down mode.

Table 13. USB PHY current consumption in power down mode

	VDD_USB_CAP (3.0 V)	VDD_HIGH_CAP (2.5 V)	NVCC_PLL (1.1 V)
Current	5.1 μA	1.7 μA	< 0.5 μA

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.2 System power and clocks

This section provide the information about the system power and clocks.

4.2.1 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1.1 Power-up sequence

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- When internal DCDC is enabled, external delay circuit is required to delay the “DCDC_PSWITCH” signal 1 ms after DCDC_IN is stable.
- POR_B should be held low during the entire power up sequence.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG1_VBUS, USB_OTG2_VBUS, and VDDA_ADC_3P3 are not part of the power supply sequence and may be powered at any time.

to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB Phy, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for *i.MX RT1050 Crossover Processors* (IMXRT1050HDG).

For additional information, see the *i.MX RT1050 Reference Manual* (IMXRT1050_RM).

4.2.2.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 9 for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the USB PHY, E-fuse module, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for *i.MX RT1050 Crossover Processors* (IMXRT1050HDG).

For additional information, see the *i.MX RT1050 Reference Manual* (IMXRT1050RM).

4.2.2.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB VUSB voltages (4.4 V–5.5 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either USB VBUS supply, when both are present. If only one of the USB VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX RT1050 Crossover Processors* (IMXRT1050HDG).

For additional information, see the *i.MX RT1050 Reference Manual* (IMXRT1050RM).

4.2.2.2.4 DCDC

DCDC can be configured to operate on power-save mode when the load current is less than 50 mA. During the power-save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

DCDC can detect the peak current in the P-channel switch. When the peak current exceeds the threshold, DCDC will give an alert signal, and the threshold can be configured. By this way, DCDC can roughly detect the current loading.

DCDC also includes the following protection functions:

- Over current protection. In run mode, DCDC shuts down when detecting abnormal large current in the P-type power switch.
- Over voltage protection. DCDC shuts down when detecting the output voltage is too high.
- Low voltage detection. DCDC shuts down when detecting the input voltage is too low.

For additional information, see the *i.MX RT1050 Reference Manual* (IMXRT1050RM).

4.2.3 PLL's electrical characteristics

This section provides PLL electrical characteristics.

4.2.3.1 Audio/Video PLL's electrical parameters

Table 14. Audio/Video PLL's electrical parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.2.3.2 528 MHz PLL

Table 15. 528 MHz PLL's electrical parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.2.3.3 Ethernet PLL

Table 16. Ethernet PLL's electrical parameters

Parameter	Value
Clock output range	1 Ghz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.2.3.4 480 MHz PLL

Table 17. 480 MHz PLL's electrical parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.2.3.5 Arm PLL

Table 18. Arm PLL's electrical parameters

Parameter	Value
Clock output range	648 MHz ~ 1296 MHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.2.4 On-chip oscillators

4.2.4.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implement an oscillator. The oscillator is powered from NVCC_PLL.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.2.4.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implement a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes

4.3.1.3 LVDS I/O DC parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 22 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 22. LVDS I/O DC characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS	—	1.125	1.2	1.375	V

4.3.2 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)

Figure 4 shows load circuit for output, and Figure 5 show the output transition time waveform.

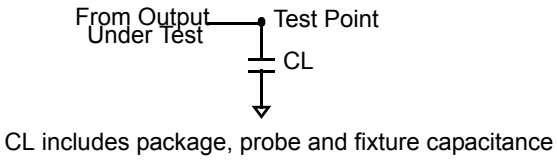


Figure 4. Load circuit for output

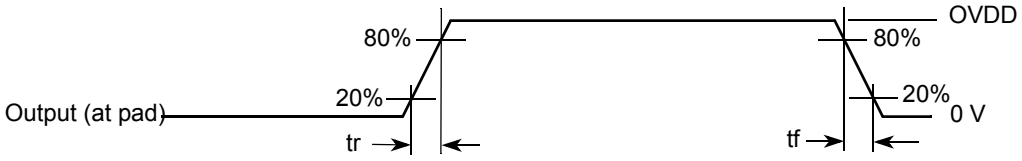


Figure 5. Output transition time waveform

4.3.2.1 General purpose I/O AC parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 23 and Table 24, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

4.4.2 WDOG reset timing parameters

Figure 8 shows the WDOG reset timing and Table 28 lists the timing parameters.

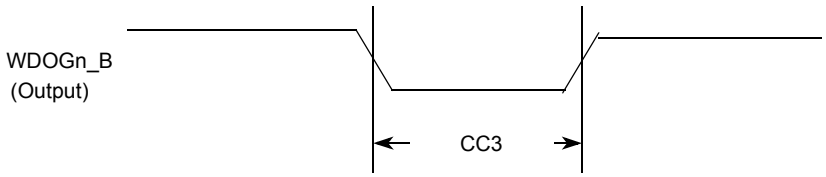


Figure 8. WDOGn_B timing diagram

Table 28. WDOGn_B timing parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOGn_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOGn_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.4.3 SCAN JTAG Controller (SJC) timing parameters

Figure 9 depicts the SJC test clock input timing. Figure 10 depicts the SJC boundary scan timing. Figure 11 depicts the SJC test access port. Signal parameters are listed in Table 29.

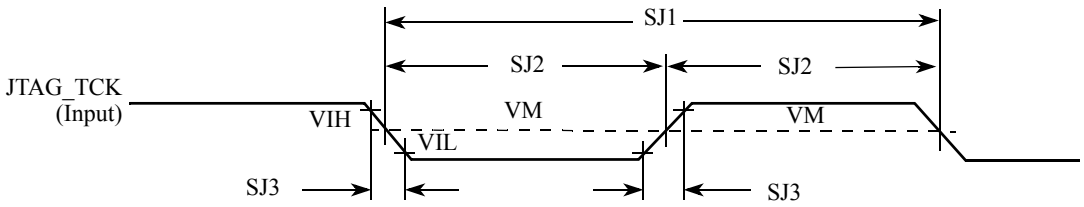


Figure 9. Test clock input timing diagram

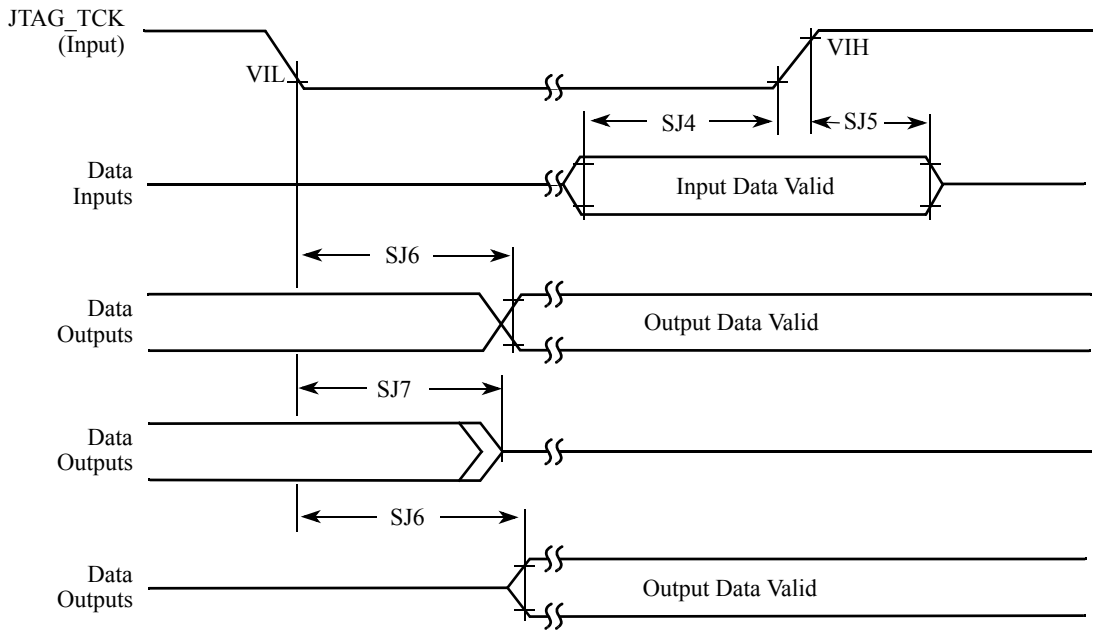


Figure 10. Boundary Scan (JTAG) timing diagram

Table 43. FlexSPI output timing in SDR mode (continued)

Symbol	Parameter	Min	Max	Unit
T_{CSS}	Chip select output setup time	3 x T_{CK} - 1	—	ns
T_{CSH}	Chip select output hold time	3 x T_{CK} + 2	—	ns

1 The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHA*x*CR1 register, the default values are shown above. Please refer to the *i.MX RT1050 Reference Manual (IMXRT1050_RM)* for more details.

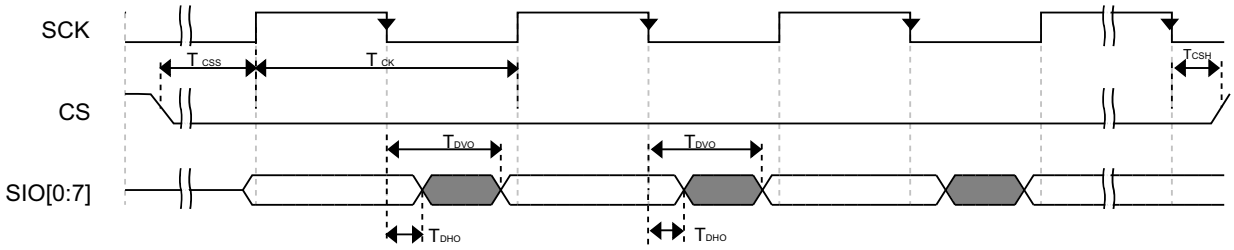


Figure 23. FlexSPI output timing in SDR mode

4.5.2.2.2 DDR mode

Table 44. FlexSPI output timing in DDR mode

Symbol	Parameter	Min	Max	Unit
	Frequency of operation[1]	—	166	MHz
T_{ck}	SCK clock period	6.0	—	ns
T_{DVO}	Output data valid time	—	2.2	ns
T_{DHO}	Output data hold time	0.8	—	ns
T_{CSS}	Chip select output setup time	3 x T_{CK} / 2 - 0.7	—	ns
T_{CSH}	Chip select output hold time	3 x T_{CK} / 2 + 0.8	—	ns

1 The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHA*x*CR1 register, the default values are shown above. Please refer to the *i.MX RT1050 Reference Manual (IMXRT1050_RM)* for more details.

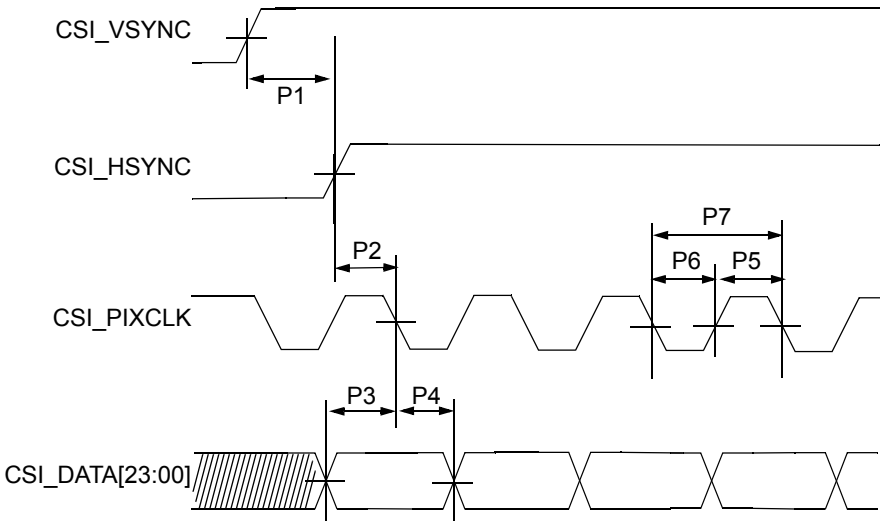
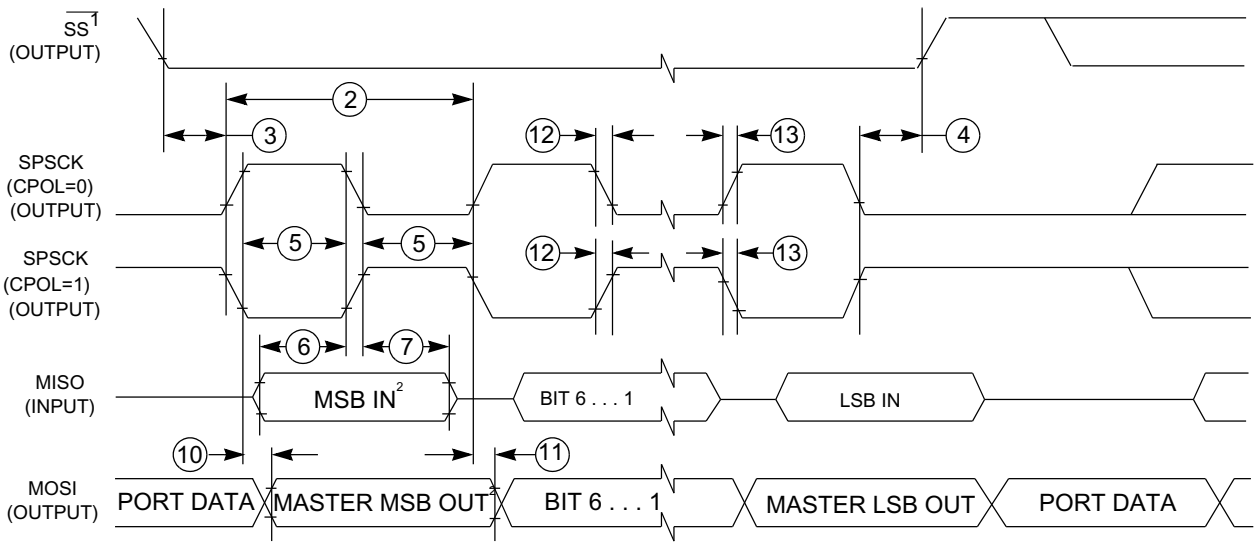


Figure 26. CSI Gated clock mode—sensor data at rising edge, latch data at falling edge

Table 45. CSI gated clock mode timing parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	33.5	—	ns
P2	CSI_HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns
P4	CSI DATA hold time	tDh	1	—	ns
P5	CSI pixel clock high time	tCLKh	3.75	—	ns
P6	CSI pixel clock low time	tCLKl	3.75	—	ns
P7	CSI pixel clock frequency	fCLK	—	80	MHz



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 35. LPSPI Master mode timing (CPHA = 1)

Table 56. LPSPI Slave mode timing

Number	Symbol	Description	Min.	Max.	Units	Note
1	f_{OP}	Frequency of operation	0	f_{periph} / 2	Hz	[1]
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	[2]
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	[3]
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	[4]
10	t_V	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI} t_{FI}	Rise time input Fall time input	—	$t_{periph - 25}$	ns	—
13	t_{RO} t_{FO}	Rise time input Fall time input	—	25	ns	—

1 Absolute maximum frequency of operation (fop) is 30 MHz. The clock driver in the LPSPI module for f_{periph} must be guaranteed this limit is not exceeded.

2 $t_{periph} = 1 / f_{periph}$

3 Time to data active from high-impedance state

4 Hold time to high-impedance state

4.9.3.4 HS200 mode timing

Figure 41 depicts the timing of HS200 mode, and Table 61 lists the HS200 timing characteristics.

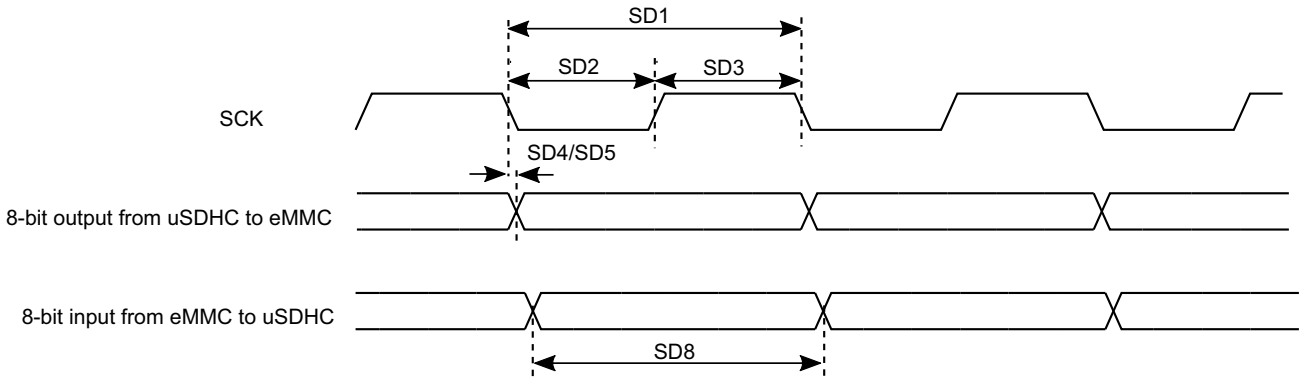


Figure 41. HS200 mode timing

Table 61. HS200 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]HS200 is for 8 bits while SDR104 is for 4 bits.

4.9.3.5 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1 supply are identical to those shown in Table 21, "Single voltage GPIO DC parameters," on page 30.

4.9.4 Ethernet controller (ENET) AC electrical specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.1.2 10 x 10 mm supplies contact assignments and functional contact assignments

Table 81 shows the device connection list for ground, sense, and reference contact signals.

Table 81. 10 x 10 mm supplies contact assignment

Supply Rail Name	Ball(s) Position(s)	Remark
DCDC_IN	L1, L2	—
DCDC_IN_Q	K4	—
DCDC_GND	N1, N2	—
DCDC_LP	M1, M2	—
DCDC_PSWITCH	K3	—
DCDC_SENSE	J5	—
GPANAIO	N10	—
NGND_KEL0	K9	—
NVCC_EMC	E6, F5	—
NVCC_GPIO	E9, F10, J10	—
NVCC_PLL	P10	—
NVCC_SD0	J6	—
NVCC_SD1	K5	—
VDDA_ADC_3P3	N14	—
VDD_HIGH_CAP	P8	—
VDD_HIGH_IN	P12	—
VDD_SNVS_CAP	M10	—
VDD_SNVS_IN	M9	—
VDD_SOC_IN	F6, F7, F8, F9, G6, G9, H6, H9, J9	—
VDD_USB_CAP	K8	—
VSS	A1, A14, B5, B10, E2, E13, G7, G8, H7, H8, J7, J8, K2, K13, L9, N5, N8, P1, P14	—

Table 82 shows an alpha-sorted list of functional contact assignments for the 10 x 10 mm package.

Table 82. 10 x 10 mm functional contact assignments

Ball Name	10 x 10 Ball	Power Group	Ball Type	Default Setting			
				Default Mode	Default Function	Input/ Output	Value
CCM_CLK1_N	P13	—	—	—	CCM_CLK1_N	—	—
CCM_CLK1_P	N13	—	—	—	CCM_CLK1_P	—	—

Table 82. 10 x 10 mm functional contact assignments (continued)

GPIO_AD_B0_00	M14	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[0]	Input	Keeper
GPIO_AD_B0_01	H10	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[1]	Input	Keeper
GPIO_AD_B0_02	M11	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[2]	Input	Keeper
GPIO_AD_B0_03	G11	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[3]	Input	Keeper
GPIO_AD_B0_04	F11	NVCC_GPIO	Digital GPIO	ALT0	SRC.BOOT.MODE[0]	Input	100 K PD
GPIO_AD_B0_05	G14	NVCC_GPIO	Digital GPIO	ALT0	SRC.BOOT.MODE[1]	Input	100 K PD
GPIO_AD_B0_06	E14	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.TMS	Input	47 K PU
GPIO_AD_B0_07	F12	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.TCK	Input	47 K PU
GPIO_AD_B0_08	F13	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.MOD	Input	100 K PU
GPIO_AD_B0_09	F14	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.TDI	Input	47 K PU
GPIO_AD_B0_10	G13	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.TDO	Input	Keeper
GPIO_AD_B0_11	G10	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.TRSTB	Input	47 K PU
GPIO_AD_B0_12	K14	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[12]	Input	Keeper
GPIO_AD_B0_13	L14	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[13]	Input	Keeper
GPIO_AD_B0_14	H14	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[14]	Input	Keeper
GPIO_AD_B0_15	L10	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[15]	Input	Keeper
GPIO_AD_B1_00	J11	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[16]	Input	Keeper
GPIO_AD_B1_01	K11	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[17]	Input	Keeper
GPIO_AD_B1_02	L11	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[18]	Input	Keeper
GPIO_AD_B1_03	M12	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[19]	Input	Keeper
GPIO_AD_B1_04	L12	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[20]	Input	Keeper

Table 82. 10 x 10 mm functional contact assignments (continued)

GPIO_AD_B1_05	K12	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[21]	Input	Keeper
GPIO_AD_B1_06	J12	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[22]	Input	Keeper
GPIO_AD_B1_07	K10	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[23]	Input	Keeper
GPIO_AD_B1_08	H13	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[24]	Input	Keeper
GPIO_AD_B1_09	M13	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[25]	Input	Keeper
GPIO_AD_B1_10	L13	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[26]	Input	Keeper
GPIO_AD_B1_11	J13	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[27]	Input	Keeper
GPIO_AD_B1_12	H12	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[28]	Input	Keeper
GPIO_AD_B1_13	H11	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[29]	Input	Keeper
GPIO_AD_B1_14	G12	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[30]	Input	Keeper
GPIO_AD_B1_15	J14	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[31]	Input	Keeper
GPIO_B0_00	D7	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[0]	Input	Keeper
GPIO_B0_01	E7	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[1]	Input	Keeper
GPIO_B0_02	E8	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[2]	Input	Keeper
GPIO_B0_03	D8	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[3]	Input	Keeper
GPIO_B0_04	C8	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[4]	Input	Keeper
GPIO_B0_05	B8	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[5]	Input	Keeper
GPIO_B0_06	A8	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[6]	Input	Keeper
GPIO_B0_07	A9	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[7]	Input	Keeper
GPIO_B0_08	B9	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[8]	Input	Keeper
GPIO_B0_09	C9	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[9]	Input	Keeper

Table 82. 10 x 10 mm functional contact assignments (continued)

GPIO_EMC_20	A3	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[20]	Input	Keeper
GPIO_EMC_21	C1	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[21]	Input	Keeper
GPIO_EMC_22	F1	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[22]	Input	Keeper
GPIO_EMC_23	G2	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[23]	Input	Keeper
GPIO_EMC_24	D3	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[24]	Input	Keeper
GPIO_EMC_25	D2	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[25]	Input	Keeper
GPIO_EMC_26	B3	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[26]	Input	Keeper
GPIO_EMC_27	A2	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[27]	Input	100 K PD
GPIO_EMC_28	D1	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[28]	Input	Keeper
GPIO_EMC_29	E1	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[29]	Input	Keeper
GPIO_EMC_30	C6	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[30]	Input	Keeper
GPIO_EMC_31	C5	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[31]	Input	Keeper
GPIO_EMC_32	D5	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[18]	Input	Keeper
GPIO_EMC_33	C4	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[19]	Input	Keeper
GPIO_EMC_34	D4	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[20]	Input	Keeper
GPIO_EMC_35	E5	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[21]	Input	Keeper
GPIO_EMC_36	C3	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[22]	Input	Keeper
GPIO_EMC_37	E4	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[23]	Input	Keeper
GPIO_EMC_38	D6	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[24]	Input	Keeper
GPIO_EMC_39	B7	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[25]	Input	Keeper
GPIO_EMC_40	A7	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[26]	Input	Keeper

Table 82. 10 x 10 mm functional contact assignments (continued)

PMIC_STBY_REQ	L7	VDD_SNVS_IN	Digital GPIO	ALT0	CCM.PMIC_VSTBY_REQ	Output	100 K PU (PKE disabled)
POR_B	M7	VDD_SNVS_IN	Digital GPIO	ALT0	SRC.POR_B	Input	100 K PU
RTC_XTALI	N9	—	—	—	—	—	—
RTC_XTALO	P9	—	—	—	—	—	—
TEST_MODE	K6	VDD_SNVS_IN	Digital GPIO	ALT0	TCU.TEST_MODE	Input	100 K PU
USB_OTG1_CHD_B	N12	—	—	—	—	—	—
USB_OTG1_DN	M8	—	—	—	—	—	—
USB_OTG1_DP	L8	—	—	—	—	—	—
USB_OTG1_VBUS	N6	—	—	—	—	—	—
USB_OTG2_DN	N7	—	—	—	—	—	—
USB_OTG2_DP	P7	—	—	—	—	—	—
USB_OTG2_VBUS	P6	—	—	—	—	—	—
XTALI	P11	—	—	—	—	—	—
XTALO	N11	—	—	—	—	—	—
WAKEUP	L6	VDD_SNVS_IN	Digital GPIO	ALT5	GPIO5.IO[0]	Input	100 K PU