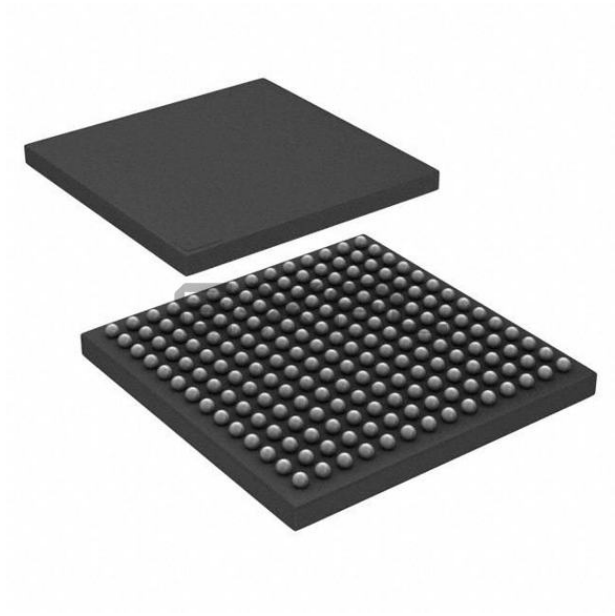

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	600MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	-
Program Memory Type	External Program Memory
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 20x12b
Oscillator Type	External, Internal
Operating Temperature	0°C ~ 95°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LFBGA
Supplier Device Package	196-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mimxrt1052dvl6b

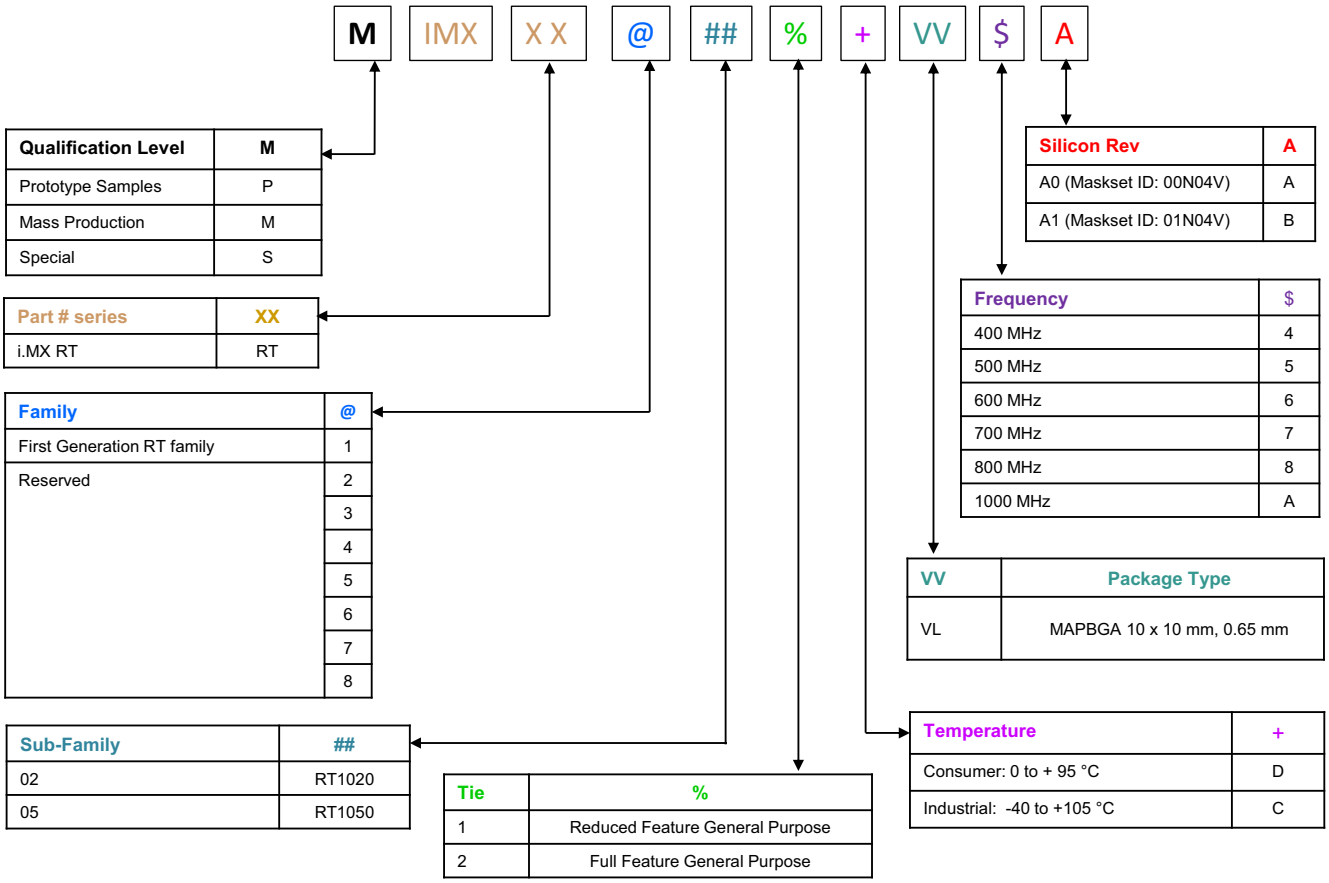


Figure 1. Part number nomenclature—i.MX RT1050

Table 2. i.MX RT1050 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
FlexIO1 FlexIO2	Flexible Input/output	Connectivity and Communications	The FlexIO is capable of supporting a wide range of protocols including, but not limited to: UART, I2C, SPI, I2S, camera interface, display interface, PWM waveform generation, etc. The module can remain functional when the chip is in a low power mode provided the clock it is using remain active.
FlexPWM1 FlexPWM2 FlexPWM3 FlexPWM4	Pulse Width Modulation	Timer Peripherals	The pulse-width modulator (PWM) contains four PWM sub-modules, each of which is set up to control a single half-bridge power stage. Fault channel support is provided. The PWM module can generate various switching patterns, including highly sophisticated waveforms.
FlexRAM	RAM	Memories	The i.MX RT1050 has 512 KB of on-chip RAM which could be flexible allocated to I-TCM, D-TCM, and on-chip RAM (OCRAM) in a 32 KB granularity. The FlexRAM is the manager of the 512 KB on-chip RAM array. Major functions of this blocks are: interfacing to I-TCM and D-TCM of Arm core and OCRAM controller; dynamic RAM arrays allocation for I-TCM, D-TCM, and OCRAM.
FlexSPI	Quad Serial Peripheral Interface	Connectivity and Communications	FlexSPI acts as an interface to one or two external serial flash devices, each with up to four bidirectional data lines.
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT1 GPT2	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
KPP	Keypad Port	Human Machine Interfaces	The KPP is a 16-bit peripheral that can be used as a keypad matrix interface or as general purpose input/output (I/O). It supports 8 x 8 external key pad matrix. Main features are: • Multiple-key detection • Long key-press detection • Standby key-press detection • Supports a 2-point and 3-point contact key matrix

Table 2. i.MX RT1050 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
Temp Monitor	Temperature Monitor	Analog	The temperature sensor implements a temperature sensor/conversion function based on a temperature-dependent voltage to time conversion.
TSC	Touch Screen	Human Machine Interfaces	With touch controller to support 4-wire and 5-wire resistive touch panel.
USBO2	Universal Serial Bus 2.0	Connectivity Peripherals	USBO2 (USB OTG1 and USB OTG2) contains: • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX RT1050 specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 Two ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)
WDOG1 WDOG2	Watch Dog	Timer Peripherals	The watchdog (WDOG) Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
XBAR	Cross BAR	Cross Trigger	Each crossbar switch is an array of muxes with shared inputs. Each mux output provides one output of the crossbar. The number of inputs and the number of muxes/outputs are user configurable and registers are provided to select which of the shared inputs are routed to each output.

Table 5. Recommended connections for unused analog interfaces

Module	Pad Name	Recommendations if Unused
CCM	CCM_CLK1_N, CCM_CLK1_P	Not connected
USB	USB_OTG1_CHD_B, USB_OTG1_DN, USB_OTG1_DP, USB_OTG1_VBUS, USB_OTG2_DN, USB_OTG2_DP, USB_OTG2_VBUS	Not connected
ADC	VDDA_ADC_3P3	VDDA_ADC_3P3 must be powered even if the ADC is not used.

Table 9. Operating ranges (continued)

A/D converter	VDDA_ADC_3P3	—	3.0	3.15	3.6	V	VDDA_ADC_3P3 must be powered even if the ADC is not used. VDDA_ADC_3P3 cannot be powered when the other SoC supplies (except VDD_SNVS_IN) are off.
Temperature Operating Ranges							
Junction temperature	Tj	Standard Commercial	0	—	95	°C	See the application note, i.MX RT1050 Product Lifetime Usage Estimates for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This result in an optimized power/speed ratio.

2 Applying the maximum voltage results in shorten lifetime. 3.6 V usage limited to < 1% of the use profile. Reset of profile limited to below 3.49 V.

3 In setting VDD_SNVS_IN voltage with regards to Charging Currents and RTC, refer to the *i.MX RT1050 Hardware Development Guide* (IMXRT1050HDG).

4.1.4 External clock sources

Each i.MX RT1050 processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 10 shows the interface frequency requirements.

Table 10. External input clock frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for *i.MX RT1050 Crossover Processors* (IMXRT1050HDG).

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

4.2.2.2.4 DCDC

DCDC can be configured to operate on power-save mode when the load current is less than 50 mA. During the power-save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

DCDC can detect the peak current in the P-channel switch. When the peak current exceeds the threshold, DCDC will give an alert signal, and the threshold can be configured. By this way, DCDC can roughly detect the current loading.

DCDC also includes the following protection functions:

- Over current protection. In run mode, DCDC shuts down when detecting abnormal large current in the P-type power switch.
- Over voltage protection. DCDC shuts down when detecting the output voltage is too high.
- Low voltage detection. DCDC shuts down when detecting the input voltage is too low.

For additional information, see the *i.MX RT1050 Reference Manual* (IMXRT1050RM).

4.2.3 PLL's electrical characteristics

This section provides PLL electrical characteristics.

4.2.3.1 Audio/Video PLL's electrical parameters

Table 14. Audio/Video PLL's electrical parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.2.3.2 528 MHz PLL

Table 15. 528 MHz PLL's electrical parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

power from VDD_HIGH_IN when that supply is available and transitions to the backup battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to a crude internal ring oscillator. The frequency range of this block is approximately 10–45 kHz. It highly depends on the process, voltage, and temperature.

The OSC32k runs from VDD_SNVS_CAP supply, which comes from the VDD_HIGH_IN/VDD_SNVS_IN. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDD_HIGH_IN range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell. For example, for Panasonic ML621:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k.

Table 19. OSC32K main characteristics

	Min	Typ	Max	Comments
Fosc	—	32.768 KHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 μA	—	The 4 μA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 μA when ring oscillator is inactive, 20 μA when the ring oscillator is running. Another 1.5 μA is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 μA on vdd_rtc when the ring oscillator is not running.
Bias resistor	—	14 MΩ	—	This integrated bias resistor sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.3 I/O parameters

This section provide parameters on I/O interfaces.

4.3.1 I/O DC parameters

This section includes the DC parameters of the following I/O types:

Table 21. Single voltage GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1]	V_{OH}	Ioh= -0.1mA (ipp_dse=001,010) Ioh= -1mA (ipp_dse=011,100,101,110,111)	NVCC_XXXX-0.15	–	V
Low-level output voltage[1]	VOL	Iol= 0.1mA (ipp_dse=001,010) Iol= 1mA (ipp_dse=011,100,101,110,111)	–	0.15	V
High-Level input voltage[1,2]	VIH	—	0.7*NVCC_XXXX	NVCC_XXXX	V
Low-Level input voltage[1,2]	VIL	—	0	0.3 x NVCC_XXXX	V
Input Hysteresis (NVCC_XXXX= 1.8V)	VHYS_LowVDD	NVCC_XXXX=1.8V	250	—	mV
Input Hysteresis (NVCC_XXXX=3.3V)	VHYS_HighVDD	NVCC_XXXX=3.3V	250	—	mV
Schmitt trigger VT+[2,3]	VTH+	—	0.5 x NVCC_XXXX	—	mV
Schmitt trigger VT-[2,3]	VTH-	—	—	0.5 x NVCC_XXXX	mV
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=0V	—	212	μA
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=NVCC_XXXX	—	1	μA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=0V	—	100	μA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=NVCC_XXXX	—	1	μA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=0V	—	48	μA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=NVCC_XXXX	—	1	μA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=NVCC_XXXX	—	48	μA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=0V	—	1	μA
Input current (no PU/PD)	IIN	VI = 0, VI = NVCC_XXXX	-1	1	μA
Keeper Circuit Resistance	R_Keeper	VI =0.3*NVCC_XXXX, VI = 0.7* NVCC_XXXX	105	175	kΩ

1 Overshoot and undershoot conditions (transitions above NVCC_XXXX and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.3.3.1 Single voltage GPIO output buffer impedance

Table 25 shows the GPIO output buffer impedance (NVCC_XXXX 1.8 V).

Table 25. GPIO output buffer average impedance (NVCC_XXXX 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 88 65 52 43 37	Ω

Table 26 shows the GPIO output buffer impedance (NVCC_XXXX 3.3 V).

Table 26. GPIO output buffer average impedance (NVCC_XXXX 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	157 78 53 39 32 26 23	Ω

4.4 System modules

This section contains the timing and electrical parameters for the modules in the i.MX RT1050 processor.

4.4.1 Reset timings parameters

Figure 7 shows the reset timing and Table 27 lists the timing parameters.

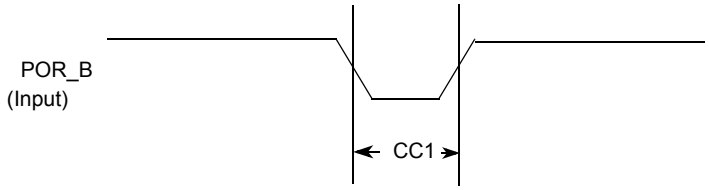


Figure 7. Reset timing diagram

Table 27. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	RTC_XTALI cycle

1 Address output hold time is configurable by SEMC_*CR0.AH. AH field setting value is 0x0 in above table. When AH is set with value N, T_{AHO} min time should be ((N + 1) x T_{CK}). See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for more detail about SEMC_*CR0.AH register field.

2 ADV# low time is configurable by SEMC_*CR0.AS. AS field setting value is 0x0 in above table. When AS is set with value N, T_{ADL} min time should be ((N + 1) x T_{CK} - 1). See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for more detail about SEMC_*CR0.AS register field.

3 Data output hold time is configurable by SEMC_*CR0.WEH. WEH field setting value is 0x0 in above table. When WEH is set with value N, T_{DHO} min time should be ((N + 1) x T_{CK}). See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for more detail about SEMC_*CR0.WEH register field.

4 WE# low time is configurable by SEMC_*CR0.WEL. WEL field setting value is 0x0 in above table. When WEL is set with value N, T_{WEL} min time should be ((N + 1) x T_{CK} - 1). See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for more detail about SEMC_*CR0.WEL register field.

Figure 13 shows the output timing in ASYNC mode.

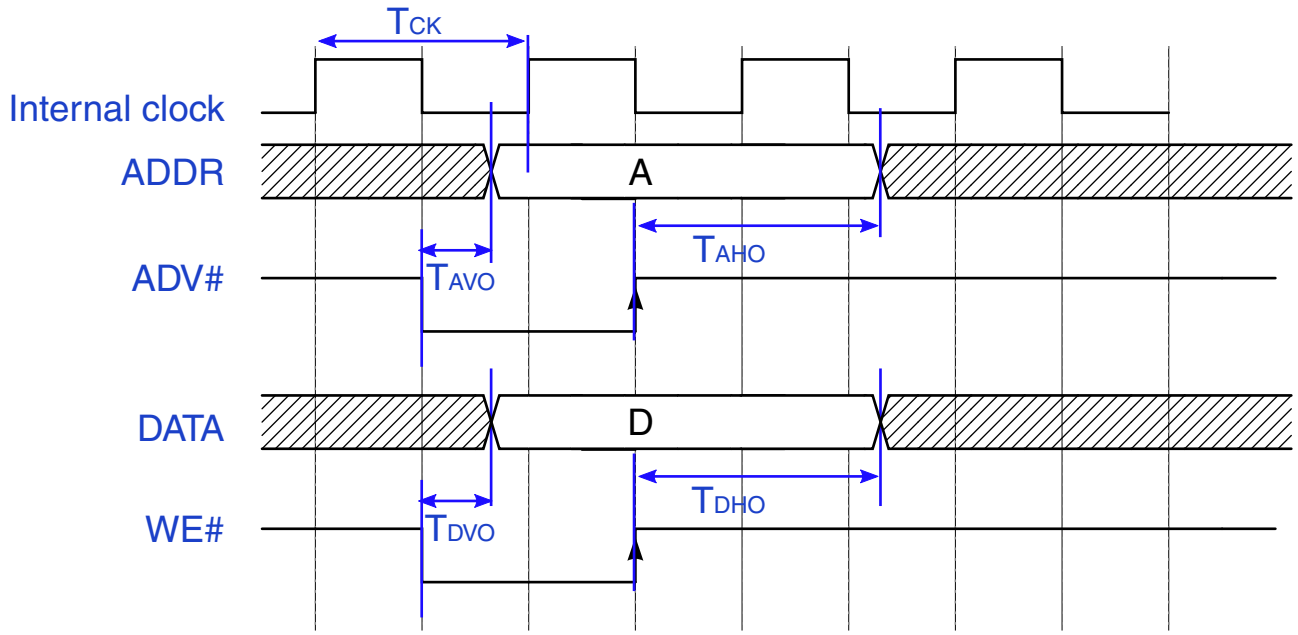


Figure 13. SEMC output timing in ASYNC mode

4.5.1.1.2 SEMC output timing in SYNC mode

Table 31 shows SEMC output timing in SYNC mode.

Table 31. SEMC output timing in SYNC mode

Symbol	Parameter	Min.	Max.	Unit	Comment
	Frequency of operation	—	166	MHz	—
T_{CK}	Internal clock period	6	—	ns	—

Table 54. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_H	Analog comparator hysteresis[1]				mV
	• CR0[HYSTCTR] = 00	—	1	2	
	• CR0[HYSTCTR] = 01	—	21	54	
	• CR0[HYSTCTR] = 10	—	42	108	
	• CR0[HYSTCTR] = 11	—	64	184	
V_{CMPOH}	Output high	V_{DD} - 0.5	—	—	V
V_{CMPOI}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN = 1, PMODE = 1)[2]	—	25	40	ns
t_{DLS}	Propagation delay, low-speed mode (EN = 1, PMODE = 0)[2]	—	50	90	ns
t_{DInit}	Analog comparator initialization delay[3]	—	1.5	—	μs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	5	—	μA
R_{DAC6b}	6-bit DAC reference inputs	—	V_{DD}	—	V
INL_{DAC6b}	6-bit DAC integral non-linearity	-0.3	—	0.3	LSB[4]
DNL_{DAC6b}	6-bit DAC differential non-linearity	-0.15	—	0.15	LSB[4]

1 Typical hysteresis is measured with input voltage range limited to 0.7 to V_{DD} - 0.7 V in high speed mode.

2 Signal swing is 100 mV.

3 Comparator initialization delay is defined as the time between software writes to the enable comparator module and the comparator output setting to a stable level.

4 1 LSB = $V_{reference}$ / 64

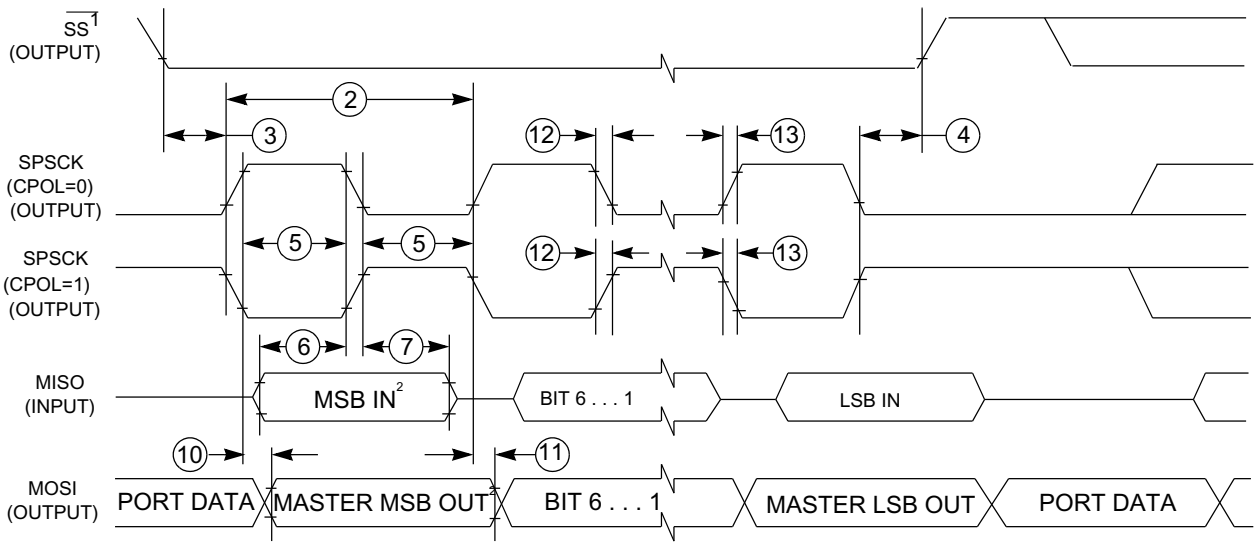
4.9 Communication interfaces

The following sections provide the information about communication interfaces.

4.9.1 LPSPI timing parameters

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 35. LPSPI Master mode timing (CPHA = 1)

Table 56. LPSPI Slave mode timing

Number	Symbol	Description	Min.	Max.	Units	Note
1	f_{OP}	Frequency of operation	0	f_{periph} / 2	Hz	[1]
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	[2]
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	[3]
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	[4]
10	t_V	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI} t_{FI}	Rise time input Fall time input	—	$t_{periph - 25}$	ns	—
13	t_{RO} t_{FO}	Rise time input Fall time input	—	25	ns	—

1 Absolute maximum frequency of operation (fop) is 30 MHz. The clock driver in the LPSPI module for f_{periph} must be guaranteed this limit is not exceeded.

2 $t_{periph} = 1 / f_{periph}$

3 Time to data active from high-impedance state

4 Hold time to high-impedance state

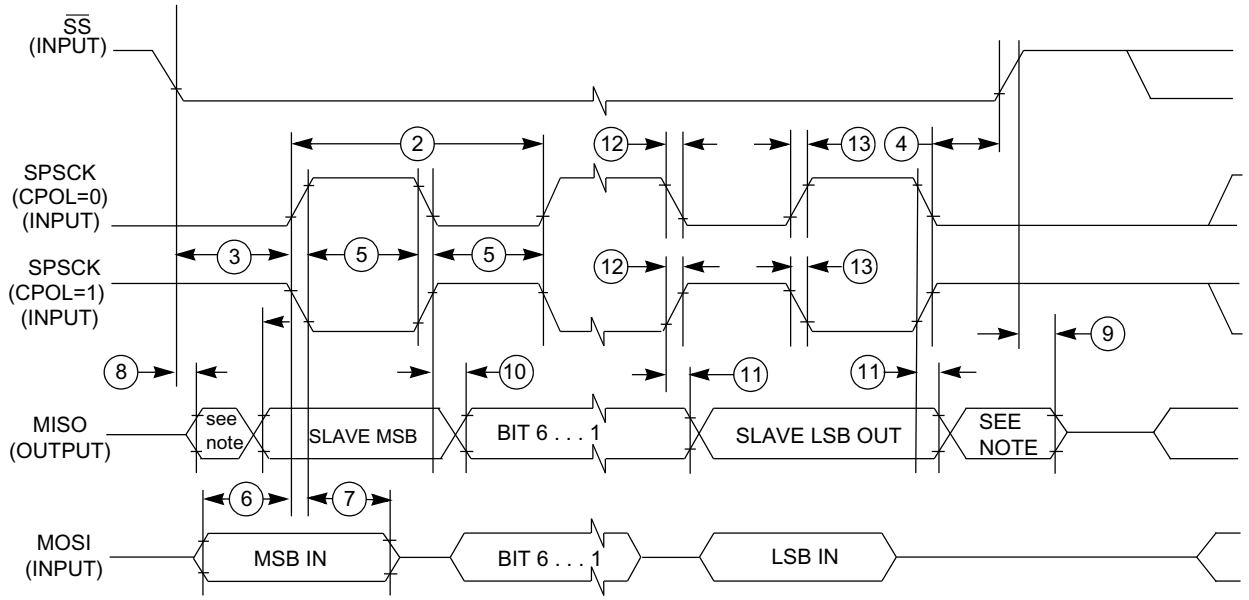


Figure 36. LPSPI Slave mode timing (CPHA = 0)

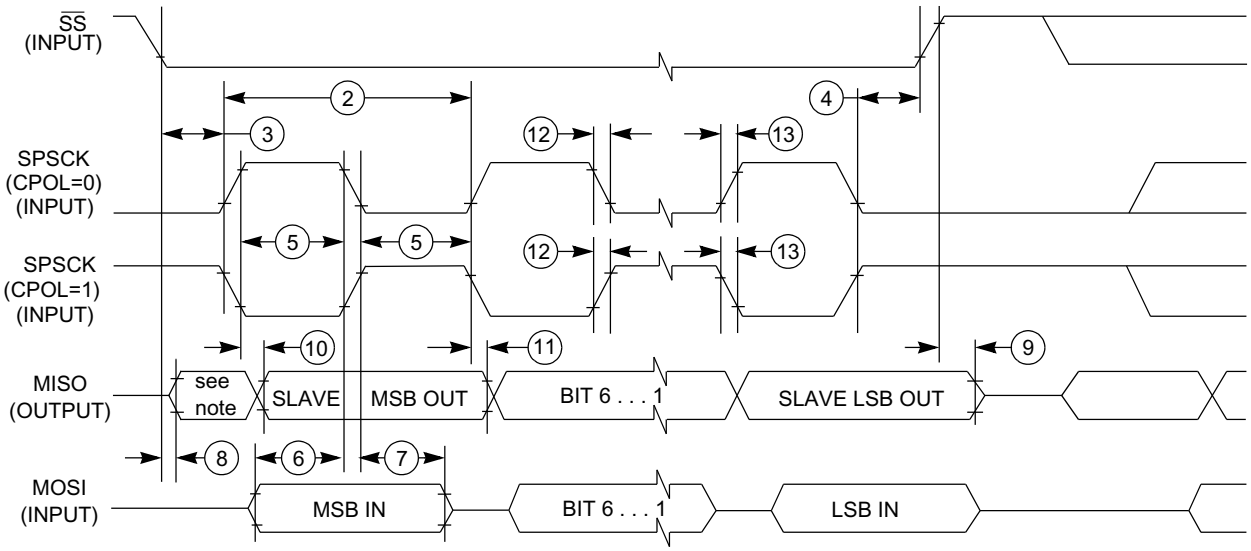


Figure 37. LPSPI Slave mode timing (CPHA = 1)

Table 72. Boot through FlexSPI (continued)

PAD Name	IO Function	Mux Mode	Comments
GPIO_SD_B1_10	flexspi.A_DATA[2]	ALT 1	—
GPIO_SD_B1_11	flexspi.A_DATA[3]	ALT 1	—

Table 73. Boot through SD1

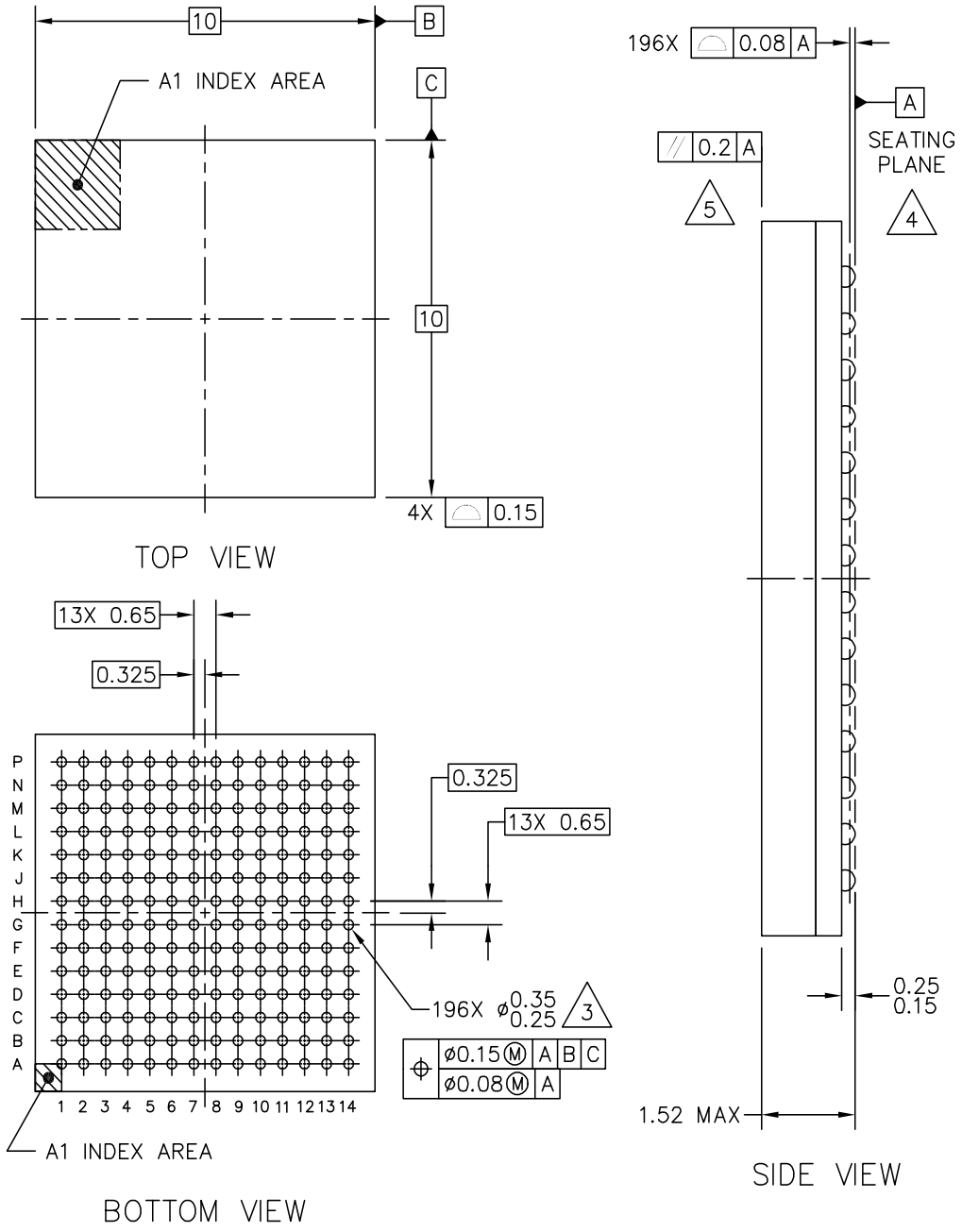
PAD Name	IO Function	Mux Mode	Comments
GPIO_SD_B0_00	usdhc1.CMD	ALT 0	—
GPIO_SD_B0_01	usdhc1.CLK	ALT 0	—
GPIO_SD_B0_02	usdhc1.DATA0	ALT 0	—
GPIO_SD_B0_03	usdhc1.DATA1	ALT 0	—
GPIO_SD_B0_04	usdhc1.DATA2	ALT 0	—
GPIO_SD_B0_05	usdhc1.DATA3	ALT 0	—

Table 74. Boot through SD2

PAD Name	IO Function	Mux Mode	Comments
GPIO_SD_B1_00	usdhc2.DATA3	ALT 0	—
GPIO_SD_B1_01	usdhc2.DATA2	ALT 0	—
GPIO_SD_B1_02	usdhc2.DATA1	ALT 0	—
GPIO_SD_B1_03	usdhc2.DATA0	ALT 0	—
GPIO_SD_B1_04	usdhc2.CLK	ALT 0	—
GPIO_SD_B1_05	usdhc2.CMD	ALT 0	—
GPIO_SD_B1_06	usdhc2.RESET_B	ALT 0	—
GPIO_SD_B1_08	usdhc2.DATA4	ALT 0	—
GPIO_SD_B1_09	usdhc2.DATA5	ALT 0	—
GPIO_SD_B1_10	usdhc2.DATA6	ALT 0	—
GPIO_SD_B1_11	usdhc2.DATA7	ALT 0	—

Table 75. Boot through SPI-1

PAD Name	IO Function	Mux Mode	Comments
GPIO_SD_B0_00	lpspi1.SCK	ALT 4	—
GPIO_SD_B0_02	lpspi1.SDO	ALT 4	—
GPIO_SD_B0_03	lpspi1.SDI	ALT 4	—
GPIO_SD_B0_01	lpspi1.PCS0	ALT 4	—



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TITLE: PBGA, LOW PROFILE, FINE PITCH, 196 I/O, 10 X 10 PKG, 0.65 MM PITCH (MAP)	DOCUMENT NO: 98ASA00030D	REV: A
	STANDARD: NON-JEDEC	
	SOT1546-1	05 JAN 2016

Figure 48. 10 x 10 mm BGA, case x package top, bottom, and side Views

Table 82. 10 x 10 mm functional contact assignments (continued)

GPIO_AD_B0_00	M14	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[0]	Input	Keeper
GPIO_AD_B0_01	H10	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[1]	Input	Keeper
GPIO_AD_B0_02	M11	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[2]	Input	Keeper
GPIO_AD_B0_03	G11	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[3]	Input	Keeper
GPIO_AD_B0_04	F11	NVCC_GPIO	Digital GPIO	ALT0	SRC.BOOT.MODE[0]	Input	100 K PD
GPIO_AD_B0_05	G14	NVCC_GPIO	Digital GPIO	ALT0	SRC.BOOT.MODE[1]	Input	100 K PD
GPIO_AD_B0_06	E14	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.TMS	Input	47 K PU
GPIO_AD_B0_07	F12	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.TCK	Input	47 K PU
GPIO_AD_B0_08	F13	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.MOD	Input	100 K PU
GPIO_AD_B0_09	F14	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.TDI	Input	47 K PU
GPIO_AD_B0_10	G13	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.TDO	Input	Keeper
GPIO_AD_B0_11	G10	NVCC_GPIO	Digital GPIO	ALT0	JTAG.MUX.TRSTB	Input	47 K PU
GPIO_AD_B0_12	K14	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[12]	Input	Keeper
GPIO_AD_B0_13	L14	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[13]	Input	Keeper
GPIO_AD_B0_14	H14	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[14]	Input	Keeper
GPIO_AD_B0_15	L10	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[15]	Input	Keeper
GPIO_AD_B1_00	J11	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[16]	Input	Keeper
GPIO_AD_B1_01	K11	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[17]	Input	Keeper
GPIO_AD_B1_02	L11	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[18]	Input	Keeper
GPIO_AD_B1_03	M12	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[19]	Input	Keeper
GPIO_AD_B1_04	L12	NVCC_GPIO	Digital GPIO	ALT5	GPIO1.IO[20]	Input	Keeper

Table 82. 10 x 10 mm functional contact assignments (continued)

GPIO_B0_10	D9	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[10]	Input	Keeper
GPIO_B0_11	A10	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[11]	Input	Keeper
GPIO_B0_12	C10	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[12]	Input	Keeper
GPIO_B0_13	D10	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[13]	Input	Keeper
GPIO_B0_14	E10	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[14]	Input	Keeper
GPIO_B0_15	E11	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[15]	Input	Keeper
GPIO_B1_00	A11	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[16]	Input	Keeper
GPIO_B1_01	B11	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[17]	Input	Keeper
GPIO_B1_02	C11	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[18]	Input	Keeper
GPIO_B1_03	D11	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[19]	Input	Keeper
GPIO_B1_04	E12	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[20]	Input	Keeper
GPIO_B1_05	D12	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[21]	Input	Keeper
GPIO_B1_06	C12	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[22]	Input	Keeper
GPIO_B1_07	B12	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[23]	Input	Keeper
GPIO_B1_08	A12	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[24]	Input	Keeper
GPIO_B1_09	A13	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[25]	Input	Keeper
GPIO_B1_10	B13	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[26]	Input	Keeper
GPIO_B1_11	C13	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[27]	Input	Keeper
GPIO_B1_12	D13	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[28]	Input	Keeper
GPIO_B1_13	D14	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[29]	Input	Keeper
GPIO_B1_14	C14	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[30]	Input	Keeper

Table 82. 10 x 10 mm functional contact assignments (continued)

GPIO_B1_15	B14	NVCC_GPIO	Digital GPIO	ALT5	GPIO2.IO[31]	Input	Keeper
GPIO_EMC_00	E3	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[0]	Input	Keeper
GPIO_EMC_01	F3	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[1]	Input	Keeper
GPIO_EMC_02	F4	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[2]	Input	Keeper
GPIO_EMC_03	G4	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[3]	Input	Keeper
GPIO_EMC_04	F2	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[4]	Input	Keeper
GPIO_EMC_05	G5	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[5]	Input	Keeper
GPIO_EMC_06	H5	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[6]	Input	Keeper
GPIO_EMC_07	H4	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[7]	Input	Keeper
GPIO_EMC_08	H3	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[8]	Input	Keeper
GPIO_EMC_09	C2	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[9]	Input	Keeper
GPIO_EMC_10	G1	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[10]	Input	Keeper
GPIO_EMC_11	G3	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[11]	Input	Keeper
GPIO_EMC_12	H1	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[12]	Input	Keeper
GPIO_EMC_13	A6	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[13]	Input	Keeper
GPIO_EMC_14	B6	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[14]	Input	Keeper
GPIO_EMC_15	B1	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[15]	Input	Keeper
GPIO_EMC_16	A5	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[16]	Input	Keeper
GPIO_EMC_17	A4	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[17]	Input	Keeper
GPIO_EMC_18	B2	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[18]	Input	Keeper
GPIO_EMC_19	B4	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[19]	Input	Keeper

Table 82. 10 x 10 mm functional contact assignments (continued)

GPIO_EMC_20	A3	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[20]	Input	Keeper
GPIO_EMC_21	C1	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[21]	Input	Keeper
GPIO_EMC_22	F1	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[22]	Input	Keeper
GPIO_EMC_23	G2	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[23]	Input	Keeper
GPIO_EMC_24	D3	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[24]	Input	Keeper
GPIO_EMC_25	D2	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[25]	Input	Keeper
GPIO_EMC_26	B3	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[26]	Input	Keeper
GPIO_EMC_27	A2	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[27]	Input	100 K PD
GPIO_EMC_28	D1	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[28]	Input	Keeper
GPIO_EMC_29	E1	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[29]	Input	Keeper
GPIO_EMC_30	C6	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[30]	Input	Keeper
GPIO_EMC_31	C5	NVCC_EMC	Digital GPIO	ALT5	GPIO4.IO[31]	Input	Keeper
GPIO_EMC_32	D5	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[18]	Input	Keeper
GPIO_EMC_33	C4	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[19]	Input	Keeper
GPIO_EMC_34	D4	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[20]	Input	Keeper
GPIO_EMC_35	E5	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[21]	Input	Keeper
GPIO_EMC_36	C3	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[22]	Input	Keeper
GPIO_EMC_37	E4	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[23]	Input	Keeper
GPIO_EMC_38	D6	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[24]	Input	Keeper
GPIO_EMC_39	B7	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[25]	Input	Keeper
GPIO_EMC_40	A7	NVCC_EMC	Digital GPIO	ALT5	GPIO3.IO[26]	Input	Keeper

6.1.3 10 x 10 mm, 0.65 mm pitch, ball map

Table 83 shows the 10 x 10 mm, 0.65 mm pitch ball map for the i.MX RT1050.

Table 83. 10 x 10 mm, 0.65 mm pitch, ball map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	GPIO_EMC_27	GPIO_EMC_20	GPIO_EMC_17	GPIO_EMC_16	GPIO_EMC_13	GPIO_EMC_40	GPIO_B0_06	GPIO_B0_07	GPIO_B0_11	GPIO_B1_00	GPIO_B1_08	GPIO_B1_09	VSS	A
B	GPIO_EMC_15	GPIO_EMC_18	GPIO_EMC_26	GPIO_EMC_19	VSS	GPIO_EMC_14	GPIO_EMC_39	GPIO_B0_05	GPIO_B0_08	VSS	GPIO_B1_01	GPIO_B1_07	GPIO_B1_10	GPIO_B1_15	B
C	GPIO_EMC_21	GPIO_EMC_09	GPIO_EMC_36	GPIO_EMC_33	GPIO_EMC_31	GPIO_EMC_30	GPIO_EMC_41	GPIO_B0_04	GPIO_B0_09	GPIO_B0_12	GPIO_B1_02	GPIO_B1_06	GPIO_B1_11	GPIO_B1_14	C
D	GPIO_EMC_28	GPIO_EMC_25	GPIO_EMC_24	GPIO_EMC_34	GPIO_EMC_32	GPIO_EMC_38	GPIO_B0_00	GPIO_B0_03	GPIO_B0_10	GPIO_B0_13	GPIO_B1_03	GPIO_B1_05	GPIO_B1_12	GPIO_B1_13	D
E	GPIO_EMC_29	VSS	GPIO_EMC_00	GPIO_EMC_37	GPIO_EMC_35	NVCC_EMC	GPIO_B0_01	GPIO_B0_02	NVCC_GPIO	GPIO_B0_14	GPIO_B0_15	GPIO_B1_04	VSS	GPIO_AD_B0_06	E
F	GPIO_EMC_22	GPIO_EMC_04	GPIO_EMC_01	GPIO_EMC_02	NVCC_EMC	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	NVCC_GPIO	GPIO_AD_B0_04	GPIO_AD_B0_07	GPIO_AD_B0_08	GPIO_AD_B0_09	F
G	GPIO_EMC_10	GPIO_EMC_23	GPIO_EMC_11	GPIO_EMC_03	GPIO_EMC_05	VDD_SOC_IN	VSS	VSS	VDD_SOC_IN	GPIO_AD_B0_11	GPIO_AD_B0_03	GPIO_AD_B1_14	GPIO_AD_B0_10	GPIO_AD_B0_05	G