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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
	Ankiya
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	33MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	33
Program Memory Size	4KB (2K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	232 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c42a-33-pq

Clocking Scheme/Instruction Cycle 3.1

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3, and Q4. Internally, the program counter (PC) is incremented every Q1, and the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-3.

3.2 **Instruction Flow/Pipelining**

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3, and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (Example 3-2).

A fetch cycle begins with the program counter incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

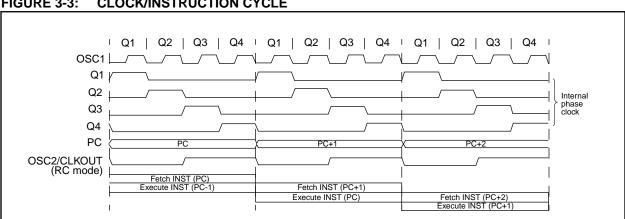
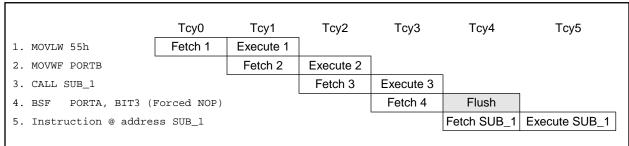


FIGURE 3-3: CLOCK/INSTRUCTION CYCLE

EXAMPLE 3-2: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

FIGURE 4-2: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

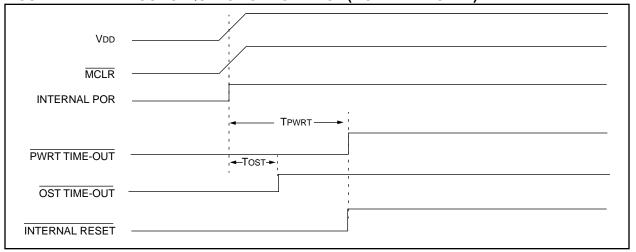


FIGURE 4-3: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD)

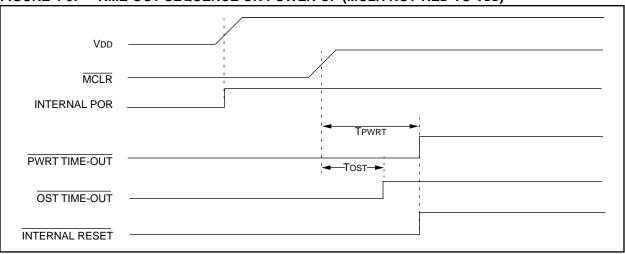
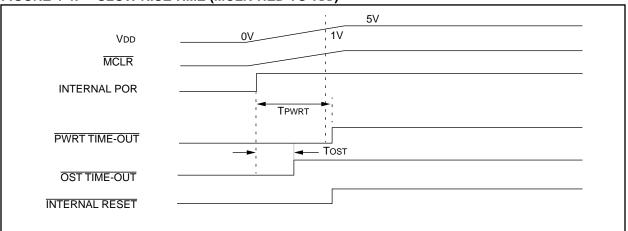


FIGURE 4-4: SLOW RISE TIME (MCLR TIED TO VDD)



Example 8-4 shows the sequence to do an 16 x 16 signed multiply. Equation 8-2 shows the algorithm that used. The 32-bit result is stored in four registers RES3:RES0. To account for the sign bits of the arguments, each argument pairs most significant bit (MSb) is tested and the appropriate subtractions are done.

EQUATION 8-2: 16 x 16 SIGNED MULTIPLICATION ALGORITHM

RES3:RES0

```
= ARG1H:ARG1L * ARG2H:ARG2L

= (ARG1H * ARG2H * 2<sup>16</sup>) + (ARG1H * ARG2L * 2<sup>8</sup>) + (ARG1L * ARG2H * 2<sup>8</sup>) + (ARG1L * ARG2L) + (-1 * ARG2H<7> * ARG1H:ARG1L * 2<sup>16</sup>) + (-1 * ARG1H<7> * ARG2H:ARG2L * 2<sup>16</sup>)
```

EXAMPLE 8-4: 16 x 16 SIGNED MULTIPLY ROUTINE

```
MOVFP
          ARG1L, WREG
  MULWF
          ARG2L
                    ; ARG1L * ARG2L ->
                     ; PRODH:PRODL
  MOVPF
          PRODH, RES1 ;
  MOVPF
          PRODL, RESO ;
  MOVFP
          ARG1H, WREG
  MULWF
          ARG2H ; ARG1H * ARG2H ->
                     ; PRODH:PRODL
  MOVPF
          PRODH, RES3 ;
  MOVPF
          PRODL, RES2 ;
  MOVED
          ARG1L, WREG
          ARG2H ; ARG1L * ARG2H ->
  MULWF
                    ; PRODH:PRODL
  MOVFP
          PRODL, WREG;
          RES1, F ; Add cross
  ADDWF
          PRODH, WREG; products
  MOVFP
  ADDWFC
          RES2, F
                  ;
          WREG, F
  CLRF
                     ;
  ADDWFC
          RES3, F
  MOVFP
          ARG1H, WREG;
          ARG2L ; ARG1H * ARG2L ->
  MULWF
                    ; PRODH:PRODL
  MOVED
          PRODL, WREG;
          RES1, F ; Add cross
  ADDWF
          PRODH, WREG; products
  MOVFP
          RES2, F ;
  ADDWFC
  CLRF
          WREG, F
                     ;
                    ;
  ADDWFC
          RES3, F
          ARG2H, 7
                   ; ARG2H:ARG2L neg?
  BTFSS
  GOTO
          SIGN_ARG1 ; no, check ARG1
  MOVFP
          ARG1L, WREG;
          RES2 ;
  SUBWE
  MOVFP
          ARG1H, WREG;
  SUBWFB
          RES3
SIGN_ARG1
          ARG1H, 7
                    ; ARG1H:ARG1L neg?
  BTFSS
  GOTO
          CONT_CODE ; no, done
  MOVFP
          ARG2L, WREG;
  SUBWF
          RES2 ;
  MOVED
          ARG2H, WREG;
  SUBWFB
          RES3
CONT_CODE
```

FIGURE 13-3: USART TRANSMIT

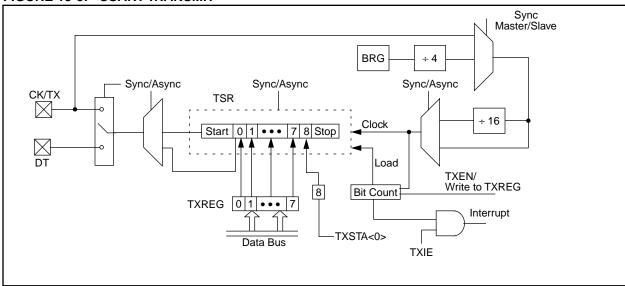
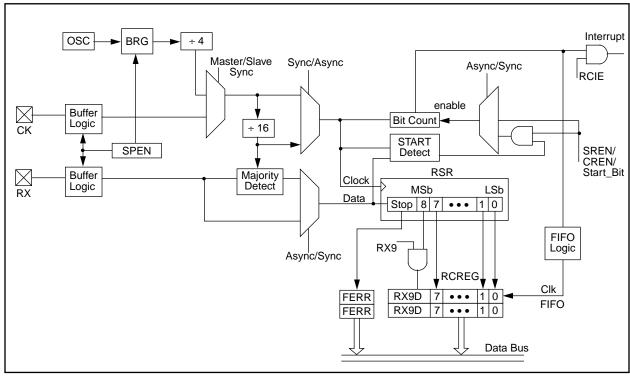


FIGURE 13-4: USART RECEIVE



13.4 <u>USART Synchronous Slave Mode</u>

The synchronous slave mode differs from the master mode in the fact that the shift clock is supplied externally at the RA5/TX/CK pin (instead of being supplied internally in the master mode). This allows the device to transfer or receive data in the SLEEP mode. The slave mode is entered by clearing the CSRC (TXSTA<7>) bit.

13.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the sync master and slave modes are identical except in the case of the SLEEP mode.

If two words are written to TXREG and then the SLEEP instruction executes, the following will occur. The first word will immediately transfer to the TSR and will transmit as the shift clock is supplied. The second word will remain in TXREG. TXIF will not be set. When the first word has been shifted out of TSR, TXREG will transfer the second word to the TSR and the TXIF flag will now be set. If TXIE is enabled, the interrupt will wake the chip from SLEEP and if the global interrupt is enabled, then the program will branch to interrupt vector (0020h).

Steps to follow when setting up a Synchronous Slave Transmission:

- Enable the synchronous slave serial port by setting the SYNC and SPEN bits and clearing the CSRC bit.
- 2. Clear the CREN bit.
- 3. If interrupts are desired, then set the TXIE bit.
- If 9-bit transmission is desired, then set the TX9 bit.
- 5. Start transmission by loading data to TXREG.
- If 9-bit transmission is selected, the ninth bit should be loaded in TX9D.
- 7. Enable the transmission by setting TXEN.

Writing the transmit data to the TXREG, then enabling the transmit (setting TXEN) allows transmission to start sooner then doing these two events in the reverse order.

Note:

To terminate a transmission, either clear the SPEN bit, or the TXEN bit. This will reset the transmit logic, so that it will be in the proper state when transmit is re-enabled.

13.4.2 USART SYNCHRONOUS SLAVE RECEPTION

Operation of the synchronous master and slave modes are identical except in the case of the SLEEP mode. Also, SREN is a don't care in slave mode.

If receive is enabled (CREN) prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR will transfer the data to RCREG (setting RCIF) and if the RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0020h).

Steps to follow when setting up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting the SYNC and SPEN bits and clearing the CSRC bit.
- 2. If interrupts are desired, then set the RCIE bit.
- 3. If 9-bit reception is desired, then set the RX9 bit.
- 4. To enable reception, set the CREN bit.
- The RCIF bit will be set when reception is complete and an interrupt will be generated if the RCIE bit was set.
- Read RCSTA to get the ninth bit (if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading RCREG.
- 8. If any error occurred, clear the error by clearing the CREN bit.

Note: To abort reception, either clear the SPEN bit, the SREN bit (when in single receive mode), or the CREN bit (when in continuous receive mode). This will reset the receive logic, so that it will be in the proper state when receive is re-enabled.

14.2.4 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with series resonance, or one with parallel resonance.

Figure 14-5 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 14-5: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

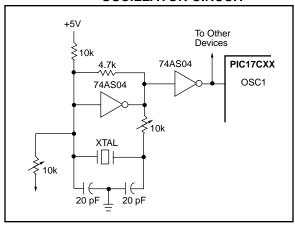
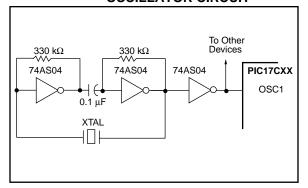


Figure 14-6 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 k Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 14-6: EXTERNAL SERIES
RESONANT CRYSTAL
OSCILLATOR CIRCUIT



14.2.5 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 14-6 shows how the R/C combination is connected to the PIC17CXX. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 $M\Omega$), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 $k\Omega$ and 100 $k\Omega$.

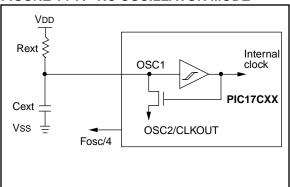
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With little or no external capacitance, oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 18.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 18.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-2 for waveform).

FIGURE 14-7: RC OSCILLATOR MODE



BSF Bit Set f Syntax: [label] BSF f,b Operands: $0 \le f \le 255$ $0 \le b \le 7$ Operation: $1 \rightarrow (f {<} b {>})$ Status Affected: None Encoding: 1000 ffff ffff 0bbb Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Execute	Write
	register 'f'		register 'f'

Example: BSF FLAG_REG, 7

1

Before Instruction FLAG_REG= 0x0A

After Instruction

FLAG_REG= 0x8A

BTFSC	Bit Test,	Bit Test, skip if Clear							
Syntax:	[label] E	[label] BTFSC f,b							
Operands:	$0 \le f \le 25$ $0 \le b \le 7$	$0 \le f \le 255$ $0 \le b \le 7$							
Operation:	skip if $(f < b >) = 0$								
Status Affected:	None								
Encoding:	1001	1bbb	ffff	ffff					
Description:		If bit 'b' in register 'f' is 0 then the next instruction is skipped.							
	fetched du) then the n ring the cur scarded, ar	rent instru	ction exe-					

instruction.

Words: 1 Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Execute	NOP
	register 'f'		

cuted instead, making this a two-cycle

If skip:

Q1	Q2	Q3	Q4
Forced NOP	NOP	Execute	NOP

Example: HERE BTFSC FLAG,1 FALSE: TRUE:

Before Instruction

PC = address (HERE)

After Instruction

If FLAG<1> = 0;

PC = address (TRUE)

If FLAG<1> = 1;

PC = address (FALSE)

CPFSEQ	Compare skip if f =	e f with WRE WREG	G,	СР	FSGT	Compare skip if f >		/REG,	
Syntax:	[label]	CPFSEQ f		Sy	ntax:	[label] (CPFSGT	f	
Operands:	$0 \le f \le 25$	5		Ор	erands:	$0 \le f \le 25$	5		
Operation:	(f) – (WRE skip if (f) = (unsigned	, .		Ор	eration:	(f) – (WREG skip if (f) > (unsigned G	(WREG)	on)	
Status Affected:	None			Sta	atus Affected:	None			
Encoding:	0011	0001 ff	ff ffff	En	coding:	0011	0010	ffff	ffff
Description:	location 'f'	the contents of to the contents an unsigned	•	De	scription:	Compares location 'f' to by perform	to the con	tents of th signed su	ne WREG btraction.
	tion is disc	EG then the fet arded and an ead making this	NOP is exe-			If the conte WREG the discarded a instead ma tion.	n the fetcl and an NO	ned instru DP is exec	ction is
Words:	1			\\/c	ords:	1			
Cycles:	1 (2)					1 (2)			
Q Cycle Activity:				•	cles:	1 (2)			
Q1	Q2	Q3	Q4	Ų(¬	Cycle Activity: Q1	Q2	Q3		Q4
Decode	Read register 'f'	Execute	NOP		Decode	Read register 'f'	Execu		NOP
If skip:				If s	kip:	register i			
Q1	Q2	Q3	Q4	s 1	Q1	Q2	Q3		Q4
Forced NOP	NOP	Execute	NOP		Forced NOP	NOP	Execu	te	NOP
Example:	HERE NEQUAL EQUAL	CPFSEQ REG:		Ex	ample:	HERE NGREATER	CPFSG	T REG	
Before Instru PC Addre WREG REG		ERE			Before Instru PC WREG		: ddress (H	ERE)	
After Instruct		/REG;			After Instruc		REG;		

If REG

PC

РС

WREG;

 \neq

Address (EQUAL)

Address (NEQUAL)

Address (GREATER)

Address (NGREATER)

WREG;

PC

If REG

Applicable Devices 42 R42 42A 43 R43 44

17.3 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created using one of the following formats:

1. TppS2ppS

2. TppS

2. TppS				
Т				
F	Frequency	Т	Time	
Lowerd	case symbols (pp) and their meanings:			
рр				
ad	Address/Data	ost	Oscillator Start-up Timer	
al	ALE	pwrt	Power-up Timer	
СС	Capture1 and Capture2	rb	PORTB	
ck	CLKOUT or clock	rd	RD	
dt	Data in	rw	RD or WR	
in	INT pin	tO	TOCKI	
io	I/O port	t123	TCLK12 and TCLK3	
mc	MCLR	wdt	Watchdog Timer	
oe	ŌĒ	wr	WR	
os	OSC1			
Upper	case symbols and their meanings:			
S				
D	Driven	L	Low	
E	Edge	P	Period	
F	Fall	R	Rise	
Н	High	V	Valid	
1	Invalid (Hi-impedance)	Z	Hi-impedance	

Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44

FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

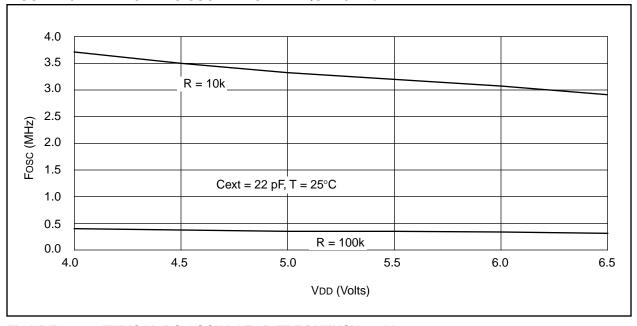
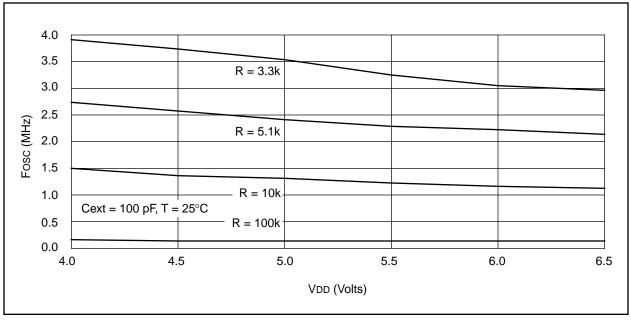


FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44

FIGURE 18-19: VTH, VIL of I/O PINS (SCHMITT TRIGGER) vs. VDD

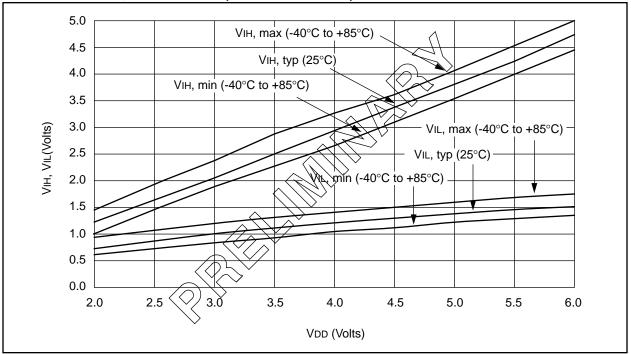
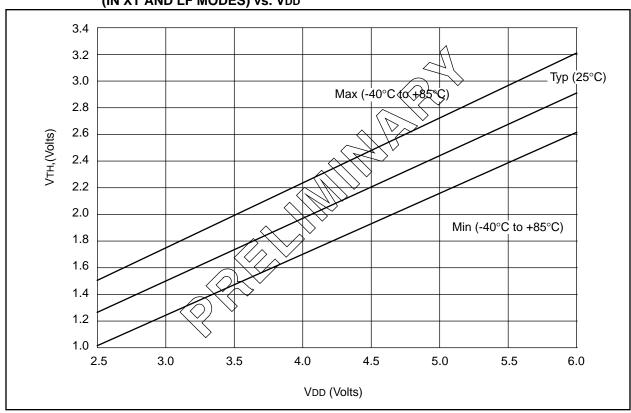


FIGURE 18-20: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT AND LF MODES) vs. VDD



NOTES:

Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44

FIGURE 19-7: CAPTURE TIMINGS

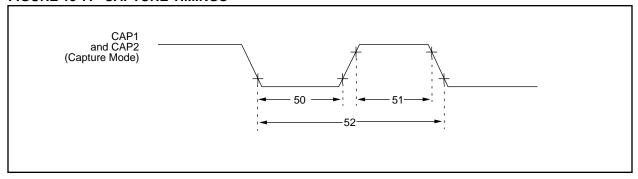


TABLE 19-7: CAPTURE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
50	TccL	Capture1 and Capture2 input low time	10 *	_	_	ns	
51	TccH	Capture1 and Capture2 input high time	10 *	_	_	ns	
52	TccP	Capture1 and Capture2 input period	2Tcy § N	_	_	ns	N = prescale value (4 or 16)

- These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- § This specification ensured by design.

FIGURE 19-8: PWM TIMINGS

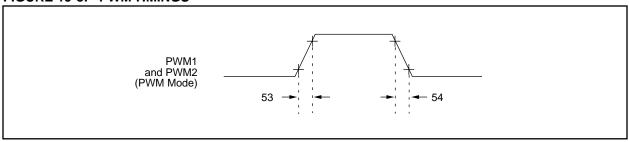


TABLE 19-8: PWM REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
53	TccR	PWM1 and PWM2 output rise time	_	10 *	35 *§	ns	
54	TccF	PWM1 and PWM2 output fall time	_	10 *	35 *§	ns	

These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

[§] This specification ensured by design.

Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44

FIGURE 19-9: USART MODULE: SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

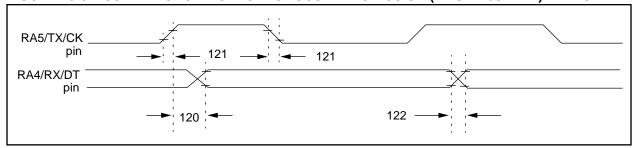


TABLE 19-9: SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE)	PIC17CR42/42A/43/R43/44	_	_	50	ns	
		Clock high to data out valid	PIC17LCR42/42A/43/R43/44	_	_	75	ns	
121	TckRF	Clock out rise time and fall time	PIC17CR42/42A/43/R43/44	_	_	25	ns	
		(Master Mode)	PIC17LCR42/42A/43/R43/44	_	_	40	ns	
122	TdtRF	Data out rise time and fall time	PIC17CR42/42A/43/R43/44	_	_	25	ns	
			PIC17LCR42/42A/43/R43/44	_	_	40	ns	

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-10: USART MODULE: SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

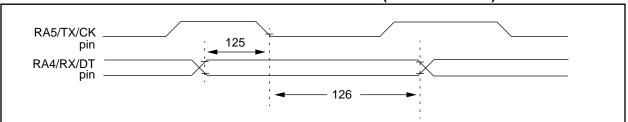


TABLE 19-10: SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
125	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data hold before CK↓ (DT hold time)	15	_	_	ns	
126	TckL2dtl	Data hold after CK↓ (DT hold time)	15	_	_	ns	

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices 42 R42 42A 43 R43 44

FIGURE 19-12: MEMORY INTERFACE READ TIMING (NOT SUPPORTED IN PIC17LC4X DEVICES)

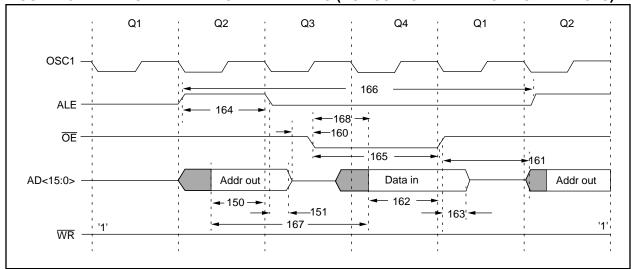


TABLE 19-12: MEMORY INTERFACE READ REQUIREMENTS (NOT SUPPORTED IN PIC17LC4X DEVICES)

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
150	TadV2alL	AD15:AD0 (address) valid to ALE↓ (address setup time)	0.25Tcy - 10	_	_	ns	
151	TalL2adl	ALE↓ to address out invalid (address hold time)	5*	_	_	ns	
160	TadZ2oeL	AD15:AD0 hi-impedance to OE ↓	0*	_	_	ns	
161	ToeH2adD	OE↑ to AD15:AD0 driven	0.25Tcy - 15	_	_	ns	
162	TadV2oeH	Data in valid before OE ↑ (data setup time)	35	_	_	ns	
163	ToeH2adl	OE↑to data in invalid (data hold time)	0	_	_	ns	
164	TalH	ALE pulse width	_	0.25Tcy §	_	ns	
165	ToeL	OE pulse width	0.5Tcy - 35 §	_	_	ns	
166	TalH2alH	ALE↑ to ALE↑(cycle time)	_	Tcy §	_	ns	
167	Tacc	Address access time	_	_	0.75Tcy - 30	ns	
168	Toe	Output enable access time (OE low to Data Valid)	_	_	0.5Tcy - 45	ns	

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

[§] This specification ensured by design.

Applicable Devices 42 R42 42A 43 R43 44

FIGURE 20-13: WDT TIMER TIME-OUT PERIOD vs. VDD

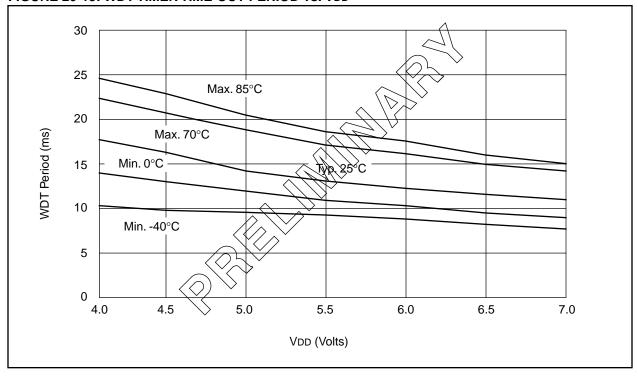
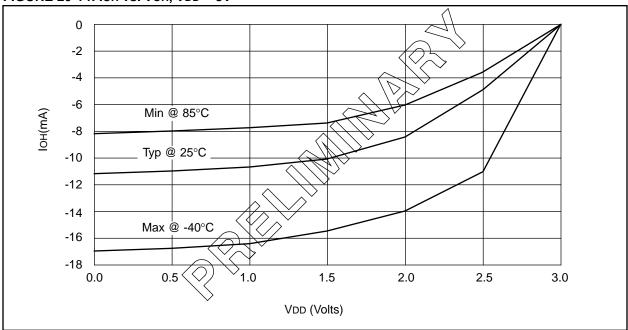


FIGURE 20-14: IOH vs. VOH, VDD = 3V



ndirect Addressing		TSTFSZ	140
Indirect Addressing	39	XORLW	141
Operation	40	XORWF	141
Registers		Instruction Set Summary	107
nitialization Conditions For Special Function Registers	19	INT Pin	
nitializing PORTB		INTE	
nitializing PORTC		INTEDG	
nitializing PORTD		Interrupt on Change Feature	, -
nitializing PORTE		Interrupt Status Register (INTSTA)	
nstruction Flow/Pipelining		Interrupt Status Register (INTSTA)	
		•	07
nstruction Set		Context Saving	21
ADDLW		Flag bits	0.4
ADDWF		TMR1IE	
ADDWFC	113	TMR1IF	
ANDLW	113	TMR2IE	21
ANDWF	114	TMR2IF	21
BCF	114	TMR3IE	21
BSF	115	TMR3IF	21
BTFSC	115	Interrupts	21
BTFSS		Logic	
BTG		Operation	
CALL		Peripheral Interrupt Enable	
CLRF		Peripheral Interrupt Request	
CLRWDT		PWM	
COMF		Status Register	
CPFSEQ	119	Table Write Interaction	
CPFSGT	119	Timing	26
CPFSLT	120	Vectors	
DAW	120	Peripheral Interrupt	26
DECF	121	RA0/INT Interrupt	
DECFSNZ	122	T0CKI Interrupt	
DECFSZ		TMR0 Interrupt	
GOTO		Vectors/Priorities	
INCF			
		Wake-up from SLEEP	
INCFSNZ		INTF	
INCFSZ	_	INTSTA	
IORLW		INTSTA Register	
IORWF	125	IORLW	
LCALL	125	IORWF	125
MOVFP	126		
MOVLB	126		
MOVLR	127	L	
MOVLW	127		
MOVPF	128	LCALL	
MOVWF		Long Writes	45
MULLW			
MULWF		8.4	
		М	
NEGW			
NOP		Memory	
RETFIE	131	External Interface	31
RETLW	131	External Memory Waveforms	31
RETURN	132	Memory Map (Different Modes)	30
RLCF	132	Mode Memory Access	
RLNCF	133	Organization	
RRCF	133	Program Memory	
RRNCF		Program Memory Map	
SETF			
SLEEP		Microcontroller	
		Microprocessor	
SUBLW		Minimizing Current Consumption	
SUBWF		MOVFP	
SUBWFB		MOVLB	126
SWAPF	137	MOVLR	127
TABLRD13	7, 138	MOVLW	
TABLWT13	8, 139	MOVPF	
TLRD	139	MOVWF	
TLWT		MPASM Assembler	
	•	INII 401NI 499EHIDIEI	140, 144

Figure 19-2:	External Clock Timing	184	Table 6-2:	EPROM Memory Access Time	
Figure 19-3:	CLKOUT and I/O Timing	185		Ordering Suffix	.31
Figure 19-4:	Reset, Watchdog Timer,		Table 6-3:	Special Function Registers	.34
	Oscillator Start-Up Timer, and		Table 7-1:	Interrupt - Table Write Interaction	.45
	Power-Up Timer Timing	186	Table 8-1:	Performance Comparison	.49
Figure 19-5:	Timer0 Clock Timings	187	Table 9-1:	PORTA Functions	.54
Figure 19-6:	Timer1, Timer2, and Timer3 Clock		Table 9-2:	Registers/Bits Associated with PORTA	.54
-	Timings	187	Table 9-3:	PORTB Functions	.57
Figure 19-7:	Capture Timings		Table 9-4:	Registers/Bits Associated with PORTB	
Figure 19-8:	PWM Timings		Table 9-5:	PORTC Functions	
Figure 19-9:	USART Module: Synchronous		Table 9-6:	Registers/Bits Associated with PORTC	
J	Transmission (Master/Slave) Timing	189	Table 9-7:	PORTD Functions	
Figure 19-10:	USART Module: Synchronous		Table 9-8:	Registers/Bits Associated with PORTD	.61
J	Receive (Master/Slave) Timing	189	Table 9-9:	PORTE Functions	
Figure 19-11:	Memory Interface Write Timing		Table 9-10:	Registers/Bits Associated with PORTE	
3	(Not Supported in PIC17LC4X Devices)	190	Table 11-1:	Registers/Bits Associated with Timer0	
Figure 19-12:	Memory Interface Read Timing		Table 12-1:	Turning On 16-bit Timer	
	(Not Supported in PIC17LC4X Devices)	191	Table 12-2:	Summary of Timer1 and Timer2	
Figure 20-1:	Typical RC Oscillator Frequency vs.			Registers	.74
	Temperature	193	Table 12-3:	PWM Frequency vs. Resolution at	
Figure 20-2:	Typical RC Oscillator Frequency			25 MHz	.76
ga. o _o	vs. VDD	194	Table 12-4:	Registers/Bits Associated with PWM	
Figure 20-3:	Typical RC Oscillator Frequency		Table 12-5:	Registers Associated with Capture	
1 1guio 20 0.	vs. VDD	194	Table 12-6:	Summary of TMR1, TMR2, and TMR3	0
Figure 20-4:	Typical RC Oscillator Frequency	104	14510 12 0.	Registers	81
1 1ga10 20 1.	vs. VDD	195	Table 13-1:	Baud Rate Formula	
Figure 20-5:	Transconductance (gm) of LF Oscillator	100	Table 13-2:	Registers Associated with Baud Rate	.00
riguic 20 3.	vs. VDD	196	Table 10-2.	Generator	86
Figure 20-6:	Transconductance (gm) of XT Oscillator	100	Table 13-3:	Baud Rates for Synchronous Mode	
riguic 20 0.	vs. VDD	106	Table 13-4:	Baud Rates for Asynchronous Mode	
Figure 20-7:	Typical IDD vs. Frequency (External	190	Table 13-4:	Registers Associated with Asynchronous	.00
riguic 20 7.	Clock 25°C)	107	Table 15 5.	Transmission	an
Figure 20-8:	Maximum IDD vs. Frequency (External	191	Table 13-6:	Registers Associated with Asynchronous	.90
rigule 20-6.	Clock 125°C to -40°C)	107	Table 13-0.	Reception	വാ
Figure 20-9:	Typical IPD vs. VDD Watchdog	191	Table 13-7:	Registers Associated with Synchronous	.92
rigule 20-9.	Disabled 25°C	100	Table 13-7.	•	0.4
Figure 20 10:	Maximum IPD vs. VDD Watchdog	190	Table 13-8:	Master Transmission Registers Associated with Synchronous	.94
Figure 20-10.	Disabled	100	Table 13-0.		06
Figure 20 11:	Typical IPD vs. VDD Watchdog	190	Table 13-9:	Master Reception Registers Associated with Synchronous	.90
rigule 20-11.	Enabled 25°C	100	Table 13-9.	Slave Transmission	00
Figure 20 12:		199	Toble 12 10:	Registers Associated with Synchronous	.90
Figure 20-12.	Maximum IPD vs. VDD Watchdog	100	Table 13-10:		00
Eiguro 20 12:	Enabled		Toble 14 1:	Slave Reception	
-	WDT Timer Time-Out Period vs. VDD		Table 14-1:	Configuration Locations	UU
-	IOH vs. VOH, VDD = 3V		Table 14-2:	Capacitor Selection for Ceramic	104
	IOH VS. VOH, VDD = 5V		Toble 14.2:	Resonators	UI
	IOL vs. VOL, VDD = 3V		Table 14-3:	Capacitor Selection for Crystal	104
	IOL VS. VOL, VDD = 5V	202	Table 4.4.4.	OscillatoR	UI
Figure 20-16.	VTH (Input Threshold Voltage) of	202	Table 14-4:	Registers/Bits Associated with the	104
F: 20 40:	I/O Pins (TTL) vs. VDD	202	Table 45.4.	Watchdog Timer	
Figure 20-19:	VTH, VIL of I/O Pins (Schmitt Trigger)	000	Table 15-1:	Opcode Field Descriptions	
F: 20 20:	VS. VDD	203	Table 15-2:	PIC17CXX Instruction Set	
Figure 20-20:	VTH (Input Threshold Voltage) of OSC1	000	Table 16-1:	development tools from microchip1	40
	Input (In XT and LF Modes) vs. VDD	203	Table 17-1:	Cross Reference of Device Specs for	
LIST OF TAE	RI FS			Oscillator Configurations and Frequencies	
		_		of Operation (Commercial Devices)1	
Table 1-1:	PIC17CXX Family of Devices		Table 17-2:	External Clock Timing Requirements1	
Table 3-1:	Pinout Descriptions		Table 17-3:	CLKOUT and I/O Timing Requirements1	56
Table 4-1:	Time-Out in Various Situations		Table 17-4:	Reset, Watchdog Timer,	
Table 4-2:	STATUS Bits and Their Significance	. 16		Oscillator Start-Up Timer and	
Table 4-3:	Reset Condition for the Program Counter			Power-Up Timer Requirements1	
	and the CPUSTA Register	. 16	Table 17-5:	Timer0 Clock Requirements1	58
Table 4-4:	Initialization Conditions For Special		Table 17-6:	Timer1, Timer2, and Timer3 Clock	
	Function Registers			Requirements1	
Table 5-1:	Interrupt Vectors/Priorities		Table 17-7:	Capture Requirements1	
Table 6-1:	Mode Memory Access	. 30	Table 17-8:	PWM Requirements1	159

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