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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	33MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	33
Program Memory Size	4KB (2K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	232 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c42a-33i-l

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For register and module descriptions in this data sheet, device legends show which devices apply to those sections. For example, the legend below shows that some features of only the PIC17C43, PIC17C43, PIC17C44 are described in this section.

Applicable Devices 42 R42 42A 43 R43 44

To Our Valued Customers

We constantly strive to improve the quality of all our products and documentation. We have spent an exceptional amount of time to ensure that these documents are correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error from the previous version of the PIC17C4X Data Sheet (Literature Number DS30412B), please use the reader response form in the back of this data sheet to inform us. We appreciate your assistance in making this a better document.

To assist you in the use of this document, Appendix C contains a list of new information in this data sheet, while Appendix D contains information that has changed

			-		-	
Name	DIP No.	PLCC No.	QFP No.	I/O/P Type	Buffer Type	Description
						PORTD is a bi-directional I/O Port.
RD0/AD8	40	43	15	I/O	TTL	This is also the upper byte of the 16-bit system bus in
RD1/AD9	39	42	14	I/O	TTL	microprocessor mode or extended microprocessor mode
RD2/AD10	38	41	13	I/O	TTL	or extended microcontroller mode. In multiplexed system
RD3/AD11	37	40	12	I/O	TTL	as data input or output
RD4/AD12	36	39	11	I/O	TTL	
RD5/AD13	35	38	10	I/O	TTL	
RD6/AD14	34	37	9	I/O	TTL	
RD7/AD15	33	36	8	I/O	TTL	
RE0/ALE	30	32	4	I/O	TTL	PORTE is a bi-directional I/O Port. In microprocessor mode or extended microcontroller mode, it is the Address Latch Enable (ALE) output. Address should be latched on the falling edge of ALE output.
RE1/OE	29	31	3	I/O	TTL	In microprocessor or extended microcontroller mode, it is the Output Enable (\overline{OE}) control output (active low).
RE2/WR	28	30	2	I/O	TTL	In microprocessor or extended microcontroller mode, it is the Write Enable (WR) control output (active low).
TEST	27	29	1	I	ST	Test mode selection control input. Always tie to Vss for nor- mal operation.
Vss	10, 31	11, 12, 33, 34	5, 6, 27, 28	Р		Ground reference for logic and I/O pins.
Vdd	1	1, 44	16, 17	Р		Positive supply for logic and I/O pins.

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Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input. NOTES:

TABLE 6-1: MODE MEMORY ACCESS

Operating Mode	Internal Program Memory	Configuration Bits, Test Memory, Boot ROM
Microprocessor	No Access	No Access
Microcontroller	Access	Access
Extended Microcontroller	Access	No Access
Protected Microcontroller	Access	Access

The PIC17C4X can operate in modes where the program memory is off-chip. They are the microprocessor and extended microcontroller modes. The microprocessor mode is the default for an unprogrammed device.

Regardless of the processor mode, data memory is always on-chip.

FIGURE 6-2: MEMORY MAP IN DIFFERENT MODES



8.0 HARDWARE MULTIPLIER

All PIC17C4X devices except the PIC17C42, have an 8 x 8 hardware multiplier included in the ALU of the device. By making the multiply a hardware operation, it completes in a single instruction cycle. This is an unsigned multiply that gives a 16-bit result. The result is stored into the 16-bit PRODuct register (PRODH:PRODL). The multiplier does not affect any flags in the ALUSTA register.

Making the 8 x 8 multiplier execute in a single cycle gives the following advantages:

- Higher computational throughput
- Reduces code size requirements for multiply algorithms

The performance increase allows the device to be used in applications previously reserved for Digital Signal Processors.

Table 8-1 shows a performance comparison between the PIC17C42 and all other PIC17CXX devices, which have the single cycle hardware multiply.

Example 8-1 shows the sequence to do an 8 x 8 unsigned multiply. Only one instruction is required when one argument of the multiply is already loaded in the WREG register.

Example 8-2 shows the sequence to do an 8×8 signed multiply. To account for the sign bits of the arguments, each argument's most significant bit (MSb) is tested and the appropriate subtractions are done.

EXAMPLE 8-1: 8 x 8 MULTIPLY ROUTINE

MOVFP	ARG1,	WREG					
MULWF	ARG2		;	ARG1	*	ARG2	->
			;	PRO	DDI	H:PROI	ЪГ

EXAMPLE 8-2: 8 x 8 SIGNED MULTIPLY ROUTINE

MOVFP	ARG1, WREG		
MULWF	ARG2	;	ARG1 * ARG2 ->
		;	PRODH: PRODL
BTFSC	ARG2, SB	;	Test Sign Bit
SUBWF	PRODH, F	;	PRODH = PRODH
		;	- ARG1
MOVFP	ARG2, WREG		
BTFSC	ARG1, SB	;	Test Sign Bit
SUBWF	PRODH, F	;	PRODH = PRODH
		•	- ARC2

Doutino	Device	Program Memory		Time	
Routine	Device	(Words)	Cycles (Max)	@ 25 MHz	@ 33 MHz
8 x 8 unsigned	PIC17C42	13	69	11.04 μs	N/A
	All other PIC17CXX devices	1	1	160 ns	121 ns
8 x 8 signed	PIC17C42	—	—	—	N/A
	All other PIC17CXX devices	6	6	960 ns	727 ns
16 x 16 unsigned	PIC17C42	21	242	38.72 μs	N/A
	All other PIC17CXX devices	24	24	3.84 µs	2.91 μs
16 x 16 signed	PIC17C42	52	254	40.64 μs	N/A
	All other PIC17CXX devices	36	36	5.76 μs	4.36 μs

TABLE 8-1: PERFORMANCE COMPARISON

9.4 PORTD and DDRD Registers

PORTD is an 8-bit bi-directional port. The corresponding data direction register is DDRD. A '1' in DDRD configures the corresponding port pin as an input. A '0' in the DDRC register configures the corresponding port pin as an output. Reading PORTD reads the status of the pins, whereas writing to it will write to the port latch. PORTD is multiplexed with the system bus. When operating as the system bus, PORTD is the high order byte of the address/data bus (AD15:AD8). The timing for the system bus is shown in the Electrical Characteristics section.

Note: This port is configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O. Example 9-3 shows the instruction sequence to initialize PORTD. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

EXAMPLE 9-3: INITIALIZING PORTD

MOVLB	1	;	Select Bank 1
CLRF	PORTD	;	Initialize PORTD data
		;	latches before setting
		;	the data direction
		;	register
MOVLW	0xCF	;	Value used to initialize
		;	data direction
MOVWF	DDRD	;	Set RD<3:0> as inputs
		;	RD<5:4> as outputs
		;	RD<7:6> as inputs





FIGURE 14-3: CRYSTAL OPERATION, OVERTONE CRYSTALS (XT OSC CONFIGURATION)



TABLE 14-2: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
LF	455 kHz 2.0 MHz	15 - 68 pF 10 - 33 pF
ХТ	4.0 MHz 8.0 MHz 16.0 MHz	22 - 68 pF 33 - 100 pF 33 - 100 pF

Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

Resonators Used:

455 kHz	Panasonic EFO-A455K04B	± 0.3%			
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%			
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%			
8.0 MHz	± 0.5%				
16.0 MHz Murata Erie CSA16.00MX ± 0.5%					
Resonators used did not have built-in capacitors.					

TABLE 14-3:CAPACITOR SELECTION
FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LF	32 kHz ⁽¹⁾	100-150 pF	100-150 pF
	1 MHz	10-33 pF	10-33 pF
	2 MHz	10-33 pF	10-33 pF
XT	2 MHz	47-100 pF	47-100 pF
	4 MHz	15-68 pF	15-68 pF
	8 MHz ⁽²⁾	15-47 pF	15-47 pF
	16 MHz	TBD	TBD
	25 MHz	15-47 pF	15-47 pF
	32 MHz ⁽³⁾	₍₃₎	₍₃₎

Higher capacitance increases the stability of the oscillator but also increases the start-up time and the oscillator current. These values are for design guidance only. Rs may be required in XT mode to avoid overdriving the crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values for external components.

- Note 1: For VDD > 4.5V, C1 = C2 \approx 30 pF is recommended.
 - 2: Rs of 330Ω is required for a capacitor combination of 15/15 pF.
 - 3: Only the capacitance of the board was present.

Crystals Used:

32.768 kHz	Epson C-001R32.768K-A	± 20 PPM
1.0 MHz	ECS-10-13-1	\pm 50 PPM
2.0 MHz	ECS-20-20-1	± 50 PPM
4.0 MHz	ECS-40-20-1	± 50 PPM
8.0 MHz	ECS ECS-80-S-4	± 50 PPM
	ECS-80-18-1	
16.0 MHz	ECS-160-20-1	TBD
25 MHz	CTS CTS25M	± 50 PPM
32 MHz	CRYSTEK HF-2	± 50 PPM

14.2.3 EXTERNAL CLOCK OSCILLATOR

In the EC oscillator mode, the OSC1 input can be driven by CMOS drivers. In this mode, the OSC1/CLKIN pin is hi-impedance and the OSC2/CLK-OUT pin is the CLKOUT output (4 Tosc).

FIGURE 14-4: EXTERNAL CLOCK INPUT OPERATION (EC OSC CONFIGURATION)



MULLW	Multiply I	_iteral with V	VREG	MUL	WF	Multiply V	VREG with f	:
Syntax:	[label]	MULLW k		Synt	ax:	[label]	MULWF f	
Operands:	$0 \le k \le 25$	5		Ope	rands:	$0 \le f \le 25$	5	
Operation:	(k x WRE	G) \rightarrow PRODH	H:PRODL	Ope	ration:	(WREG x	f) \rightarrow PRODH	I:PRODL
Status Affected:	None			Statu	us Affected:	None		
Encoding:	1011	1100 kkl	kk kkkk	Enco	oding:	0011	0100 fff	f ffff
Description:	An unsigne out betwee and the 8-b result is pla register pai high byte. WREG is u None of the Note that n is possible result is po	d multiplication n the contents it literal 'k'. The iced in PRODH r. PRODH con nchanged. e status flags a either overflow in this operatic ssible but not c	n is carried of WREG = 16-bit H:PRODL tains the are affected. y nor carry on. A zero detected.	Desc	cription:	An unsigne out betwee and the reg 16-bit resul PRODH:PF PRODH co Both WREC None of the Note that n is possible result is po	d multiplication n the contents jister file locati t is stored in th RODL register ntains the high G and 'f' are ur e status flags a either overflow in this operation ssible but not of	n is carried of WREG on 'f'. The ne pair. n byte. nchanged. are affected. v nor carry on. A zero detected.
Words:	1			Word	ds:	1		
Cycles:	1			Cycl	es:	1		
Q Cycle Activity:				Q Cy	cle Activity:			
Q1	Q2	Q3	Q4	-	Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Execute	Write registers PRODH: PRODL		Decode	Read register 'f'	Execute	Write registers PRODH: PRODL
Example:	MULLW	0xC4		<u>Exar</u>	nple:	MULWF	REG	
Before Instru WREG PRODH PRODL After Instruc	uction = 0x = ? = ? tion	Æ2			Before Instru WREG REG PRODH PRODL	uction = 0> = 0> = ? = ?	(C4 (B5	
WREG PRODH PRODL	= 0 = 0 = 0 instruction	(C4 (AD (08 is not avail	able in the		After Instruc WREG REG PRODH PRODL	tion = 0> = 0> = 0> = 0>	xC4 (B5 (8A (94	
		•		No	ote: This PIC1	instruction 7C42 device	is not avail	able in the

PIC17C4X

RLNCF Rotate Left f (no carry)								
Synt	ax:	[label]	RLN	ICF	f,d		
Ope	rands:	0 d	≤ f ≤ 2 ∈ [0,1	255]				
Ope	ration:	f∢ f	$\langle n \rangle \rightarrow \langle 7 \rangle \rightarrow$	d <n+ d<0></n+ 	1>;			
Statu	us Affected:	Ν	lone					
Enco	oding:	Γ	0010	00	1d	ff	ff	ffff
Deso	cription:	T o p s	he cont ne bit to laced ir tored ba	tents o the le WRE ack in r	f regi eft. If G. If regist regi	ster ' d' is d' is er 'f'. ster f	f' are 0 the 1 the f	rotated result is result is
Word	ds:	1						
Cycl	es:	1						
QC	cle Activity:							
	Q1	-	Q2		Q3			Q4
	Decode	F reg	Read jister 'f'	E	xecut	e	W des	rite to tination
<u>Exar</u>	<u>mple</u> :	R	LNCF		REG	, 1		
	Before Instru	ictior	ו					
	C REG	= =	0 1110	1011				
	After Instruct C	tion =						
	REG	=	1101	0111				

RRCF		Rotate	Right	f throug	gh Ca	arry
Syntax:		[label]	RRC	CF f,d		
Operand	ds:	0 ≤ f ≤ 2 d ∈ [0,1	55]			
Operatio	on:	$f < n > \rightarrow$ $f < 0 > \rightarrow$ $C \rightarrow d < 2$	d <n-1: C; 7></n-1: 	>;		
Status A	Affected:	С				
Encodin	g:	0001	100	d ff	ff	ffff
Descript	tion:	The cont one bit to Flag. If 'd WREG. I back in re	ents of the rig ' is 0 th f 'd' is 1 egister	register ' ht throug e result i the resu 'f'. register	f' are ih the s plac ilt is p f	rotated e Carry ced in blaced
\A/= = -l= -						
vvoras:		1				
Cycles:	A	1				
Q Cycle	Activity:	00		00		04
	Decode	Read register 'f	E	xecute	V de:	Vrite to stination
Example	<u>ə</u> :	RRCF		REG1	,0	
Bef	ore Instru	iction				
	REG1 C	= 1110 = 0	0110			
Afte	er Instruct REG1 WREG C	tion = 1110 = 0111 = 0	0110 0011			

17.0 PIC17C42 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias	55 to +125°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	0 to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0.6V to +14V
Voltage on RA2 and RA3 with respect to Vss	-0.6V to +12V
Voltage on all other pins with respect to Vss	0.6V to VDD + 0.6V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin(s) - Total	250 mA
Maximum current into VDD pin(s) - Total	200 mA
Input clamp current, lik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	±20 mA
Maximum output current sunk by any I/O pin (except RA2 and RA3)	35 mA
Maximum output current sunk by RA2 or RA3 pins	60 mA
Maximum output current sourced by any I/O pin	20 mA
Maximum current sunk by PORTA and PORTB (combined)	150 mA
Maximum current sourced by PORTA and PORTB (combined)	100 mA
Maximum current sunk by PORTC, PORTD and PORTE (combined)	150 mA
Maximum current sourced by PORTC, PORTD and PORTE (combined)	100 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD-VOH)) x IOH} + Σ (VOL x IOL)

Note 2: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 17-3: CLKOUT AND I/O TIMING



TABLE 17-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓		15‡	30 ‡	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑	—	15‡	30 ‡	ns	Note 1
12	TckR	CLKOUT rise time	—	5‡	15 ‡	ns	Note 1
13	TckF	CLKOUT fall time	—	5‡	15 ‡	ns	Note 1
14	TckH2ioV	CLKOUT [↑] to Port out valid	—	_	0.5TCY + 20‡	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT	0.25Tcy + 25 ‡	_	_	ns	Note 1
16	TckH2iol	Port in hold after CLKOUT	0 ‡	_	_	ns	Note 1
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid	—	_	100 ‡	ns	
20	TioR	Port output rise time	—	10‡	35 ‡	ns	
21	TioF	Port output fall time	—	10‡	35 ‡	ns	
22	TinHL	INT pin high or low time	25 *	—	—	ns	
23	TrbHL	RB7:RB0 change INT high or low time	25 *	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Measurements are taken in EC Mode where OSC2 output = 4 x Tosc = Tcy.

FIGURE 18-13: WDT TIMER TIME-OUT PERIOD vs. VDD



FIGURE 18-14: IOH vs. VOH, VDD = 3V



19.2 **DC CHARACTERISTICS:**

PIC17LC42A/43/LC44 (Commercial, Industrial) PIC17LCR42/43 (Commercial, Industrial)

DC CHARA Parameter No.	CTERIS	STICS	Operating Min	g tempe	erature Max	-40°C 0°C Units	\leq TA \leq +85°C for industrial and \leq TA \leq +70°C for commercial Conditions
D001	VDD	Supply Voltage	2.5	-	6.0	V	
D002	VDR	RAM Data Retention Voltage (Note 1)	1.5 *	-	_	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	_	Vss	_	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.060 *	_	_	mV/ms	See section on Power-on Reset for details
D010 D011 D014	IDD	Supply Current (Note 2)	_ _ _	3 6 95	6 12 * 150	mA mA μA	Fosc = 4 MHz (Note 4) Fosc = 8 MHz Fosc = 32 kHz, WDT disabled (EC osc configuration)
D020 D021	IPD	Power-down Current (Note 3)	_	10 < 1	40 5	μΑ μΑ	VDD = 5.5V, WDT enabled VDD = 5.5V, WDT disabled

These parameters are characterized but not tested.

+ Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD or VSS, TOCKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

Current consumed from the oscillator and I/O's driving external capacitive or resistive loads needs to be considered.

For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as: VbD / (2 • R). For capacitive loads, the current can be estimated (for an individual I/O pin) as (CL • VDD) • f

CL = Total capacitive load on the I/O pin; f = average frequency the I/O pin switches.

The capacitive currents are most significant when the device is configured for external execution (includes extended microcontroller mode).

- 3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

Standard Operating Conditions (unloss otherwise stated)



TABLE 19-11: MEMORY INTERFACE WRITE REQUIREMENTS (NOT SUPPORTED IN PIC17LC4X DEVICES)

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
150	TadV2alL	AD<15:0> (address) valid to ALE↓ (address setup time)	0.25Tcy - 10	_	_	ns	
151	TalL2adl	ALE↓ to address out invalid (address hold time)	0	_	_	ns	
152	TadV2wrL	Data out valid to $\overline{WR} \downarrow$ (data setup time)	0.25Tcy - 40	—	_	ns	
153	TwrH2adl	WR [↑] to data out invalid (data hold time)	_	0.25Tcy §	_	ns	
154	TwrL	WR pulse width	—	0.25TCY §		ns	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.



TABLE 19-12: MEMORY INTERFACE READ REQUIREMENTS (NOT SUPPORTED IN PIC17LC4X DEVICES)

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
150	TadV2alL	AD15:AD0 (address) valid to ALE↓ (address setup time)	0.25Tcy - 10	_	ľ	ns	
151	TalL2adl	ALE↓ to address out invalid (address hold time)	5*		_	ns	
160	TadZ2oeL	AD15:AD0 hi-impedance to $\overline{OE}\downarrow$	0*	—	_	ns	
161	ToeH2adD	OE↑ to AD15:AD0 driven	0.25Tcy - 15	_	_	ns	
162	TadV2oeH	Data in valid before OE↑ (data setup time)	35	—	—	ns	
163	ToeH2adI	OE↑to data in invalid (data hold time)	0	_	_	ns	
164	TalH	ALE pulse width	—	0.25Tcy §	_	ns	
165	ToeL	OE pulse width	0.5Tcy - 35 §	—	_	ns	
166	TalH2alH	ALE↑ to ALE↑(cycle time)	—	TCY §	_	ns	
167	Тасс	Address access time	—	—	0.75Tcy - 30	ns	
168	Тое	Output enable access time (OE low to Data Valid)	_	_	0.5Tcy - 45	ns	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

*

NOTES:

PIC17C4X











21 5	44-Lead Plastic Surface Mount ((TOFP 10x10 mm Body	(10/010 mm Lead Form)
Z 1.J	H-Leau I lastic Suilace Mount		

Package Group: Plastic TQFP							
		Millimeters			Inches		
Symbol	Min	Мах	Notes	Min	Мах	Notes	
A	1.00	1.20		0.039	0.047		
A1	0.05	0.15		0.002	0.006		
A2	0.95	1.05		0.037	0.041		
D	11.75	12.25		0.463	0.482		
D1	9.90	10.10		0.390	0.398		
E	11.75	12.25		0.463	0.482		
E1	9.90	10.10		0.390	0.398		
L	0.45	0.75		0.018	0.030		
е	0.80	BSC		0.031	BSC		
b	0.30	0.45		0.012	0.018		
b1	0.30	0.40		0.012	0.016		
С	0.09	0.20		0.004	0.008		
c1	0.09	0.16		0.004	0.006		
N	44	44		44	44		
Θ	0°	7 °		0°	7 °		

Note 1: Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25m/m (0.010") per side. D1 and E1 dimensions including mold mismatch.

2: Dimension "b" does not include Dambar protrusion, allowable Dambar protrusion shall be 0.08m/m (0.003")max.

3: This outline conforms to JEDEC MS-026.

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