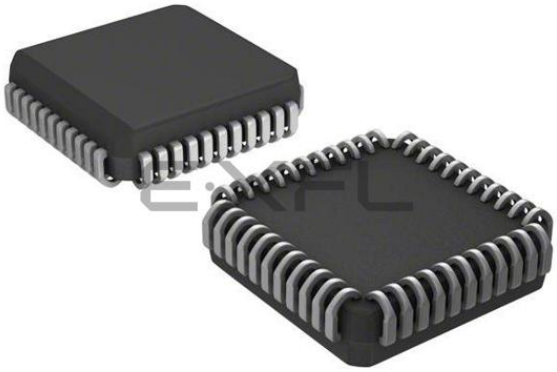

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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 8KB (4K x 16) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 454 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic17c43-16e-l |

**TABLE 1-1: PIC17CXX FAMILY OF DEVICES**

| Features | | PIC17C42 | PIC17CR42 | PIC17C42A | PIC17C43 | PIC17CR43 | PIC17C44 |
|---|---|---|---|---|---|---|---|
| Maximum Frequency of Operation | | 25 MHz | 33 MHz | 33 MHz | 33 MHz | 33 MHz | 33 MHz |
| Operating Voltage Range | | 4.5 - 5.5V | 2.5 - 6.0V | 2.5 - 6.0V | 2.5 - 6.0V | 2.5 - 6.0V | 2.5 - 6.0V |
| Program Memory x16 | (EPROM) | 2K | - | 2K | 4K | - | 8K |
| | (ROM) | - | 2K | - | - | 4K | - |
| Data Memory (bytes) | | 232 | 232 | 232 | 454 | 454 | 454 |
| Hardware Multiplier (8 x 8) | | - | Yes | Yes | Yes | Yes | Yes |
| Timer0 (16-bit + 8-bit postscaler) | | Yes | Yes | Yes | Yes | Yes | Yes |
| Timer1 (8-bit) | | Yes | Yes | Yes | Yes | Yes | Yes |
| Timer2 (8-bit) | | Yes | Yes | Yes | Yes | Yes | Yes |
| Timer3 (16-bit) | | Yes | Yes | Yes | Yes | Yes | Yes |
| Capture inputs (16-bit) | | 2 | 2 | 2 | 2 | 2 | 2 |
| PWM outputs (up to 10-bit) | | 2 | 2 | 2 | 2 | 2 | 2 |
| USART/SCI | | Yes | Yes | Yes | Yes | Yes | Yes |
| Power-on Reset | | Yes | Yes | Yes | Yes | Yes | Yes |
| Watchdog Timer | | Yes | Yes | Yes | Yes | Yes | Yes |
| External Interrupts | | Yes | Yes | Yes | Yes | Yes | Yes |
| Interrupt Sources | | 11 | 11 | 11 | 11 | 11 | 11 |
| Program Memory Code Protect | | Yes | Yes | Yes | Yes | Yes | Yes |
| I/O Pins | | 33 | 33 | 33 | 33 | 33 | 33 |
| I/O High Current Capability | Source | 25 mA | 25 mA | 25 mA | 25 mA | 25 mA | 25 mA |
| | Sink | 25 mA(1) | 25 mA(1) | 25 mA(1) | 25 mA(1) | 25 mA(1) | 25 mA(1) |
| Package Types | | 40-pin DIP<br>44-pin PLCC<br>44-pin MQFP | 40-pin DIP<br>44-pin PLCC<br>44-pin MQFP<br>44-pin TQFP | 40-pin DIP<br>44-pin PLCC<br>44-pin MQFP<br>44-pin TQFP | 40-pin DIP<br>44-pin PLCC<br>44-pin MQFP<br>44-pin TQFP | 40-pin DIP<br>44-pin PLCC<br>44-pin MQFP<br>44-pin TQFP | 40-pin DIP<br>44-pin PLCC<br>44-pin MQFP<br>44-pin TQFP |

Note 1: Pins RA2 and RA3 can sink up to 60 mA.


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## 2.0 PIC17C4X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC17C4X Product Selection System section at the end of this data sheet. When placing orders, please use the "PIC17C4X Product Identification System" at the back of this data sheet to specify the correct part number.

For the PIC17C4X family of devices, there are four device "types" as indicated in the device number:

1. **C**, as in PIC17**C**42. These devices have EPROM type memory and operate over the standard voltage range.
2. **LC**, as in PIC17**LC**42. These devices have EPROM type memory, operate over an extended voltage range, and reduced frequency range.
3. **CR**, as in PIC17**CR**42. These devices have ROM type memory and operate over the standard voltage range.
4. **LCR**, as in PIC17**LCR**42. These devices have ROM type memory, operate over an extended voltage range, and reduced frequency range.

### 2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package, is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the configuration modes. Microchip's PRO MATE™ programmer supports programming of the PIC17C4X. Third party programmers also are available; refer to the *Third Party Guide* for a list of sources.

### 2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

### 2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

### 2.4 Serialized Quick-Turnaround Production (SQTP$^{SM}$) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

ROM devices do not allow serialization information in the program memory space.

For information on submitting ROM code, please contact your regional sales office.

### 2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, thus giving customers a low cost option for high volume, mature products.

For information on submitting ROM code, please contact your regional sales office.

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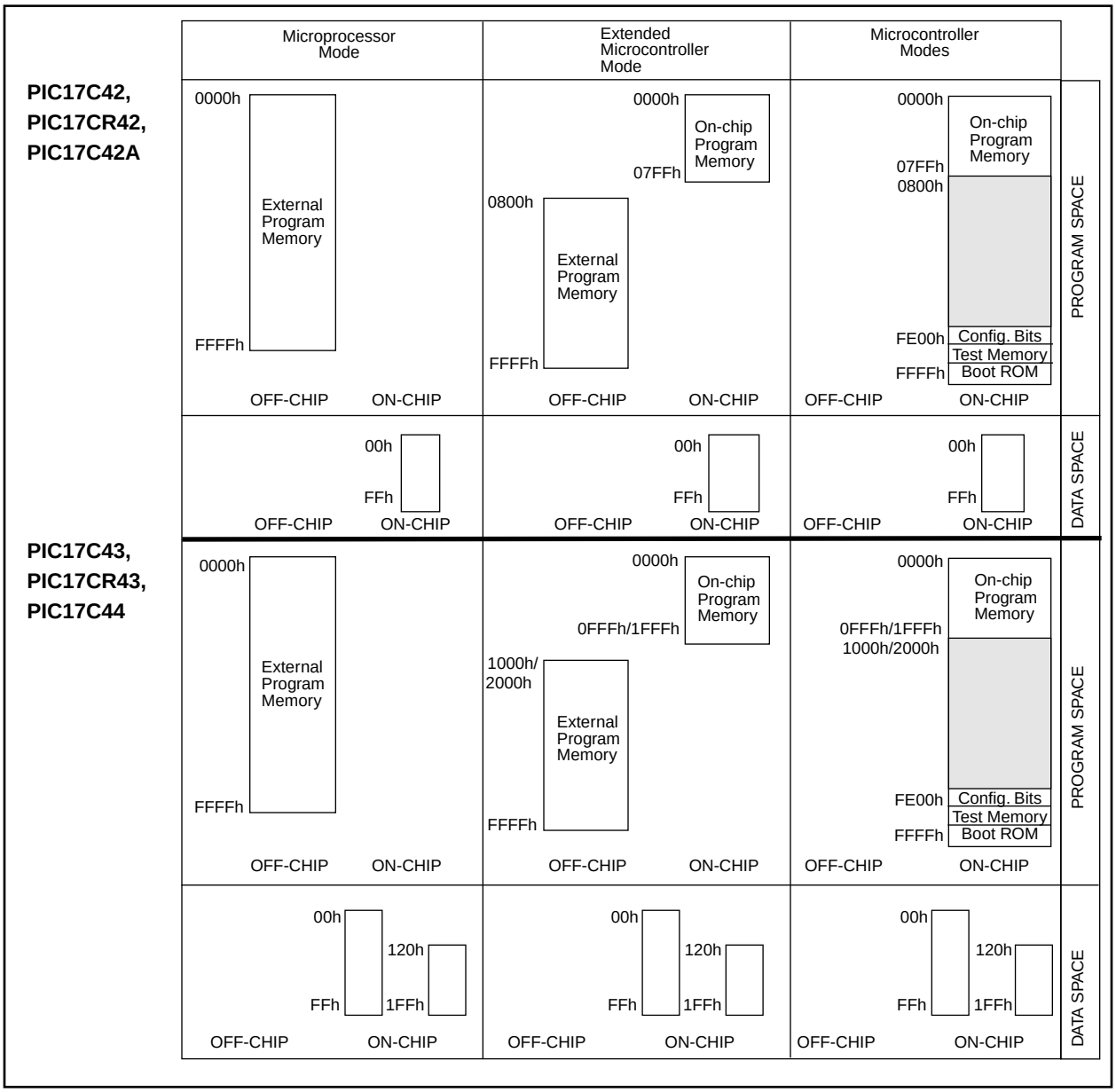
**TABLE 6-1: MODE MEMORY ACCESS**

| Operating Mode | Internal Program Memory | Configuration Bits, Test Memory, Boot ROM |
|---|---|---|
| Microprocessor | No Access | No Access |
| Microcontroller | Access | Access |
| Extended Microcontroller | Access | No Access |
| Protected Microcontroller | Access | Access |

The PIC17C4X can operate in modes where the program memory is off-chip. They are the microprocessor and extended microcontroller modes. The microprocessor mode is the default for an unprogrammed device.

Regardless of the processor mode, data memory is always on-chip.

**FIGURE 6-2: MEMORY MAP IN DIFFERENT MODES**





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### 6.4.1 INDIRECT ADDRESSING REGISTERS

The PIC17C4X has four registers for indirect addressing. These registers are:

- INDF0 and FSR0
- INDF1 and FSR1

Registers INDF0 and INDF1 are not physically implemented. Reading or writing to these registers activates indirect addressing, with the value in the corresponding FSR register being the address of the data. The FSR is an 8-bit register and allows addressing anywhere in the 256-byte data memory address range. For banked memory, the bank of memory accessed is specified by the value in the BSR.

If file INDF0 (or INDF1) itself is read indirectly via an FSR, all '0's are read (Zero bit is set). Similarly, if INDF0 (or INDF1) is written to indirectly, the operation will be equivalent to a NOP, and the status bits are not affected.

### 6.4.2 INDIRECT ADDRESSING OPERATION

The indirect addressing capability has been enhanced over that of the PIC16CXX family. There are two control bits associated with each FSR register. These two bits configure the FSR register to:

- Auto-decrement the value (address) in the FSR after an indirect access
- Auto-increment the value (address) in the FSR after an indirect access
- No change to the value (address) in the FSR after an indirect access

These control bits are located in the ALUSTA register. The FSR1 register is controlled by the FS3:FS2 bits and FSR0 is controlled by the FS1:FS0 bits.

When using the auto-increment or auto-decrement features, the effect on the FSR is not reflected in the ALUSTA register. For example, if the indirect address causes the FSR to equal '0', the Z bit will not be set.

If the FSR register contains a value of 0h, an indirect read will read 0h (Zero bit is set) while an indirect write will be equivalent to a NOP (status bits are not affected).

Indirect addressing allows single cycle data transfers within the entire data space. This is possible with the use of the MOVPF and MOVFP instructions, where either 'p' or 'f' is specified as INDF0 (or INDF1).

If the source or destination of the indirect address is in banked memory, the location accessed will be determined by the value in the BSR.

A simple program to clear RAM from 20h - FFh is shown in Example 6-1.

**EXAMPLE 6-1: INDIRECT ADDRESSING**

```
    MOVLW    0x20          ;
    MOVWF    FSR0          ; FSR0 = 20h
    BCF      ALUSTA, FS1   ; Increment FSR
    BSF      ALUSTA, FS0   ; after access
    BCF      ALUSTA, C     ; C = 0
    MOVLW    END_RAM + 1   ;
LP  CLRF     INDF0         ; Addr(FSR) = 0
    CPFSEQ   FSR0          ; FSR0 = END_RAM+1?
    GOTO     LP            ; NO, clear next
    :                      ; YES, All RAM is
    :                      ; cleared
```

## 6.5 Table Pointer (TBLPTRL and TBLPTRH)

File registers TBLPTRL and TBLPTRH form a 16-bit pointer to address the 64K program memory space. The table pointer is used by instructions TABLWT and TABLRD.

The TABLRD and the TABLWT instructions allow transfer of data between program and data space. The table pointer serves as the 16-bit address of the data word within the program memory. For a more complete description of these registers and the operation of Table Reads and Table Writes, see Section 7.0.

## 6.6 Table Latch (TBLATH, TBLATL)

The table latch (TBLAT) is a 16-bit register, with TBLATH and TBLATL referring to the high and low bytes of the register. It is not mapped into data or program memory. The table latch is used as a temporary holding latch during data transfer between program and data memory (see descriptions of instructions TABLRD, TABLWT, TLRD and TLWT). For a more complete description of these registers and the operation of Table Reads and Table Writes, see Section 7.0.


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Example 8-3 shows the sequence to do a 16 x 16 unsigned multiply. Equation 8-1 shows the algorithm that is used. The 32-bit result is stored in 4 registers RES3:RES0.

**EQUATION 8-1: 16 x 16 UNSIGNED MULTIPLICATION ALGORITHM**

$$
\begin{aligned}
RES3:RES0 &= ARG1H:ARG1L * ARG2H:ARG2L \\
&= (ARG1H * ARG2H * 2^{16}) + \\
&\quad (ARG1H * ARG2L * 2^{8}) + \\
&\quad (ARG1L * ARG2H * 2^{8}) + \\
&\quad (ARG1L * ARG2L)
\end{aligned}
$$

**EXAMPLE 8-3: 16 x 16 MULTIPLY ROUTINE**

```
   MOVFP    ARG1L, WREG
   MULWF    ARG2L       ; ARG1L * ARG2L ->
                        ;   PRODH:PRODL
   MOVPF    PRODH, RES1 ;
   MOVPF    PRODL, RES0 ;
;
   MOVFP    ARG1H, WREG
   MULWF    ARG2H       ; ARG1H * ARG2H ->
                        ;   PRODH:PRODL
   MOVPF    PRODH, RES3 ;
   MOVPF    PRODL, RES2 ;
;
   MOVFP    ARG1L, WREG
   MULWF    ARG2H       ; ARG1L * ARG2H ->
                        ;   PRODH:PRODL
   MOVFP    PRODL, WREG ;
   ADDWF    RES1, F     ; Add cross
   MOVFP    PRODH, WREG ;    products
   ADDWFC   RES2, F     ;
   CLRF     WREG, F     ;
   ADDWFC   RES3, F     ;
;
   MOVFP    ARG1H, WREG ;
   MULWF    ARG2L       ; ARG1H * ARG2L ->
                        ;   PRODH:PRODL

   MOVFP    PRODL, WREG ;
   ADDWF    RES1, F     ; Add cross
   MOVFP    PRODH, WREG ;    products
   ADDWFC   RES2, F     ;
   CLRF     WREG, F     ;
   ADDWFC   RES3, F     ;
```


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### 9.4.1 PORTE AND DDRE REGISTER

PORTE is a 3-bit bi-directional port. The corresponding data direction register is DDRE. A '1' in DDRE configures the corresponding port pin as an input. A '0' in the DDRE register configures the corresponding port pin as an output. Reading PORTE reads the status of the pins, whereas writing to it will write to the port latch. PORTE is multiplexed with the system bus. When operating as the system bus, PORTE contains the control signals for the address/data bus (AD15:AD0). These control signals are Address Latch Enable (ALE), Output Enable ($\overline{OE}$), and Write ($\overline{WR}$). The control signals $\overline{OE}$ and $\overline{WR}$ are active low signals. The timing for the system bus is shown in the Electrical Characteristics section.

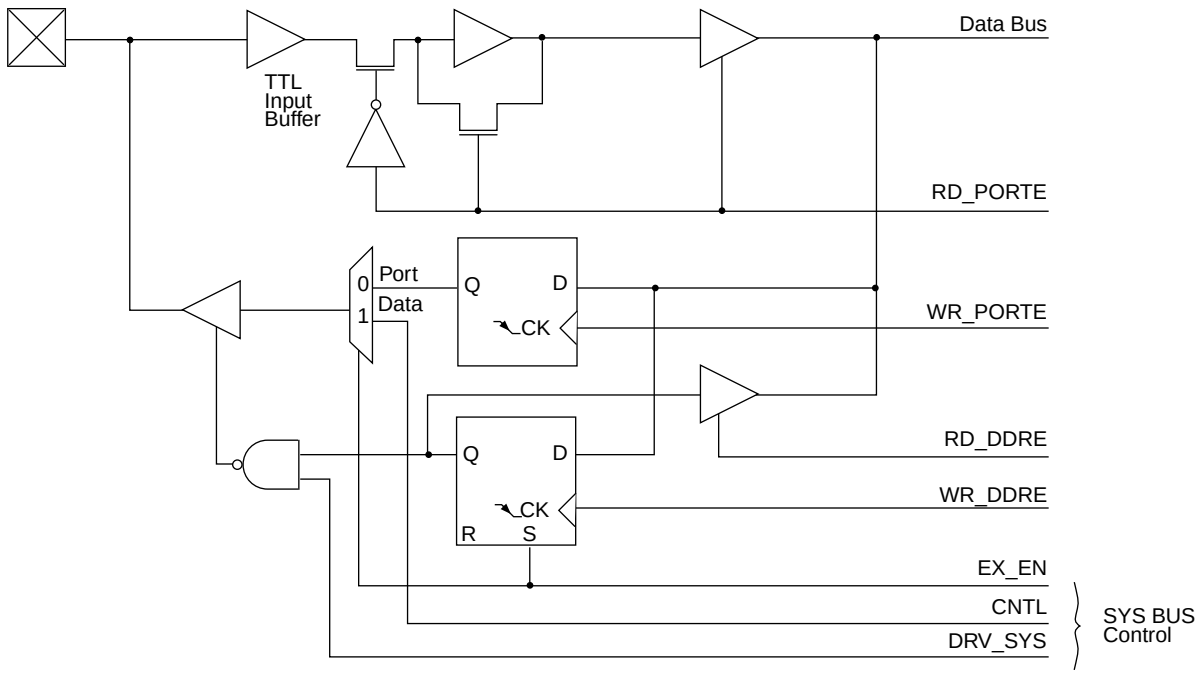
| **Note:** | This port is configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O. |
|---|---|

Example 9-4 shows the instruction sequence to initialize PORTE. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

**EXAMPLE 9-4: INITIALIZING PORTE**

```
MOVLB  1          ;  Select Bank 1
CLRF   PORTE      ;  Initialize PORTE data
                  ;   latches before setting
                  ;   the data direction
                  ;   register
MOVLW  0x03       ;  Value used to initialize
                  ;   data direction
MOVWF  DDRE       ;  Set RE<1:0> as inputs
                  ;   RE<2> as outputs
                  ;   RE<7:3> are always
                  ;   read as '0'
```

**FIGURE 9-8: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)**




Note: I/O pins have protection diodes to VDD and Vss.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## 11.0 TIMER0

The Timer0 module consists of a 16-bit timer/counter, TMR0. The high byte is TMR0H and the low byte is TMR0L. A software programmable 8-bit prescaler makes an effective 24-bit overflow timer. The clock source is also software programmable as either the internal instruction clock or the RA1/T0CKI pin. The control bits for this module are in register T0STA (Figure 11-1).

**FIGURE 11-1: T0STA REGISTER (ADDRESS: 05h, UNBANKED)**

| R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | U - 0 |
|---|---|---|---|---|---|---|---|
| INTEDG | T0SE | T0CS | PS3 | PS2 | PS1 | PS0 | — |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented, Read as '0'
-n = Value at POR reset

bit 7: **INTEDG**: RA0/INT Pin Interrupt Edge Select bit
This bit selects the edge upon which the interrupt is detected
1 = Rising edge of RA0/INT pin generates interrupt
0 = Falling edge of RA0/INT pin generates interrupt

bit 6: **T0SE**: Timer0 Clock Input Edge Select bit
This bit selects the edge upon which TMR0 will increment
When T0CS = 0
1 = Rising edge of RA1/T0CKI pin increments TMR0 and/or generates a T0CKIF interrupt
0 = Falling edge of RA1/T0CKI pin increments TMR0 and/or generates a T0CKIF interrupt
When T0CS = 1
Don't care

bit 5: **T0CS**: Timer0 Clock Source Select bit
This bit selects the clock source for TMR0.
1 = Internal instruction clock cycle ($T_{CY}$)
0 = T0CKI pin

bit 4-1: **PS3:PS0**: Timer0 Prescale Selection bits
These bits select the prescale value for TMR0.

| PS3:PS0 | Prescale Value |
|---|---|
| 0000 | 1:1 |
| 0001 | 1:2 |
| 0010 | 1:4 |
| 0011 | 1:8 |
| 0100 | 1:16 |
| 0101 | 1:32 |
| 0110 | 1:64 |
| 0111 | 1:128 |
| 1xxx | 1:256 |

bit 0: **Unimplemented**: Read as '0'

## 12.0 TIMER1, TIMER2, TIMER3, PWMS AND CAPTURES

The PIC17C4X has a wealth of timers and time-based functions to ease the implementation of control applications. These time-base functions include two PWM outputs and two Capture inputs.

Timer1 and Timer2 are two 8-bit incrementing timers, each with a period register (PR1 and PR2 respectively) and separate overflow interrupt flags. Timer1 and Timer2 can operate either as timers (increment on internal Fosc/4 clock) or as counters (increment on falling edge of external clock on pin RB4/TCLK12). They are also software configurable to operate as a single 16-bit timer. These timers are also used as the time-base for the PWM (pulse width modulation) module.

Timer3 is a 16-bit timer/counter consisting of the TMR3H and TMR3L registers. This timer has four other associated registers. Two registers are used as a 16-bit period register or a 16-bit Capture1 register (PR3H/CA1H:PR3L/CA1L). The other two registers are strictly the Capture2 registers (CA2H:CA2L). Timer3 is the time-base for the two 16-bit captures.

TMR3 can be software configured to increment from the internal system clock or from an external signal on the RB5/TCLK3 pin.

Figure 12-1 and Figure 12-2 are the control registers for the operation of Timer1, Timer2, and Timer3, as well as PWM1, PWM2, Capture1, and Capture2.

**FIGURE 12-1: TCON1 REGISTER (ADDRESS: 16h, BANK 3)**

| R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 | R/W - 0 |
|---|---|---|---|---|---|---|---|
| CA2ED1 | CA2ED0 | CA1ED1 | CA1ED0 | T16 | TMR3CS | TMR2CS | TMR1CS |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
-n = Value at POR reset

bit 7-6: **CA2ED1:CA2ED0**: Capture2 Mode Select bits
00 = Capture on every falling edge
01 = Capture on every rising edge
10 = Capture on every 4th rising edge
11 = Capture on every 16th rising edge

bit 5-4: **CA1ED1:CA1ED0**: Capture1 Mode Select bits
00 = Capture on every falling edge
01 = Capture on every rising edge
10 = Capture on every 4th rising edge
11 = Capture on every 16th rising edge

bit 3: **T16**: Timer1:Timer2 Mode Select bit
1 = Timer1 and Timer2 form a 16-bit timer
0 = Timer1 and Timer2 are two 8-bit timers

bit 2: **TMR3CS**: Timer3 Clock Source Select bit
1 = TMR3 increments off the falling edge of the RB5/TCLK3 pin
0 = TMR3 increments off the internal clock

bit 1: **TMR2CS**: Timer2 Clock Source Select bit
1 = TMR2 increments off the falling edge of the RB4/TCLK12 pin
0 = TMR2 increments off the internal clock

bit 0: **TMR1CS**: Timer1 Clock Source Select bit
1 = TMR1 increments off the falling edge of the RB4/TCLK12 pin
0 = TMR1 increments off the internal clock

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**FIGURE 13-3: USART TRANSMIT**

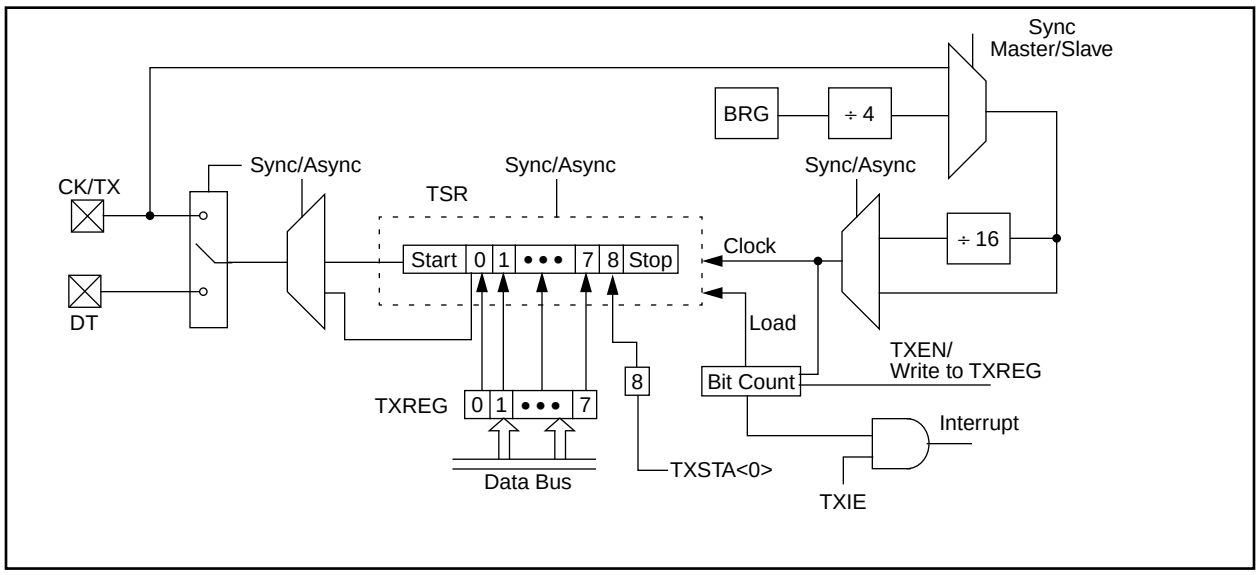
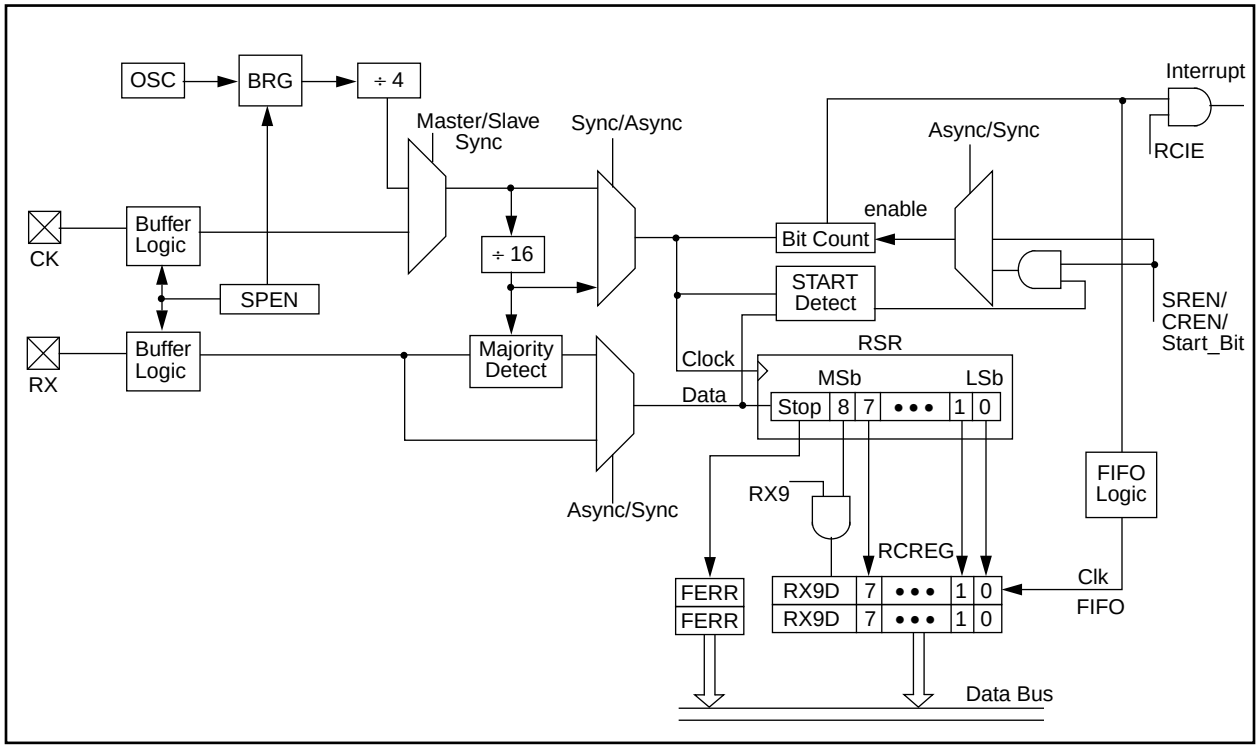



**FIGURE 13-4: USART RECEIVE**



## 14.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC17CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- OSC selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection

The PIC17CXX has a Watchdog Timer which can be shut off only through EPROM bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 96 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake from SLEEP through external reset, Watchdog Timer Reset or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LF crystal option saves power. Configuration bits are used to select various options. This configuration word has the format shown in Figure 14-1.

**FIGURE 14-1: CONFIGURATION WORD**

| R/P - 1 | U - x | U - x | U - x | U - x | U - x | U - x | U - x |
|---|---|---|---|---|---|---|---|
| PM2 (1) | — | — | — | — | — | — | — |
| bit15-7 | | | | | | | bit0 |

| U - x | R/P - 1 | U - x | R/P - 1 | R/P - 1 | R/P - 1 | R/P - 1 | R/P - 1 |
|---|---|---|---|---|---|---|---|
| — | PM1 | — | PM0 | WDTPS1 | WDTPS0 | FOSC1 | FOSC0 |
| bit15-7 | | | | | | | bit0 |

R = Readable bit
P = Programmable bit
U = Unimplemented
- n = Value for Erased Device
(x = unknown)

bit 15-9: **Unimplemented**: Read as a '1'

bit 15,6,4:**PM2, PM1, PM0**, Processor Mode Select bits
111 = Microprocessor Mode
110 = Microcontroller mode
101 = Extended microcontroller mode
000 = Code protected microcontroller mode

bit 7, 5: **Unimplemented**: Read as a '0'

bit 3-2: **WDTPS1:WDTPS0**, WDT Postscaler Select bits
11 = WDT enabled, postscaler = 1
10 = WDT enabled, postscaler = 256
01 = WDT enabled, postscaler = 64
00 = WDT disabled, 16-bit overflow timer

bit 1-0: **FOSC1:FOSC0**, Oscillator Select bits
11 = EC oscillator
10 = XT oscillator
01 = RC oscillator
00 = LF oscillator

Note 1: This bit does not exist on the PIC17C42. Reading this bit will return an unknown value (x).

## 15.0 INSTRUCTION SET SUMMARY

The PIC17CXX instruction set consists of 58 instructions. Each instruction is a 16-bit word divided into an OPCODE and one or more operands. The opcode specifies the instruction type, while the operand(s) further specify the operation of the instruction. The PIC17CXX instruction set can be grouped into three types:

- byte-oriented
- bit-oriented
- literal and control operations.

These formats are shown in Figure 15-1.

Table 15-1 shows the field descriptions for the opcodes. These descriptions are useful for understanding the opcodes in Table 15-2 and in each specific instruction descriptions.

**byte-oriented instructions**, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' = '0', the result is placed in the WREG register. If 'd' = '1', the result is placed in the file register specified by the instruction.

**bit-oriented instructions**, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

**literal and control operations**, 'k' represents an 8- or 11-bit constant or literal value.

The instruction set is highly orthogonal and is grouped into:

- byte-oriented operations
- bit-oriented operations
- literal and control operations

All instructions are executed within one single instruction cycle, unless:

- a conditional test is true
- the program counter is changed as a result of an instruction
- a table read or a table write instruction is executed (in this case, the execution takes two instruction cycles with the second cycle executed as a NOP)

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 25 MHz, the normal instruction execution time is 160 ns. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 320 ns.

**TABLE 15-1: OPCODE FIELD DESCRIPTIONS**

| Field | Description |
|---|---|
| f | Register file address (00h to FFh) |
| p | Peripheral register file address (00h to 1Fh) |
| i | Table pointer control i = '0' (do not change)<br>i = '1' (increment after instruction execution) |
| t | Table byte select t = '0' (perform operation on lower byte)<br>t = '1' (perform operation on upper byte literal field, constant data) |
| WREG | Working register (accumulator) |
| b | Bit address within an 8-bit file register |
| k | Literal field, constant data or label |
| x | Don't care location (= '0' or '1')<br>The assembler will generate code with x = '0'. It is the recommended form of use for compatibility with all Microchip software tools. |
| d | Destination select<br>0 = store result in WREG<br>1 = store result in file register f<br>Default is d = '1' |
| u | Unused, encoded as '0' |
| s | Destination select<br>0 = store result in file register f and in the WREG<br>1 = store result in file register f<br>Default is s = '1' |
| label | Label name |
| C,DC,Z,OV | ALU status bits Carry, Digit Carry, Zero, Overflow |
| GLINTD | Global Interrupt Disable bit (CPUSTA<4>) |
| TBLPTR | Table Pointer (16-bit) |
| TBLAT | Table Latch (16-bit) consists of high byte (TBLATH) and low byte (TBLATL) |
| TBLATL | Table Latch low byte |
| TBLATH | Table Latch high byte |
| TOS | Top of Stack |
| PC | Program Counter |
| BSR | Bank Select Register |
| WDT | Watchdog Timer Counter |
| $\overline{TO}$ | Time-out bit |
| $\overline{PD}$ | Power-down bit |
| dest | Destination either the WREG register or the specified register file location |
| [ ] | Options |
| ( ) | Contents |
| $\rightarrow$ | Assigned to |
| < > | Register bit field |
| $\in$ | In the set of |
| *italics* | User defined term (font is courier) |

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**BSF** **Bit Set f**

Syntax: [ *label* ] BSF f,b

Operands: $0 \le f \le 255$
$0 \le b \le 7$

Operation: $1 \rightarrow (f<b>)$

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 1000 | 0bbb | ffff | ffff |

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Execute | Write register 'f' |

Example:
```
BSF     FLAG_REG, 7
```
Before Instruction
FLAG_REG= 0x0A
After Instruction
FLAG_REG= 0x8A

**BTFSC** **Bit Test, skip if Clear**

Syntax: [ *label* ] BTFSC f,b

Operands: $0 \le f \le 255$
$0 \le b \le 7$

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 1001 | 1bbb | ffff | ffff |

Description: If bit 'b' in register 'f' is 0 then the next instruction is skipped.
If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Execute | NOP |

If skip:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Forced NOP | NOP | Execute | NOP |

Example:
```
HERE    BTFSC   FLAG,1
FALSE   :
TRUE    :
```
Before Instruction
PC = address (HERE)
After Instruction
If FLAG<1> = 0;
PC = address (TRUE)
If FLAG<1> = 1;
PC = address (FALSE)

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**MOVLR** **Move Literal to high nibble in BSR**

Syntax: [ *label* ] MOVLR k

Operands: $0 \le k \le 15$

Operation: k → (BSR<7:4>)

Status Affected: None

Encoding:

| 1011 | 101x | kkkk | uuuu |
|---|---|---|---|

Description: The 4-bit literal 'k' is loaded into the most significant 4-bits of the Bank Select Register (BSR). Only the high 4-bits of the Bank Select Register are affected. The lower half of the BSR is unchanged. The assembler will encode the “u” fields as 0.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read literal 'k:u' | Execute | Write literal 'k' to BSR<7:4> |

Example: MOVLR 5

Before Instruction
BSR register = 0x22

After Instruction
BSR register = 0x52

**Note:** This instruction is not available in the PIC17C42 device.

**MOVLW** **Move Literal to WREG**

Syntax: [ *label* ] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (WREG)

Status Affected: None

Encoding:

| 1011 | 0000 | kkkk | kkkk |
|---|---|---|---|

Description: The eight bit literal 'k' is loaded into WREG.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read literal 'k' | Execute | Write to WREG |

Example: MOVLW 0x5A

After Instruction
WREG = 0x5A

# 16.0 DEVELOPMENT SUPPORT

## 16.1 Development Tools

The PIC16/17 microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB-SIM Software Simulator
- MPLAB-C (C Compiler)
- Fuzzy logic development system (fuzzyTECH®–MP)

## 16.2 PICMASTER: High Performance Universal In-Circuit Emulator with MPLAB IDE

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX and PIC17CXX families. PICMASTER is supplied with the MPLAB™ Integrated Development Environment (IDE), which allows editing, “make” and download, and source debugging from a single environment.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new Microchip microcontrollers.

The PICMASTER Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x environment were chosen to best make these features available to you, the end user.

A CE compliant version of PICMASTER is available for European Union (EU) countries.

## 16.3 ICEPIC: Low-cost PIC16CXXX In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT® through Pentium™ based machines under Windows 3.x environment. ICEPIC features real time, non-intrusive emulation.

## 16.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode.

The PRO MATE II has programmable $V_{DD}$ and $V_{PP}$ supplies which allows it to verify programmed memory at $V_{DD}$ min and $V_{DD}$ max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC16C5X, PIC16CXXX, PIC17CXX and PIC14000 devices. It can also set configuration and code-protect bits in this mode.

## 16.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923 and PIC16C924 may be supported with an adapter socket.

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**TABLE 16-1: DEVELOPMENT TOOLS FROM MICROCHIP**

| Product | ** MPLAB™ Integrated Development Environment | MPLAB™ C Compiler | MP-DriveWay Applications Code Generator | fuzzyTECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool | *** PICMASTER® PICMASTER-CE In-Circuit Emulator | ICEPIC Low-Cost In-Circuit Emulator | ****PRO MATE™ II Universal Microchip Programmer | PICSTART® Lite Ultra Low-Cost Dev. Kit | PICSTART® Plus Low-Cost Universal Dev. Kit |
|---|---|---|---|---|---|---|---|---|---|
| PIC12C508, 509 | SW007002 | SW006005 | — | — | EM167015/ EM167101 | — | DV007003 | — | DV003001 |
| PIC14000 | SW007002 | SW006005 | — | — | EM147001/ EM147101 | — | DV007003 | — | DV003001 |
| PIC16C52, 54, 54A, 55, 56, 57, 58A | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM167015/ EM167101 | EM167201 | DV007003 | DV162003 | DV003001 |
| PIC16C554, 556, 558 | SW007002 | SW006005 | — | DV005001/ DV005002 | EM167033/ EM167113 | —- | DV007003 | — | DV003001 |
| PIC16C61 | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM167021/ N/A | EM167205 | DV007003 | DV162003 | DV003001 |
| PIC16C62, 62A, 64, 64A | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM167025/ EM167103 | EM167203 | DV007003 | DV162002 | DV003001 |
| PIC16C620, 621, 622 | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM167023/ EM167109 | EM167202 | DV007003 | DV162003 | DV003001 |
| PIC16C63, 65, 65A, 73, 73A, 74, 74A | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM167025/ EM167103 | EM167204 | DV007003 | DV162002 | DV003001 |
| PIC16C642, 662* | SW007002 | SW006005 | — | — | EM167035/ EM167105 | —- | DV007003 | DV162002 | DV003001 |
| PIC16C71 | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM167027/ EM167105 | EM167205 | DV007003 | DV162003 | DV003001 |
| PIC16C710, 711 | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM167027/ EM167105 | — | DV007003 | DV162003 | DV003001 |
| PIC16C72 | SW007002 | SW006005 | SW006006 | — | EM167025/ EM167103 | — | DV007003 | DV162002 | DV003001 |
| PIC16F83 | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM167029/ EM167107 | — | DV007003 | DV162003 | DV003001 |
| PIC16C84 | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM167029/ EM167107 | EM167206 | DV007003 | DV162003 | DV003001 |
| PIC16F84 | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM167029/ EM167107 | — | DV007003 | DV162003 | DV003001 |
| PIC16C923, 924* | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM167031/ EM167111 | — | DV007003 | — | DV003001 |
| PIC17C42, 42A, 43, 44 | SW007002 | SW006005 | SW006006 | DV005001/ DV005002 | EM177007/ EM177107 | — | DV007003 | — | DV003001 |

*Contact Microchip Technology for availability date
**MPLAB Integrated Development Environment includes MPLAB-SIM Simulator and MPASM Assembler

***All PICMASTER and PICMASTER-CE ordering part numbers above include PRO MATE II programmer
****PRO MATE socket modules are ordered separately. See development systems ordering guide for specific ordering part numbers

| Product | TRUEGAUGE® Development Kit | SEEVAL® Designers Kit | Hopping Code Security Programmer Kit | Hopping Code Security Eval/Demo Kit |
|---|---|---|---|---|
| All 2 wire and 3 wire Serial EEPROM's | N/A | DV243001 | N/A | N/A |
| MTA11200B | DV114001 | N/A | N/A | N/A |
| HCS200, 300, 301 * | N/A | N/A | PG306001 | DM303001 |


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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

## 17.2 DC CHARACTERISTICS: PIC17C42-16 (Commercial, Industrial) PIC17C42-25 (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature<br>-40°C ≤ TA ≤ +85°C for industrial and<br>0°C ≤ TA ≤ +70°C for commercial<br>Operating voltage VDD range as described in Section 17.1 | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter No.** | **Sym** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | | **Input Low Voltage** | | | | | |
| | VIL | I/O ports | | | | | |
| D030 | | with TTL buffer | VSS | – | 0.8 | V | |
| D031 | | with Schmitt Trigger buffer | VSS | – | 0.2VDD | V | |
| D032 | | $\overline{MCLR}$, OSC1 (in EC and RC mode) | Vss | – | 0.2VDD | V | Note1 |
| D033 | | OSC1 (in XT, and LF mode) | – | 0.5VDD | – | V | |
| | | **Input High Voltage** | | | | | |
| | VIH | I/O ports | | – | | | |
| D040 | | with TTL buffer | 2.0 | – | VDD | V | |
| D041 | | with Schmitt Trigger buffer | 0.8VDD | – | VDD | V | |
| D042 | | $\overline{MCLR}$ | 0.8VDD | – | VDD | V | Note1 |
| D043 | | OSC1 (XT, and LF mode) | – | 0.5VDD | – | V | |
| D050 | VHYS | Hysteresis of Schmitt Trigger inputs | 0.15VDD* | – | – | V | |
| | | **Input Leakage Current** (Notes 2, 3) | | | | | |
| D060 | IIL | I/O ports (except RA2, RA3) | – | – | ±1 | µA | Vss ≤ VPIN ≤ VDD, I/O Pin at hi-impedance PORTB weak pull-ups disabled |
| D061 | | $\overline{MCLR}$ | – | – | ±2 | µA | VPIN = Vss or VPIN = VDD |
| D062 | | RA2, RA3 | | | ±2 | µA | Vss ≤ VRA2, VRA3 ≤ 12V |
| D063 | | OSC1, TEST | – | – | ±1 | µA | Vss ≤ VPIN ≤ VDD |
| D064 | | $\overline{MCLR}$ | – | – | 10 | µA | VMCLR = VPP = 12V (when not programming) |
| D070 | IPURB | PORTB weak pull-up current | 60 | 200 | 400 | µA | VPIN = VSS, $\overline{RBPU}$ = 0 |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

†† Design guidance to attain the AC timing specifications. These loads are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17CXX Programming Specifications (Literature number DS30139).

5: The $\overline{MCLR}$/Vpp pin may be kept in this range at times other than programming, but this is not recommended.

6: For TTL buffers, the better of the two specifications may be used.


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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

**TABLE 19-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)**

| OSC | PIC17LCR42-08<br>PIC17LC42A-08<br>PIC17LC43-08<br>PIC17LCR43-08<br>PIC17LC44-08 | PIC17CR42-16<br>PIC17C42A-16<br>PIC17C43-16<br>PIC17CR43-16<br>PIC17C44-16 | PIC17CR42-25<br>PIC17C42A-25<br>PIC17C43-25<br>PIC17CR43-25<br>PIC17C44-25 | PIC17CR42-33<br>PIC17C42A-33<br>PIC17C43-33<br>PIC17CR43-33<br>PIC17C44-33 | JW Devices<br>(Ceramic Windowed Devices) |
|---|---|---|---|---|---|
| RC | VDD: 2.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. |
| XT | VDD: 2.5V to 6.0V<br>IDD: 12 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 8 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 24 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 16 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 25 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. |
| EC | VDD: 2.5V to 6.0V<br>IDD: 12 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 8 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 24 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 16 MHz Max | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 25 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. |
| LF | VDD: 2.5V to 6.0V<br>IDD: 150 µA max. at 32 kHz<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 95 µA typ. at 32 kHz<br>IPD: < 1 µA typ. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 95 µA typ. at 32 kHz<br>IPD: < 1 µA typ. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 95 µA typ. at 32 kHz<br>IPD: < 1 µA typ. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 2.5V to 6.0V<br>IDD: 150 µA max. at 32 kHz<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 2 MHz max. |

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.


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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

## 19.5 Timing Diagrams and Specifications

**FIGURE 19-2: EXTERNAL CLOCK TIMING**

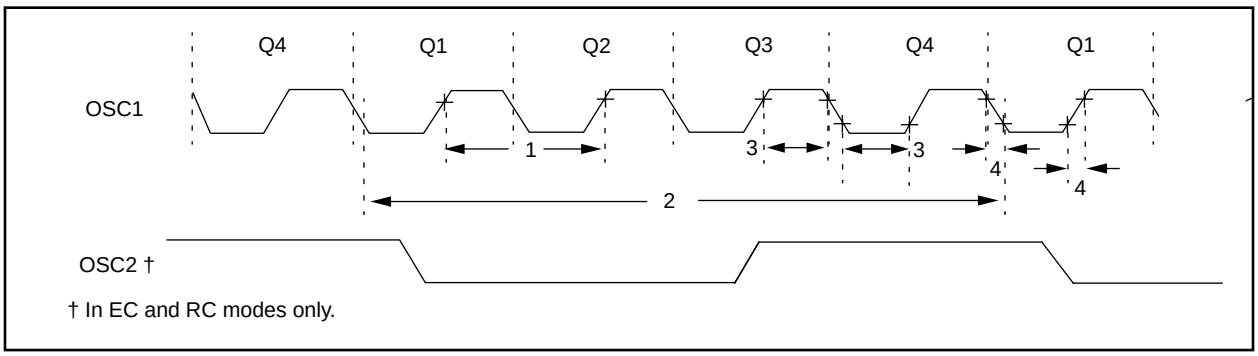


**TABLE 19-2: EXTERNAL CLOCK TIMING REQUIREMENTS**

| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | Fosc | **External CLKIN Frequency (Note 1)** | DC | — | 8 | MHz | EC osc mode - 08 devices (8 MHz devices) |
| | | | DC | — | 16 | MHz | - 16 devices (16 MHz devices) |
| | | | DC | — | 25 | MHz | - 25 devices (25 MHz devices) |
| | | | DC | — | 33 | MHz | - 33 devices (33 MHz devices) |
| | | **Oscillator Frequency (Note 1)** | DC | — | 4 | MHz | RC osc mode |
| | | | 1 | — | 8 | MHz | XT osc mode - 08 devices (8 MHz devices) |
| | | | 1 | — | 16 | MHz | - 16 devices (16 MHz devices) |
| | | | 1 | — | 25 | MHz | - 25 devices (25 MHz devices) |
| | | | 1 | — | 33 | MHz | - 33 devices (33 MHz devices) |
| | | | DC | — | 2 | MHz | LF osc mode |
| 1 | Tosc | **External CLKIN Period (Note 1)** | 125 | — | — | ns | EC osc mode - 08 devices (8 MHz devices) |
| | | | 62.5 | — | — | ns | - 16 devices (16 MHz devices) |
| | | | 40 | — | — | ns | - 25 devices (25 MHz devices) |
| | | | 30.3 | — | — | ns | - 33 devices (33 MHz devices) |
| | | **Oscillator Period (Note 1)** | 250 | — | — | ns | RC osc mode |
| | | | 125 | — | 1,000 | ns | XT osc mode - 08 devices (8 MHz devices) |
| | | | 62.5 | — | 1,000 | ns | - 16 devices (16 MHz devices) |
| | | | 40 | — | 1,000 | ns | - 25 devices (25 MHz devices) |
| | | | 30.3 | — | 1,000 | ns | - 33 devices (33 MHz devices) |
| | | | 500 | — | — | ns | LF osc mode |
| 2 | TCY | **Instruction Cycle Time (Note 1)** | 121.2 | 4/Fosc | DC | ns | |
| 3 | TosL, TosH | **Clock in (OSC1) high or low time** | 10 ‡ | — | — | ns | EC oscillator |
| 4 | TosR, TosF | **Clock in (OSC1) rise or fall time** | — | — | 5 ‡ | ns | EC oscillator |

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.


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| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

**FIGURE 19-9: USART MODULE: SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING**

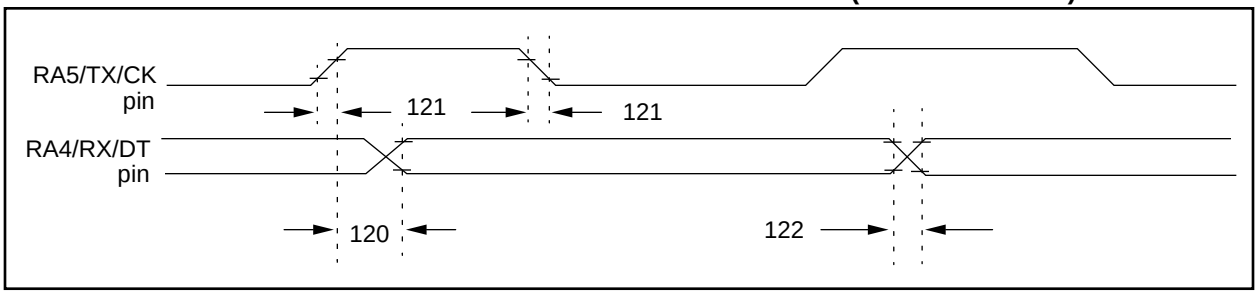


**TABLE 19-9: SYNCHRONOUS TRANSMISSION REQUIREMENTS**

| Param No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 120 | TckH2dtV | SYNC XMIT (MASTER & SLAVE) Clock high to data out valid | PIC17CR42/42A/43/R43/44 | — | — | 50 | ns | |
| | | | PIC17LCR42/42A/43/R43/44 | — | — | 75 | ns | |
| 121 | TckRF | Clock out rise time and fall time (Master Mode) | PIC17CR42/42A/43/R43/44 | — | — | 25 | ns | |
| | | | PIC17LCR42/42A/43/R43/44 | — | — | 40 | ns | |
| 122 | TdtRF | Data out rise time and fall time | PIC17CR42/42A/43/R43/44 | — | — | 25 | ns | |
| | | | PIC17LCR42/42A/43/R43/44 | — | — | 40 | ns | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 19-10: USART MODULE: SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING**

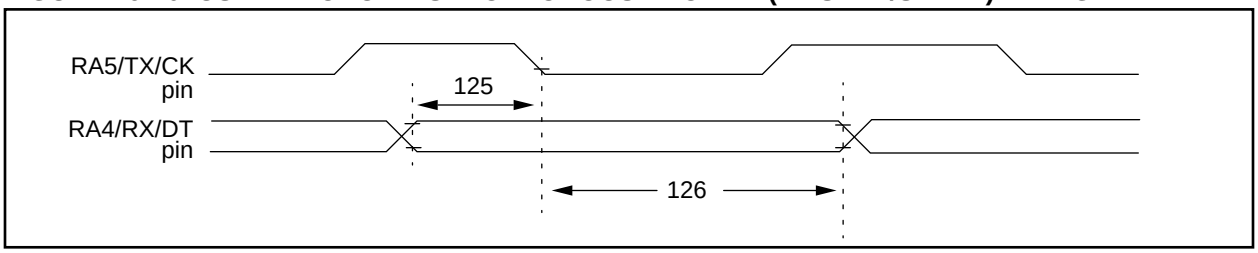


**TABLE 19-10: SYNCHRONOUS RECEIVE REQUIREMENTS**

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 125 | TdtV2ckL | SYNC RCV (MASTER & SLAVE) Data hold before CK↓ (DT hold time) | 15 | — | — | ns | |
| 126 | TckL2dtl | Data hold after CK↓ (DT hold time) | 15 | — | — | ns | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

**FIGURE 20-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**

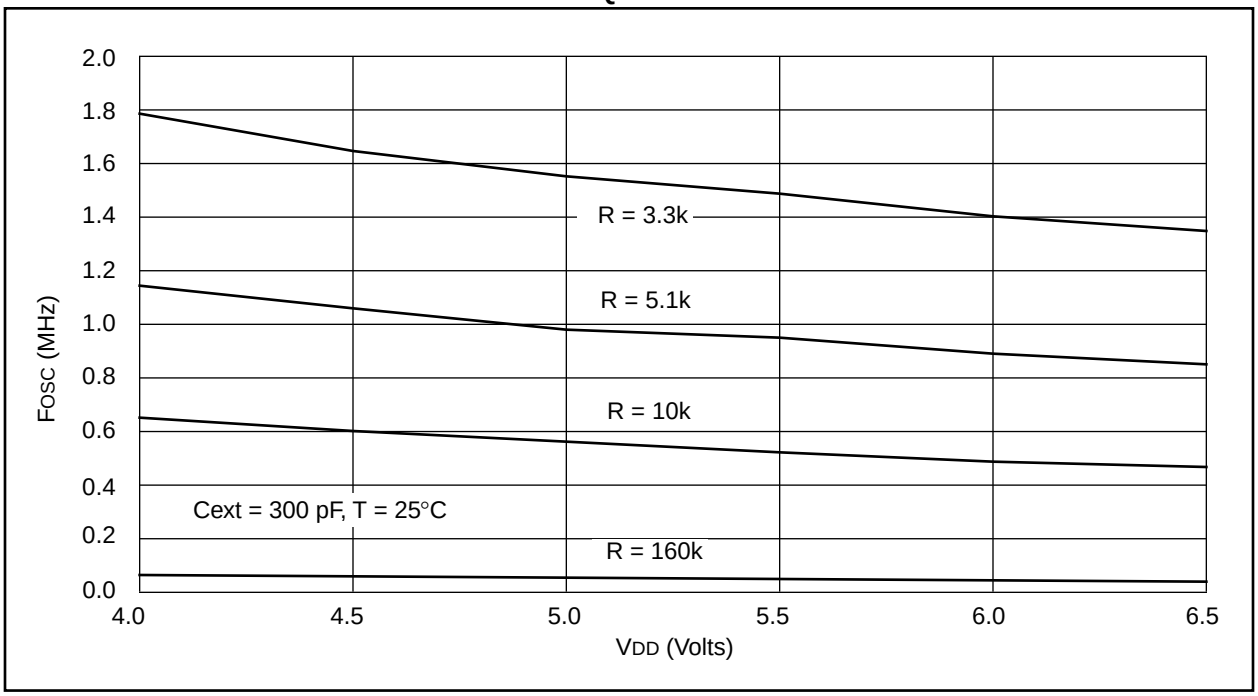


**TABLE 20-2: RC OSCILLATOR FREQUENCIES**

| Cext | Rext | Average Fosc @ 5V, 25°C | |
|---|---|---|---|
| 22 pF | 10k | 3.33 MHz | ± 12% |
| | 100k | 353 kHz | ± 13% |
| 100 pF | 3.3k | 3.54 MHz | ± 10% |
| | 5.1k | 2.43 MHz | ± 14% |
| | 10k | 1.30 MHz | ± 17% |
| | 100k | 129 kHz | ± 10% |
| 300 pF | 3.3k | 1.54 MHz | ± 14% |
| | 5.1k | 980 kHz | ± 12% |
| | 10k | 564 kHz | ± 16% |
| | 160k | 35 kHz | ± 18% |

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