# E·XFL



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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	33
Program Memory Size	8KB (4K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	454 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c43-25-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC17C4X can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC17C4X uses a modified Harvard architecture. This architecture has the program and data accessed from separate memories. So the device has a program memory bus and a data memory bus. This improves bandwidth over traditional von Neumann architecture, where program and data are fetched from the same memory (accesses over the same bus). Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. PIC17C4X opcodes are 16-bits wide, enabling single word instructions. The full 16-bit wide program memory bus fetches a 16-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions. Consequently, all instructions execute in a single cycle (121 ns @ 33 MHz), except for program branches and two special instructions that transfer data between program and data memory.

The PIC17C4X can address up to 64K x 16 of program memory space.

The **PIC17C42** and **PIC17C42A** integrate 2K x 16 of EPROM program memory on-chip, while the **PIC17CR42** has 2K x 16 of ROM program memory on-chip.

The **PIC17C43** integrates 4K x 16 of EPROM program memory, while the **PIC17CR43** has 4K x 16 of ROM program memory.

The **PIC17C44** integrates 8K x 16 EPROM program memory.

Program execution can be internal only (microcontroller or protected microcontroller mode), external only (microprocessor mode) or both (extended microcontroller mode). Extended microcontroller mode does not allow code protection.

The PIC17CXX can directly or indirectly address its register files or data memory. All special function registers, including the Program Counter (PC) and Working Register (WREG), are mapped in the data memory. The PIC17CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC17CXX simple yet efficient. In addition, the learning curve is reduced significantly.

One of the PIC17CXX family architectural enhancements from the PIC16CXX family allows two file registers to be used in some two operand instructions. This allows data to be moved directly between two registers without going through the WREG register. This increases performance and decreases program memory usage. The PIC17CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift, and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature.

The WREG register is an 8-bit working register used for ALU operations.

All PIC17C4X devices (except the PIC17C42) have an 8 x 8 hardware multiplier. This multiplier generates a 16-bit result in a single cycle.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

Although the ALU does not perform signed arithmetic, the Overflow bit (OV) can be used to implement signed math. Signed arithmetic is comprised of a magnitude and a sign bit. The overflow bit indicates if the magnitude overflows and causes the sign bit to change state. Signed math can have greater than 7-bit values (magnitude), if more than one byte is used. The use of the overflow bit only operates on bit6 (MSb of magnitude) and bit7 (sign bit) of the value in the ALU. That is, the overflow bit is not useful if trying to implement signed math where the magnitude, for example, is 11-bits. If the signed math values are greater than 7-bits (15-, 24or 31-bit), the algorithm must ensure that the low order bytes ignore the overflow status bit.

Care should be taken when adding and subtracting signed numbers to ensure that the correct operation is executed. Example 3-1 shows an item that must be taken into account when doing signed arithmetic on an ALU which operates as an unsigned machine.

#### EXAMPLE 3-1: SIGNED MATH

Hex Value	Signed Value Math	Unsigned Value Math
FFh	-127	255
<u>+ 01h</u>	<u>+ 1</u>	<u>+ 1</u>
= ?	= -126 (FEh)	= 0 (00h); Carry bit = 1
		curry pro - r

Signed math requires the result in REG to be FEh (-126). This would be accomplished by subtracting one as opposed to adding one.

Simplified block diagrams are shown in Figure 3-1 and Figure 3-2. The descriptions of the device pins are listed in Table 3-1.

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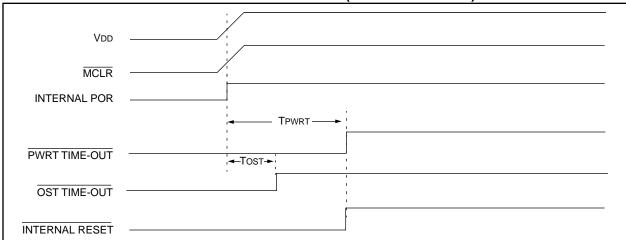
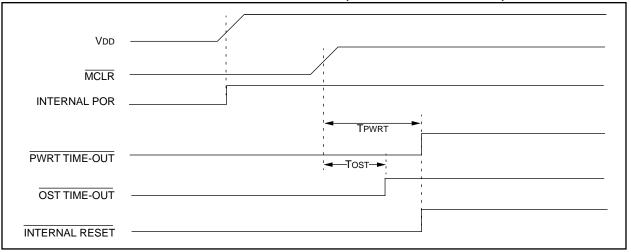
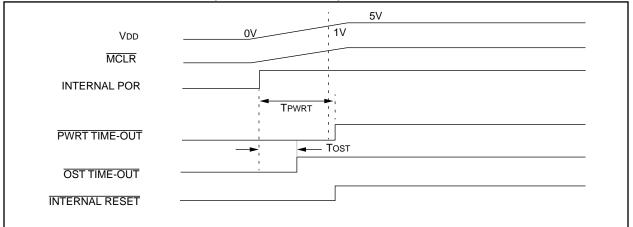


FIGURE 4-2: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

#### FIGURE 4-3: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD)



#### FIGURE 4-4: SLOW RISE TIME (MCLR TIED TO VDD)



Register	Address	Power-on Reset	MCLR Reset WDT Reset	Wake-up from SLEEP through interrupt
Unbanked	L		<u></u>	
INDF0	00h	0000 0000	0000 0000	0000 0000
FSR0	01h	XXXX XXXX	uuuu uuuu	นนนน นนนน
PCL	02h	0000h	0000h	PC + 1 <sup>(2)</sup>
PCLATH	03h	0000 0000	0000 0000	uuuu uuuu
ALUSTA	04h	1111 xxxx	1111 uuuu	1111 uuuu
TOSTA	05h	0000 000-	0000 000-	0000 000-
CPUSTA <sup>(3)</sup>	06h	11 11	11 qq	uu qq
INTSTA	07h	0000 0000	0000 0000	uuuu uuuu( <sup>1)</sup>
INDF1	08h	0000 0000	0000 0000	<u>uuuu</u> uuuu
FSR1	09h	XXXX XXXX	uuuu uuuu	uuuu uuuu
WREG	0Ah	XXXX XXXX	uuuu uuuu	uuuu uuuu
TMR0L	0Bh	XXXX XXXX	uuuu uuuu	uuuu uuuu
TMR0H	0Ch	XXXX XXXX	uuuu uuuu	uuuu uuuu
TBLPTRL <sup>(4)</sup>	0Dh	XXXX XXXX	uuuu uuuu	นนนน นนนน
TBLPTRH (4)	0Eh	XXXX XXXX	uuuu uuuu	uuuu uuuu
TBLPTRL (5)	0Dh	0000 0000	0000 0000	uuuu uuuu
TBLPTRH <sup>(5)</sup>	0Eh	0000 0000	0000 0000	<u>uuuu</u> uuuu
BSR	0Fh	0000 0000	0000 0000	
Bank 0	I		I	
PORTA	10h	0-xx xxxx	0-uu uuuu	<u>uuuu</u> uuuu
DDRB	11h	1111 1111	1111 1111	 
PORTB	12h	XXXX XXXX	uuuu uuuu	uuuu uuuu
RCSTA	13h	0000 -00x	0000 -00u	uuuu -uuu
RCREG	14h	XXXX XXXX	uuuu uuuu	uuuu uuuu
TXSTA	15h	00001x	00001u	uuuuuu
TXREG	16h	XXXX XXXX	uuuu uuuu	uuuu uuuu
SPBRG	17h	XXXX XXXX	uuuu uuuu	นนนน นนนน
Bank 1				
DDRC	10h	1111 1111	1111 1111	uuuu uuuu
PORTC	11h	XXXX XXXX	uuuu uuuu	uuuu uuuu
DDRD	12h	1111 1111	1111 1111	uuuu uuuu
PORTD	13h	XXXX XXXX	uuuu uuuu	นนนน นนนน
DDRE	14h	111	111	uuu
PORTE	15h	xxx	uuu	uuu
PIR	16h	0000 0010	0000 0010	uuuu uuuu <sup>(1)</sup>
PIE	17h	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented read as '0', q = value depends on condition. Note 1: One or more bits in INTSTA, PIR will be affected (to cause wake-up).

When the wake-up is due to an interrupt and the GLINTD bit is cleared, the PC is loaded with the interrupt vector.

3: See Table 4-3 for reset value of specific condition.

4: Only applies to the PIC17C42.

5: Does not apply to the PIC17C42.

#### 9.4 PORTD and DDRD Registers

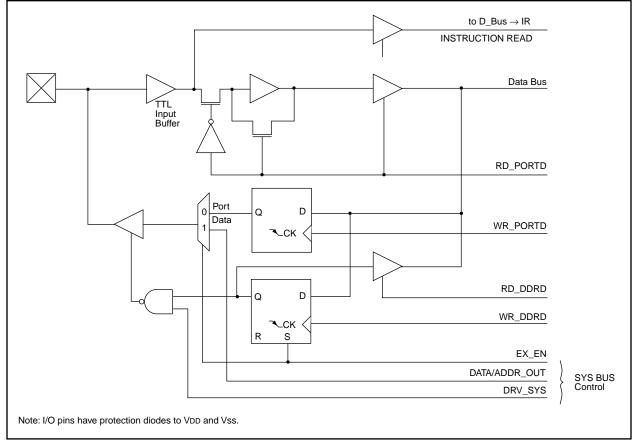
PORTD is an 8-bit bi-directional port. The corresponding data direction register is DDRD. A '1' in DDRD configures the corresponding port pin as an input. A '0' in the DDRC register configures the corresponding port pin as an output. Reading PORTD reads the status of the pins, whereas writing to it will write to the port latch. PORTD is multiplexed with the system bus. When operating as the system bus, PORTD is the high order byte of the address/data bus (AD15:AD8). The timing for the system bus is shown in the Electrical Characteristics section.

**Note:** This port is configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O. Example 9-3 shows the instruction sequence to initialize PORTD. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

#### EXAMPLE 9-3: INITIALIZING PORTD

MOVLB	1	;	Select Bank 1
CLRF	PORTD	;	Initialize PORTD data
		;	latches before setting
		;	the data direction
		;	register
MOVLW	0xCF	;	Value used to initialize
		;	data direction
MOVWF	DDRD	;	Set RD<3:0> as inputs
		;	RD<5:4> as outputs
		;	RD<7:6> as inputs





#### 9.4.1 PORTE AND DDRE REGISTER

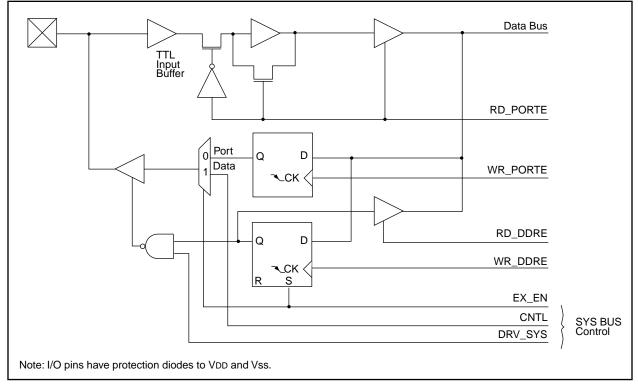
PORTE is a 3-bit bi-directional port. The corresponding data direction register is DDRE. A '1' in DDRE configures the corresponding port pin as an input. A '0' in the DDRE register configures the corresponding port pin as an output. Reading PORTE reads the status of the pins, whereas writing to it will write to the port latch. PORTE is multiplexed with the system bus. When operating as the system bus, PORTE contains the control signals for the address/data bus (AD15:AD0). These control signals are Address Latch Enable (ALE), Output Enable ( $\overline{OE}$ ), and Write ( $\overline{WR}$ ). The control signals  $\overline{OE}$  and  $\overline{WR}$  are active low signals. The timing for the system bus is shown in the Electrical Characteristics section.

Note: This port is configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O. Example 9-4 shows the instruction sequence to initialize PORTE. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

#### EXAMPLE 9-4: INITIALIZING PORTE

MOVLB	1	;	Select Bank 1
CLRF	PORTE	;	Initialize PORTE data
		;	latches before setting
		;	the data direction
		;	register
MOVLW	0x03	;	Value used to initialize
		;	data direction
MOVWF	DDRE	;	Set RE<1:0> as inputs
		;	RE<2> as outputs
		;	RE<7:3> are always
		;	read as '0'

#### FIGURE 9-8: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)



#### TABLE 9-9: PORTE FUNCTIONS

Name	Bit	Buffer Type	Function
RE0/ALE	bit0	TTL	Input/Output or system bus Address Latch Enable (ALE) control pin.
RE1/OE	bit1	TTL	Input/Output or system bus Output Enable (OE) control pin.
RE2/WR	bit2	TTL	Input/Output or system bus Write (WR) control pin.

Legend: TTL = TTL input.

#### TABLE 9-10: REGISTERS/BITS ASSOCIATED WITH PORTE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
15h, Bank 1	PORTE	—	—	—	—	_	RE2/WR	RE1/OE	RE0/ALE	xxx	uuu
14h, Bank 1	DDRE	Data dired	ata direction register for PORTE							111	111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PORTE.

Note 1: Other (non power-up) resets include: external reset through MCLR and the Watchdog Timer Reset.

ADDLW	ADD Literal to WREG					
Syntax:	[label] A	[ <i>label</i> ] ADDLW k				
Operands:	$0 \le k \le 25$	55				
Operation:	(WREG) -	+ k $\rightarrow$ (V	VREG)			
Status Affected:	OV, C, DC	C, Z				
Encoding:	1011	0001	kkkk	kkkk		
Description:	The contents of WREG are added to t 8-bit literal 'k' and the result is placed WREG.					
Words:	1					
Cycles:	1					
Q Cycle Activity:						
Q1	Q2	Q3	3	Q4		
Decode	Read literal 'k'	Execu		Vrite to WREG		
Example:	ADDLW	0x15				
Before Instruc WREG =						

ADDWF	ADD WRE	EG to f				
Syntax:	[ <i>label</i> ] A[	DDWF 1	f,d			
Operands:	$0 \le f \le 255$ $d \in [0,1]$	$\begin{array}{l} 0 \leq f \leq 255 \\ d \in \ [0,1] \end{array}$				
Operation:	(WREG) +	- (f) $\rightarrow$ (de	est)			
Status Affected:	OV, C, DC	, Z				
Encoding:	0000	111d	ffff	ffff		
Description:	Add WREG result is sto result is sto	red in WRE	EG. If 'd'	is 1 the		
Words:	1					
Cycles:	1					
Q Cycle Activity:						
Q1	Q2	Q3		Q4		
Decode	Read register 'f'	Execute	·   ·	/rite to stination		
Example:	ADDWF	REG, 0				
Before Instru WREG REG	iction = 0x17 = 0xC2					
After Instruct WREG REG	tion = 0xD9 = 0xC2					

After Instruction WREG = 0x25

MOVLR	Move Literal to high nibble in BSR			
Syntax:	[ <i>label</i> ] MOVLR k			
Operands:	$0 \le k \le 15$			
Operation:	$k \rightarrow (BSR < 7:4>)$			
Status Affected:	None			
Encoding:	1011 101x kkkk uuuu			
Description: The 4-bit literal 'k' is loaded into th most significant 4-bits of the Bank Select Register (BSR). Only the his 4-bits of the Bank Select Register are affected. The lower half of the BSR is unchanged. The assemble will encode the "u" fields as 0.				
Words:	1			
Cycles:	1			
Q Cycle Activity:				
Q1	Q2 Q3 Q4			
Decode	Read literal     Execute     Write       'k:u'     literal 'k' to     BSR<7:4>			
Example:	MOVLR 5			
Before Instruction BSR register = 0x22 After Instruction				
BSR regis				
	nstruction is not available in the C42 device.			

MOVLW	Move Literal to WREG
Syntax:	[ <i>label</i> ] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	$k \rightarrow (WREG)$
Status Affected:	None
Encoding:	1011 0000 kkkk kkkk
Description:	The eight bit literal 'k' is loaded into WREG.
Words:	1
Cycles:	1
Q Cycle Activity:	
Q1	Q2 Q3 Q4
Decode	Read Execute Write to literal 'k' WREG
Example:	MOVLW 0x5A
After Instruc WREG	

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TABLRD	Table R	ead	
Example1:	TABLRD	1, 1,	REG ;
Before Instruc	ction		
REG		=	0x53
TBLATH		=	0xAA
TBLATL		=	0x55
TBLPTR		=	0,4,1000
MEMORY	(TBLPTR)	=	0x1234
After Instruction	on (table v	write co	mpletion)
REG		=	0xAA
TBLATH		=	0x12
TBLATL		=	0x34
TBLPTR			0xA357
MEMORY	(TBLPTR)	=	0x5678
Example2:	TABLRD	0, 0,	REG ;
Before Instruc	ction		
REG		=	0x53
TBLATH		=	0xAA
TBLATL		=	0x55
TBLPTR		=	0xA356
MEMORY	(TBLPTR)	=	0x1234
After Instruction	on (table v	write co	mpletion)
REG		=	0x55
TBLATH		=	0x12
TBLATL		=	0x34
TBLPTR		=	0xA356
MEMORY	(TBLPTR)	=	0x1234

TABLWT	Table Writ	-		
Syntax:	[ <i>label</i> ] T	ABLWT	t,i,f	
Operands:	$0 \le f \le 255$ $i \in [0,1]$ $t \in [0,1]$	5		
Operation:	If $t = 0$ , $f \rightarrow TB$	LATL;		
	If t = 1, f $\rightarrow$ TB	LATH; $\rightarrow$ Prog	Mom	
	lf i = 1,	$R + 1 \rightarrow$		
Status Affected:	None			
Encoding:	1010	11ti	ffff	ffff
Description:	latch ( If t = 0	value in 'f' TBLAT) : load into : load into	low by	te;
	to the pointe	ontents of program r d to by TB _PTR poi	nemory LPTR	location
	the ins If TBL	m memor struction ta PTR point M locati	akes tw ts to ar	o-cycle
	instruc	ction is te	erminat	ed when
	LR/VPP pin m for successfu			
-	VPP = VDD gramming sec	wence of	intern	al memor
will be	executed, be h the interna	ut will no	ot be	successf
	- /	BLPTR ca	an be a	automati-
		ncremente ; TBLPTF		
	lf i = 1	increme ; TBLPTF		emented
Words:	1	, 182111		omoniou
Cycles:	2 (many if EPROM p			
Q Cycle Activity:				
Q1	Q2	Q3		Q4
Decode	Read register 'f'	Execut	e	Write

#### 16.6 <u>PICDEM-1 Low-Cost PIC16/17</u> <u>Demonstration Board</u>

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-16B programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the PICMASTER emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

#### 16.7 <u>PICDEM-2 Low-Cost PIC16CXX</u> Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-16C, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I<sup>2</sup>C bus and separate headers for connection to an LCD module and a keypad.

#### 16.8 <u>PICDEM-3 Low-Cost PIC16CXXX</u> Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals. PICDEM-3 will be available in the 3rd quarter of 1996.

#### 16.9 <u>MPLAB Integrated Development</u> <u>Environment Software</u>

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- · A full featured editor
- Three operating modes
  - editor
  - emulator
  - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

#### MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC16/17 tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
- Transfer data dynamically via DDE (soon to be replaced by OLE)
- Run up to four emulators on the same PC

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

#### 16.10 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PChosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

Droduct	** MDI ADTM		MD-Drivo/Mov		*** DICMACTED®/				DIC CTADT® DI
	Integrated	Compiler	Applications	Explorer/Edition	PICMASTER-CE	Low-Cost	II Universal	Ultra Low-Cost	Low-Cost
	Development Environment		Code Generator	Fuzzy Logic Dev. Tool	In-Circuit Emulator	In-Circuit Emulator	Microchip Programmer	Dev. Kit	Universal Dev. Kit
PIC12C508, 509	SW007002	SW006005	1	I	EM167015/ EM167101	1	DV007003	1	DV003001
PIC14000	SW007002	SW006005	I	I	EM147001/ EM147101	1	DV007003	I	DV003001
PIC16C52, 54, 54A, 55, 56, 57, 58A	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167015/ EM167101	EM167201	DV007003	DV162003	DV003001
PIC16C554, 556, 558	SW007002	SW006005	1	DV005001/ DV005002	EM167033/ EM167113	1	DV007003	I	DV003001
PIC16C61	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167021/ N/A	EM167205	DV007003	DV162003	DV003001
PIC16C62, 62A, 64, 64A	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167025/ EM167103	EM167203	DV007003	DV162002	DV003001
PIC16C620, 621, 622	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167023/ EM167109	EM167202	DV007003	DV162003	DV003001
PIC16C63, 65, 65A, 73, 73A, 74, 74A	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167025/ EM167103	EM167204	DV007003	DV162002	DV003001
PIC16C642, 662*	SW007002	SW006005	1	I	EM167035/ EM167105	1	DV007003	DV162002	DV003001
PIC16C71	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167027/ EM167105	EM167205	DV007003	DV162003	DV003001
PIC16C710, 711	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167027/ EM167105	1	DV007003	DV162003	DV003001
PIC16C72	SW007002	SW006005	SW006006	I	EM167025/ EM167103	1	DV007003	DV162002	DV003001
PIC16F83	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167029/ EM167107	1	DV007003	DV162003	DV003001
PIC16C84	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167029/ EM167107	EM167206	DV007003	DV162003	DV003001
PIC16F84	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167029/ EM167107		DV007003	DV162003	DV003001
PIC16C923, 924*	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167031/ EM167111		DV007003	I	DV003001
PIC17C42, 42A, 43, 44	SW007002	SW006005	SW006006	DV005001/ DV005002	EM177007/ EM177107	1	DV007003	I	DV003001
*Contact Microchip Technology for availability date **MPLAB Integrated Development Environment includes MPLAB-SIM Simulator and MPASM Assembler	innology for avails velopment Enviro	ability date inment includes	s MPLAB-SIM Sir	mulator and	***All PICMASTER and PICMASTER-CE ordering part numbers above include PRO MATE II programmer ****PRO MATE socket modules are ordered separately. See development systems ordering guide for specific ordering part numbers	and PICMAST rogrammer at modules are or specific orde	II PICMASTER and PICMASTER-CE ordering par PRO MATE II programmer RO MATE socket modules are ordered separately. ordering guide for specific ordering part numbers	***All PICMASTER and PICMASTER-CE ordering part numbers above include PRO MATE II programmer **PRO MATE socket modules are ordered separately. See development system ordering guide for specific ordering part numbers	lude stems
Product	TRUEGAUGI	<b>TRUEGAUGE®</b> Development Kit		<b>SEEVAL® Designers Kit</b>	Hopping Code Security Programmer Kit	Security Prog		Hopping Code Security Eval/Demo Kit	ity Eval/Demo Kit
All 2 wire and 3 wire Serial EEPROM's		N/A		DV243001		N/A		N/A	
MTA11200B		DV114001		N/A		N/A		N/A	
HCS200, 300, 301 *		N/A		N/A	-	PG306001		DM303001	001

#### TABLE 16-1: DEVELOPMENT TOOLS FROM MICROCHIP

PIC17C4X

#### Applicable Devices 42 R42 42A 43 R43 44

#### 17.1 DC CHARACTERISTICS:

#### PIC17C42-16 (Commercial, Industrial) PIC17C42-25 (Commercial, Industrial)

DC CHARA	CTERIS	STICS	Standard Operating	-	-		ns (unless otherwise stated)
						-40°C	
		1	1			0°C	$\leq$ TA $\leq$ +70°C for commercial
Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
D001	Vdd	Supply Voltage	4.5	_	5.5	V	
D002	Vdr	RAM Data Retention Voltage (Note 1)	1.5 *	-	-	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	-	Vss	-	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.060*	_	_	mV/ms	See section on Power-on Reset for details
D010	IDD	Supply Current	_	3	6	mA	Fosc = 4 MHz (Note 4)
D011		(Note 2)	-	6	12 *	mA	Fosc = 8 MHz
D012			-	11	24 *	mA	Fosc = 16 MHz
D013			-	19	38	mA	Fosc = 25 MHz
D014			-	95	150	μA	Fosc = 32 kHz WDT enabled (EC osc configuration)
D020	IPD	Power-down Current	_	10	40	μA	VDD = 5.5V, WDT enabled
D021		(Note 3)	-	< 1	5	μA	VDD = 5.5V, WDT disabled

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD or VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

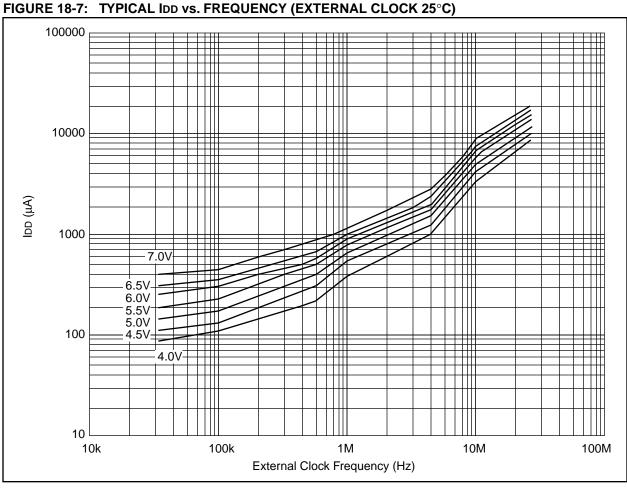
Current consumed from the oscillator and I/O's driving external capacitive or resistive loads need to be considered.

For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as:  $VDD / (2 \cdot R)$ . For capacitive loads, The current can be estimated (for an individual I/O pin) as (CL  $\cdot VDD$ )  $\cdot f$ 

CL = Total capacitive load on the I/O pin; f = average frequency on the I/O pin switches.

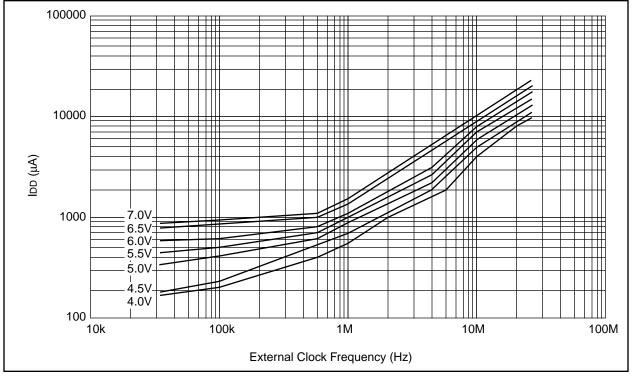
The capacitive currents are most significant when the device is configured for external execution (includes extended microcontroller mode).

- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, all I/O pins in hi-impedance state and tied to VDD or Vss.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.



#### Applicable Devices 42 R42 42A 43 R43 44

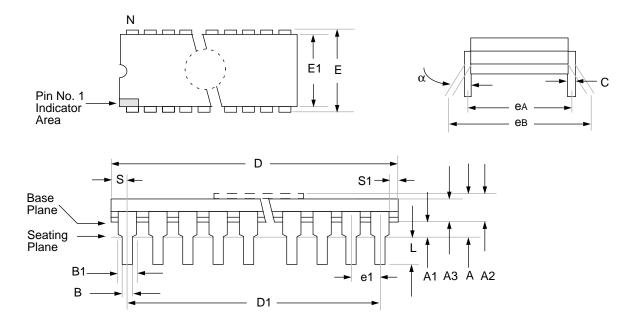




NOTES:

#### 21.0 PACKAGING INFORMATION

#### 21.1 40-Lead Ceramic CERDIP Dual In-line, and CERDIP Dual In-line with Window (600 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
		Millimeters			Inches	
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
А	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
В	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
С	0.203	0.381	Typical	0.008	0.015	Typical
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	14.986	16.002	Typical	0.590	0.630	Typical
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
Ν	40	40		40	40	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

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### APPENDIX F: ERRATA FOR PIC17C42 SILICON

The PIC17C42 devices that you have received have the following anomalies. At present there is no intention for future revisions to the present PIC17C42 silicon. If these cause issues for the application, it is recommended that you select the PIC17C42A device.

**Note:** New designs should use the PIC17C42A.

 When the Oscillator Start-Up Timer (OST) is enabled (in LF or XT oscillator modes), any interrupt that wakes the processor may cause a WDT reset. This occurs when the WDT is greater than or equal to 50% time-out period when the SLEEP instruction is executed. This will not occur in either the EC or RC oscillator modes.

#### Work-arounds

- Always ensure that the CLRWDT instruction is executed before the WDT increments past 50% of the WDT period. This will keep the "false" WDT reset from occurring.
- b) When using the WDT as a normal timer (WDT disabled), ensure that the WDT is less than or equal to 50% time-out period when the SLEEP instruction is executed. This can be done by monitoring the TO bit for changing state from set to clear. Example 1 shows putting the PIC17C42 to sleep.

#### EXAMPLE F-1: PIC17C42 TO SLEEP

BTFSS	CPUSTA,	TO	;	TO = 0?
CLRWDT			;	YES, WDT = $0$
BTFSC	CPUSTA,	то	;	WDT rollover?
GOTO	LOOP		;	NO, Wait
SLEEP			;	YES, goto Sleep
	CLRWDT BTFSC GOTO	CLRWDT BTFSC CPUSTA, GOTO LOOP	CLRWDT BTFSC CPUSTA, TO GOTO LOOP	BTFSC CPUSTA, TO ; GOTO LOOP ;

2. When the clock source of Timer1 or Timer2 is selected to external clock, the overflow interrupt flag will be set twice, once when the timer equals the period, and again when the timer value is reset to 0h. If the latency to clear TMRxIF is greater than the time to the next clock pulse, no problems will be noticed. If the latency is less than the time to the next timer clock pulse, the interrupt will be serviced twice.

#### Work-arounds

- a) Ensure that the timer has rolled over to 0h before clearing the flag bit.
- b) Clear the timer in software. Clearing the timer in software causes the period to be one count less than expected.

#### **Design considerations**

The device must not be operated outside of the specified voltage range. An external reset circuit must be used to ensure the device is in reset when a brown-out occurs or the VDD rise time is too long. Failure to ensure that the device is in reset when device voltage is out of specification may cause the device to lock-up and ignore the  $\overline{\text{MCLR}}$  pin.

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