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### What is "[Embedded - Microcontrollers](#)"?

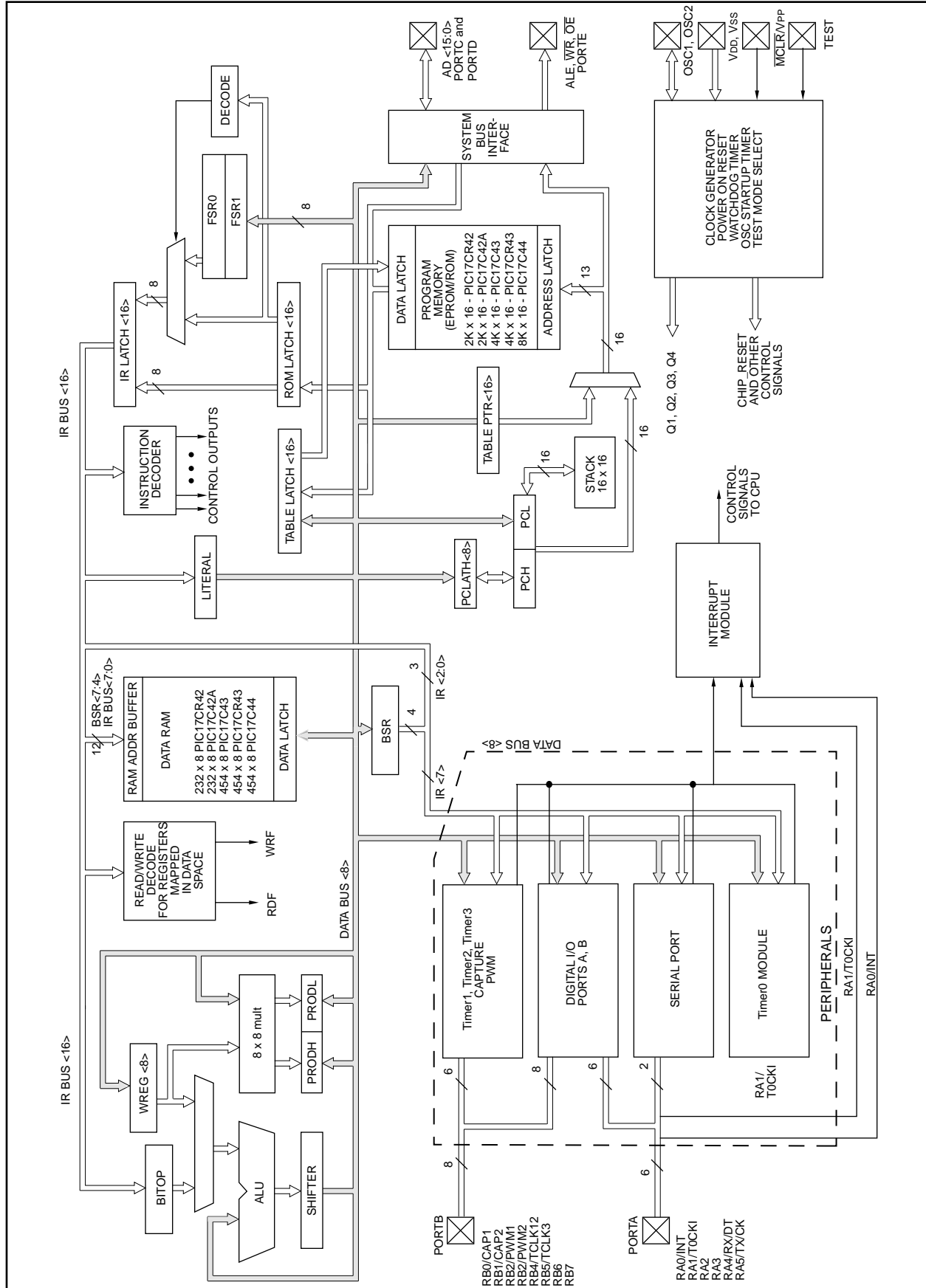
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	33MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	33
Program Memory Size	8KB (4K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	454 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic17c43-33-p">https://www.e-xfl.com/product-detail/microchip-technology/pic17c43-33-p</a>

FIGURE 3-2: PIC17CR42/42A/43/R43/44 BLOCK DIAGRAM



**TABLE 3-1: PINOUT DESCRIPTIONS**

Name	DIP No.	PLCC No.	QFP No.	I/O/P Type	Buffer Type	Description
RD0/AD8	40	43	15	I/O	TTL	PORTD is a bi-directional I/O Port. This is also the upper byte of the 16-bit system bus in microprocessor mode or extended microprocessor mode or extended microcontroller mode. In multiplexed system bus configuration these pins are address output as well as data input or output.
RD1/AD9	39	42	14	I/O	TTL	
RD2/AD10	38	41	13	I/O	TTL	
RD3/AD11	37	40	12	I/O	TTL	
RD4/AD12	36	39	11	I/O	TTL	
RD5/AD13	35	38	10	I/O	TTL	
RD6/AD14	34	37	9	I/O	TTL	
RD7/AD15	33	36	8	I/O	TTL	
RE0/ALE	30	32	4	I/O	TTL	PORTE is a bi-directional I/O Port. In microprocessor mode or extended microcontroller mode, it is the Address Latch Enable (ALE) output. Address should be latched on the falling edge of ALE output. In microprocessor or extended microcontroller mode, it is the Output Enable ( $\overline{OE}$ ) control output (active low). In microprocessor or extended microcontroller mode, it is the Write Enable ( $\overline{WR}$ ) control output (active low).
RE1/ $\overline{OE}$	29	31	3	I/O	TTL	
RE2/ $\overline{WR}$	28	30	2	I/O	TTL	
TEST	27	29	1	I	ST	Test mode selection control input. Always tie to Vss for normal operation.
Vss	10, 31	11, 12, 33, 34	5, 6, 27, 28	P		Ground reference for logic and I/O pins.
VDD	1	1, 44	16, 17	P		Positive supply for logic and I/O pins.

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input.

NOTES:

## 9.4.1 PORTE AND DDRE REGISTER

PORTE is a 3-bit bi-directional port. The corresponding data direction register is DDRE. A '1' in DDRE configures the corresponding port pin as an input. A '0' in the DDRE register configures the corresponding port pin as an output. Reading PORTE reads the status of the pins, whereas writing to it will write to the port latch. PORTE is multiplexed with the system bus. When operating as the system bus, PORTE contains the control signals for the address/data bus (AD15:AD0). These control signals are Address Latch Enable (ALE), Output Enable ( $\overline{OE}$ ), and Write ( $\overline{WR}$ ). The control signals  $\overline{OE}$  and  $\overline{WR}$  are active low signals. The timing for the system bus is shown in the Electrical Characteristics section.

**Note:** This port is configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O.

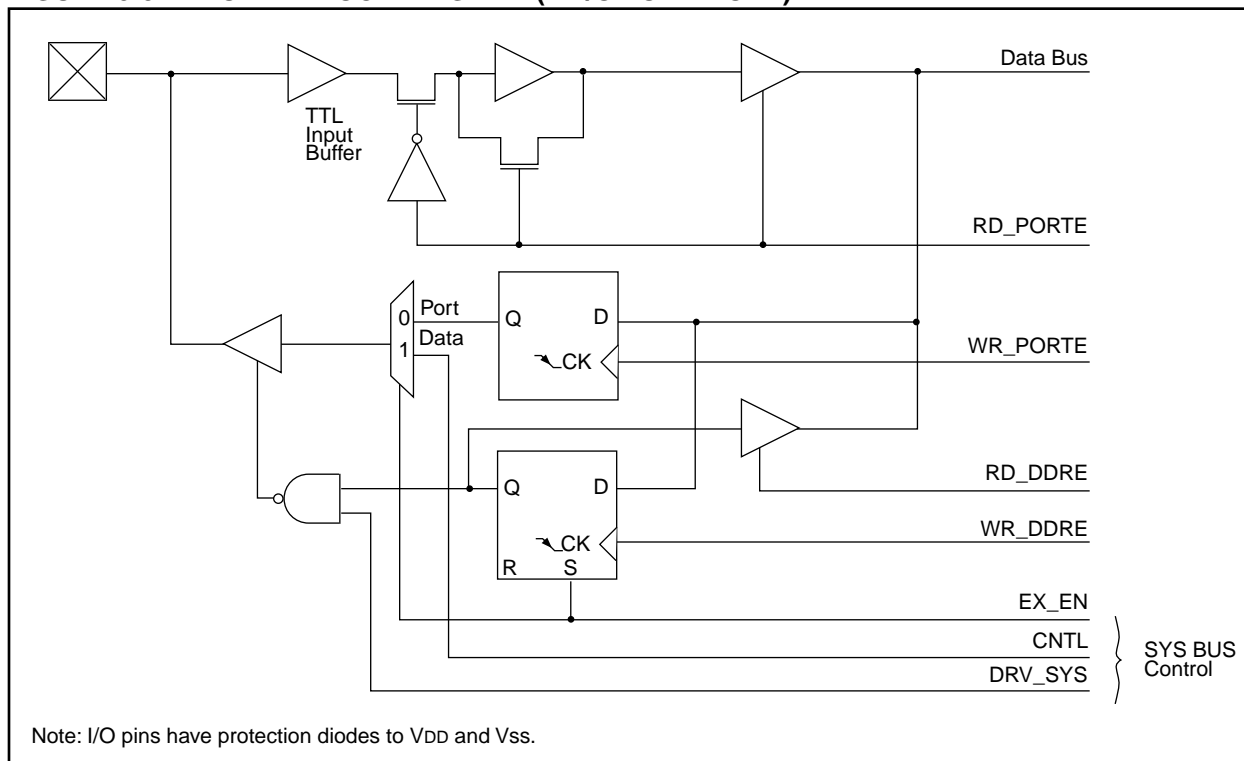
Example 9-4 shows the instruction sequence to initialize PORTE. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

### EXAMPLE 9-4: INITIALIZING PORTE

```

MOVLB 1           ; Select Bank 1
CLRF  PORTE       ; Initialize PORTE data
                  ; latches before setting
                  ; the data direction
                  ; register
MOVLW 0x03        ; Value used to initialize
                  ; data direction
MOVWF DDRE        ; Set RE<1:0> as inputs
                  ; RE<2> as outputs
                  ; RE<7:3> are always
                  ; read as '0'
    
```

**FIGURE 9-8: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)**



# PIC17C4X

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NOTES:

## 12.0 TIMER1, TIMER2, TIMER3, PWMS AND CAPTURES

The PIC17C4X has a wealth of timers and time-based functions to ease the implementation of control applications. These time-base functions include two PWM outputs and two Capture inputs.

Timer1 and Timer2 are two 8-bit incrementing timers, each with a period register (PR1 and PR2 respectively) and separate overflow interrupt flags. Timer1 and Timer2 can operate either as timers (increment on internal Fosc/4 clock) or as counters (increment on falling edge of external clock on pin RB4/TCLK12). They are also software configurable to operate as a single 16-bit timer. These timers are also used as the time-base for the PWM (pulse width modulation) module.

Timer3 is a 16-bit timer/counter consisting of the TMR3H and TMR3L registers. This timer has four other associated registers. Two registers are used as a 16-bit period register or a 16-bit Capture1 register (PR3H/CA1H:PR3L/CA1L). The other two registers are strictly the Capture2 registers (CA2H:CA2L). Timer3 is the time-base for the two 16-bit captures.

TMR3 can be software configured to increment from the internal system clock or from an external signal on the RB5/TCLK3 pin.

Figure 12-1 and Figure 12-2 are the control registers for the operation of Timer1, Timer2, and Timer3, as well as PWM1, PWM2, Capture1, and Capture2.

**FIGURE 12-1: TCON1 REGISTER (ADDRESS: 16h, BANK 3)**

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0
CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS
bit7							bit0
<p>bit 7-6: <b>CA2ED1:CA2ED0</b>: Capture2 Mode Select bits            00 = Capture on every falling edge            01 = Capture on every rising edge            10 = Capture on every 4th rising edge            11 = Capture on every 16th rising edge</p> <p>bit 5-4: <b>CA1ED1:CA1ED0</b>: Capture1 Mode Select bits            00 = Capture on every falling edge            01 = Capture on every rising edge            10 = Capture on every 4th rising edge            11 = Capture on every 16th rising edge</p> <p>bit 3: <b>T16</b>: Timer1:Timer2 Mode Select bit            1 = Timer1 and Timer2 form a 16-bit timer            0 = Timer1 and Timer2 are two 8-bit timers</p> <p>bit 2: <b>TMR3CS</b>: Timer3 Clock Source Select bit            1 = TMR3 increments off the falling edge of the RB5/TCLK3 pin            0 = TMR3 increments off the internal clock</p> <p>bit 1: <b>TMR2CS</b>: Timer2 Clock Source Select bit            1 = TMR2 increments off the falling edge of the RB4/TCLK12 pin            0 = TMR2 increments off the internal clock</p> <p>bit 0: <b>TMR1CS</b>: Timer1 Clock Source Select bit            1 = TMR1 increments off the falling edge of the RB4/TCLK12 pin            0 = TMR1 increments off the internal clock</p>							

R = Readable bit  
 W = Writable bit  
 -n = Value at POR reset

## 12.2.1 ONE CAPTURE AND ONE PERIOD REGISTER MODE

In this mode registers PR3H/CA1H and PR3L/CA1L constitute a 16-bit period register. A block diagram is shown in Figure 12-7. The timer increments until it equals the period register and then resets to 0000h. TMR3 Interrupt Flag bit (TMR3IF) is set at this point. This interrupt can be disabled by clearing the TMR3 Interrupt Enable bit (TMR3IE). TMR3IF must be cleared in software.

This mode is selected if control bit CA1/PR3 is clear. In this mode, the Capture1 register, consisting of high byte (PR3H/CA1H) and low byte (PR3L/CA1L), is configured as the period control register for TMR3. Capture1 is disabled in this mode, and the corresponding Interrupt bit CA1IF is never set. TMR3 increments until it equals the value in the period register and then resets to 0000h.

Capture2 is active in this mode. The CA2ED1 and CA2ED0 bits determine the event on which capture will occur. The possible events are:

- Capture on every falling edge
- Capture on every rising edge
- Capture every 4th rising edge
- Capture every 16th rising edge

When a capture takes place, an interrupt flag is latched into the CA2IF bit. This interrupt can be enabled by setting the corresponding mask bit CA2IE. The Peripheral Interrupt Enable bit (PEIE) must be set and the Global Interrupt Disable bit (GLINTD) must be cleared for the interrupt to be acknowledged. The CA2IF interrupt flag bit must be cleared in software.

When the capture prescale select is changed, the prescaler is not reset and an event may be generated. Therefore, the first capture after such a change will be ambiguous. However, it sets the time-base for the next capture. The prescaler is reset upon chip reset.

Capture pin RB1/CAP2 is a multiplexed pin. When used as a port pin, Capture2 is not disabled. However, the user can simply disable the Capture2 interrupt by clearing CA2IE. If RB1/CAP2 is used as an output pin, the user can activate a capture by writing to the port pin. This may be useful during development phase to emulate a capture interrupt.

The input on capture pin RB1/CAP2 is synchronized internally to internal phase clocks. This imposes certain restrictions on the input waveform (see the Electrical Specification section for timing).

The Capture2 overflow status flag bit is double buffered. The master bit is set if one captured word is already residing in the Capture2 register and another "event" has occurred on the RB1/CA2 pin. The new event will not transfer the Timer3 value to the capture register, protecting the previous unread capture value. When the user reads both the high and the low bytes (in any order) of the Capture2 register, the master overflow bit is transferred to the slave overflow bit (CA2OVF) and then the master bit is reset. The user can then read TCON2 to determine the value of CA2OVF.

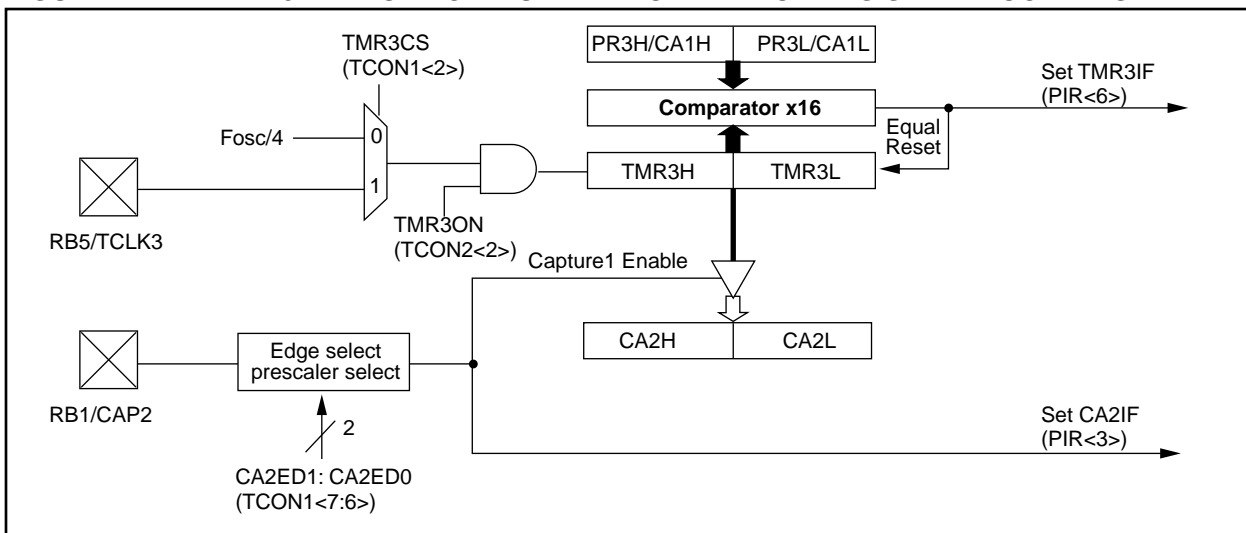
The recommended sequence to read capture registers and capture overflow flag bits is shown in Example 12-1.

### EXAMPLE 12-1: SEQUENCE TO READ CAPTURE REGISTERS

```

MOVLB 3           ;Select Bank 3
MOVPF CA2L,LO_BYTE ;Read Capture2 low
                  ;byte, store in LO_BYTE
MOVPF CA2H,HI_BYTE ;Read Capture2 high
                  ;byte, store in HI_BYTE
MOVPF TCON2,STAT_VAL ;Read TCON2 into file
                  ;STAT_VAL
    
```

**FIGURE 12-7: TIMER3 WITH ONE CAPTURE AND ONE PERIOD REGISTER BLOCK DIAGRAM**



BSF	Bit Set f				
Syntax:	[ <i>label</i> ] BSF f,b				
Operands:	$0 \leq f \leq 255$ $0 \leq b \leq 7$				
Operation:	$1 \rightarrow (f < b)$				
Status Affected:	None				
Encoding:	<table><tr><td>1000</td><td>0bbb</td><td>ffff</td><td>ffff</td></tr></table>	1000	0bbb	ffff	ffff
1000	0bbb	ffff	ffff		
Description:	Bit 'b' in register 'f' is set.				
Words:	1				
Cycles:	1				

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f'

Example: BSF FLAG\_REG, 7

Before Instruction

FLAG\_REG= 0x0A

After Instruction

FLAG\_REG= 0x8A

BTFSC	Bit Test, skip if Clear				
Syntax:	[ <i>label</i> ] BTFSC f,b				
Operands:	$0 \leq f \leq 255$ $0 \leq b \leq 7$				
Operation:	skip if (f<b>) = 0				
Status Affected:	None				
Encoding:	<table><tr><td>1001</td><td>1bbb</td><td>ffff</td><td>ffff</td></tr></table>	1001	1bbb	ffff	ffff
1001	1bbb	ffff	ffff		
Description:	If bit 'b' in register 'f' is 0 then the next instruction is skipped. If bit 'b' is 0 then the next instruction fetched during the current instruction exe-				

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	NOP

If skip:

Q1	Q2	Q3	Q4
Forced NOP	NOP	Execute	NOP

Example: HERE BTFSC FLAG, 1  
FALSE :  
TRUE :

Before Instruction

PC = address (HERE)

After Instruction

If FLAG<1> = 0;

PC = address (TRUE)

If FLAG<1> = 1;

PC = address (FALSE)

## DECF Decrement f

Syntax: [ *label* ] DECF f,d

Operands:  $0 \leq f \leq 255$   
 $d \in [0,1]$

Operation:  $(f) - 1 \rightarrow (\text{dest})$

Status Affected: OV, C, DC, Z

Encoding: 

0000	011d	ffff	ffff
------	------	------	------

Description: Decrement register 'f'. If 'd' is 0 the result is stored in WREG. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: DECF CNT, 1

Before Instruction

CNT = 0x01  
Z = 0

After Instruction

CNT = 0x00  
Z = 1

## DECFSZ Decrement f, skip if 0

Syntax: [ *label* ] DECFSZ f,d

Operands:  $0 \leq f \leq 255$   
 $d \in [0,1]$

Operation:  $(f) - 1 \rightarrow (\text{dest})$ ;  
skip if result = 0

Status Affected: None

Encoding: 

0001	011d	ffff	ffff
------	------	------	------

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is placed back in register 'f'.

If the result is 0, the next instruction, which is already fetched, is discarded, and an NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: HERE DECFSZ CNT, 1  
GOTO LOOP

CONTINUE

Before Instruction

PC = Address (HERE)

After Instruction

CNT = CNT - 1  
If CNT = 0;  
PC = Address (CONTINUE)  
If CNT  $\neq$  0;  
PC = Address (HERE+1)

## MOVPF Move p to f

Syntax: `[label] MOVPF p,f`

Operands:  $0 \leq f \leq 255$   
 $0 \leq p \leq 31$

Operation:  $(p) \rightarrow (f)$

Status Affected: Z

Encoding: 

010p	pppp	ffff	ffff
------	------	------	------

Description: Move data from data memory location 'p' to data memory location 'f'. Location 'f' can be anywhere in the 256 byte data space (00h to FFh) while 'p' can be 00h to 1Fh.

Either 'p' or 'f' can be WREG (a useful special situation).

MOVPF is particularly useful for transferring a peripheral register (e.g. the timer or an I/O port) to a data memory location. Both 'f' and 'p' can be indirectly addressed.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'p'	Execute	Write register 'f'

Example: `MOVPF REG1, REG2`

Before Instruction

REG1 = 0x11  
 REG2 = 0x33

After Instruction

REG1 = 0x11  
 REG2 = 0x11

## MOVWF Move WREG to f

Syntax: `[label] MOVWF f`

Operands:  $0 \leq f \leq 255$

Operation:  $(WREG) \rightarrow (f)$

Status Affected: None

Encoding: 

0000	0001	ffff	ffff
------	------	------	------

Description: Move data from WREG to register 'f'. Location 'f' can be anywhere in the 256 word data space.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f'

Example: `MOVWF REG`

Before Instruction

WREG = 0x4F  
 REG = 0xFF

After Instruction

WREG = 0x4F  
 REG = 0x4F

NEGW

Negate W

Syntax:

[*label*] NEGW f,s

Operands:

$0 \leq F \leq 255$

$s \in [0,1]$

Operation:

$\overline{WREG} + 1 \rightarrow (f);$

$\overline{WREG} + 1 \rightarrow s$

Status Affected:

OV, C, DC, Z

Encoding:

0010	110s	ffff	ffff
------	------	------	------

Description:

WREG is negated using two's complement. If 's' is 0 the result is placed in WREG and data memory location 'f'. If 's' is 1 the result is placed only in data memory location 'f'.

Words:

1

Cycles:

1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f' and other specified register

Example:                NEGW    REG,0

Before Instruction  
WREG    =    0011 1010 [0x3A],  
REG      =    1010 1011 [0xAB]  
  
After Instruction  
WREG    =    1100 0111 [0xC6]  
REG      =    1100 0111 [0xC6]

NOP

No Operation

Syntax:

[*label*] NOP

Operands:

None

Operation:

No operation

Status Affected:

None

Encoding:

0000	0000	0000	0000
------	------	------	------

Description:

No operation.

Words:

1

Cycles:

1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	NOP	Execute	NOP

Example:  
  
None.

XORLW		Exclusive OR Literal with WREG							
Syntax:	[ <i>label</i> ] XORLW k								
Operands:	0 ≤ k ≤ 255								
Operation:	(WREG) .XOR. k → (WREG)								
Status Affected:	Z								
Encoding:	<table><tr><td>1011</td><td>0100</td><td>kkkk</td><td>kkkk</td></tr></table>					1011	0100	kkkk	kkkk
1011	0100	kkkk	kkkk						
Description:	The contents of WREG are XOR'ed with the 8-bit literal 'k'. The result is placed in WREG.								
Words:	1								
Cycles:	1								
Q Cycle Activity:									
	Q1	Q2	Q3	Q4					
	Decode	Read literal 'k'	Execute	Write to WREG					

**Example:** XORLW 0xAF

Before Instruction  
WREG = 0xB5

After Instruction  
WREG = 0x1A

XORWF		Exclusive OR WREG with f						
Syntax:	[ <i>label</i> ] XORWF f,d							
Operands:	0 ≤ f ≤ 255 d ∈ [0,1]							
Operation:	(WREG) .XOR. (f) → (dest)							
Status Affected:	Z							
Encoding:	<table><tr><td>0000</td><td>110d</td><td>ffff</td><td>ffff</td></tr></table>				0000	110d	ffff	ffff
0000	110d	ffff	ffff					
Description:	Exclusive OR the contents of WREG with register 'f'. If 'd' is 0 the result is stored in WREG. If 'd' is 1 the result is stored back in the register 'f'.							
Words:	1							
Cycles:	1							
Q Cycle Activity:								
	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Execute	Write to destination				

**Example:** XORWF REG, 1

Before Instruction  
REG = 0xAF  
WREG = 0xB5

After Instruction  
REG = 0x1A  
WREG = 0xB5

## 17.0 PIC17C42 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Ambient temperature under bias .....	-55 to +125°C
Storage temperature .....	-65°C to +150°C
Voltage on VDD with respect to VSS .....	0 to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS (Note 2) .....	-0.6V to +14V
Voltage on RA2 and RA3 with respect to VSS.....	-0.6V to +12V
Voltage on all other pins with respect to VSS .....	-0.6V to VDD + 0.6V
Total power dissipation (Note 1).....	1.0W
Maximum current out of VSS pin(s) - Total .....	250 mA
Maximum current into VDD pin(s) - Total .....	200 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > VDD) .....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > VDD).....	±20 mA
Maximum output current sunk by any I/O pin (except RA2 and RA3).....	35 mA
Maximum output current sunk by RA2 or RA3 pins .....	60 mA
Maximum output current sourced by any I/O pin .....	20 mA
Maximum current sunk by PORTA and PORTB (combined).....	150 mA
Maximum current sourced by PORTA and PORTB (combined).....	100 mA
Maximum current sunk by PORTC, PORTD and PORTE (combined).....	150 mA
Maximum current sourced by PORTC, PORTD and PORTE (combined).....	100 mA

**Note 1:** Power dissipation is calculated as follows:  $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

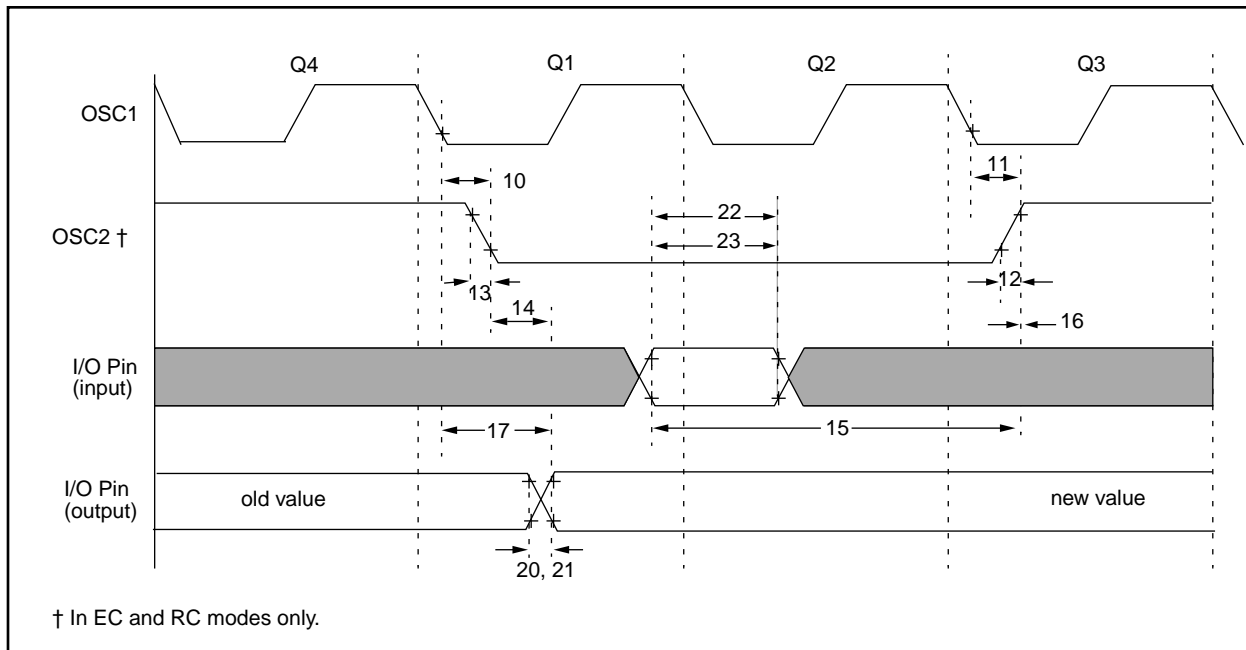
**Note 2:** Voltage spikes below VSS at the  $\overline{\text{MCLR}}$  pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the  $\overline{\text{MCLR}}$  pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# PIC17C4X

Applicable Devices 42 R42 42A 43 R43 44

**FIGURE 17-3: CLKOUT AND I/O TIMING**



**TABLE 17-3: CLKOUT AND I/O TIMING REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	—	15 ‡	30 ‡	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑	—	15 ‡	30 ‡	ns	Note 1
12	TckR	CLKOUT rise time	—	5 ‡	15 ‡	ns	Note 1
13	TckF	CLKOUT fall time	—	5 ‡	15 ‡	ns	Note 1
14	TckH2ioV	CLKOUT↑ to Port out valid	—	—	0.5Tcy + 20‡	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT↑	0.25Tcy + 25 ‡	—	—	ns	Note 1
16	TckH2ioI	Port in hold after CLKOUT↑	0 ‡	—	—	ns	Note 1
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	—	100 ‡	ns	
20	TioR	Port output rise time	—	10 ‡	35 ‡	ns	
21	TioF	Port output fall time	—	10 ‡	35 ‡	ns	
22	TinHL	INT pin high or low time	25 *	—	—	ns	
23	TrbHL	RB7:RB0 change INT high or low time	25 *	—	—	ns	

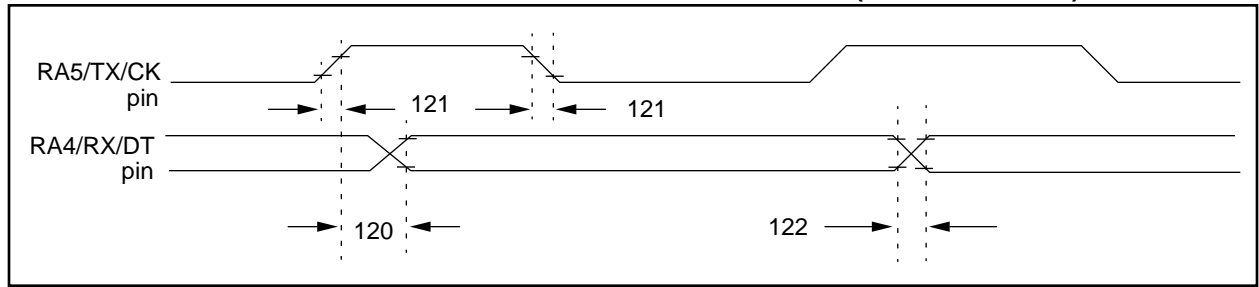
\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Measurements are taken in EC Mode where OSC2 output = 4 x TOSC = Tcy.

**FIGURE 19-9: USART MODULE: SYNCHRONOUS TRANSMISSION (MASTER/S�AVE) TIMING**

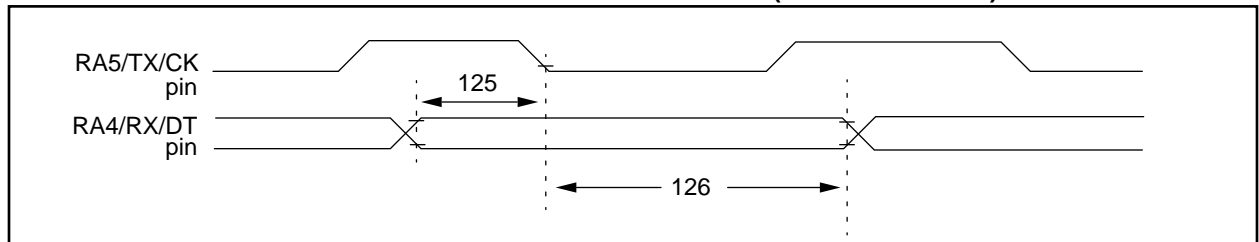


**TABLE 19-9: SYNCHRONOUS TRANSMISSION REQUIREMENTS**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC17CR42/42A/43/R43/44	—	—	50	ns
			PIC17LCR42/42A/43/R43/44	—	—	75	ns
121	TckRF	Clock out rise time and fall time (Master Mode)	PIC17CR42/42A/43/R43/44	—	—	25	ns
			PIC17LCR42/42A/43/R43/44	—	—	40	ns
122	TdtRF	Data out rise time and fall time	PIC17CR42/42A/43/R43/44	—	—	25	ns
			PIC17LCR42/42A/43/R43/44	—	—	40	ns

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 19-10: USART MODULE: SYNCHRONOUS RECEIVE (MASTER/S�AVE) TIMING**

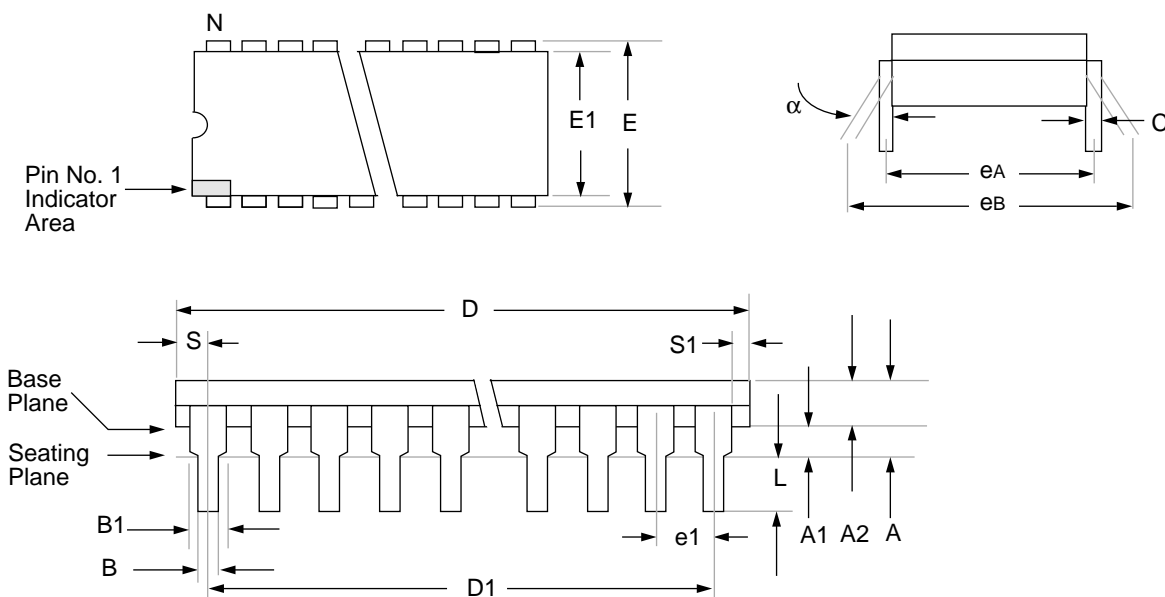


**TABLE 19-10: SYNCHRONOUS RECEIVE REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data hold before CK↓ (DT hold time)	15	—	—	ns	
126	TckL2dtI	Data hold after CK↓ (DT hold time)	15	—	—	ns	

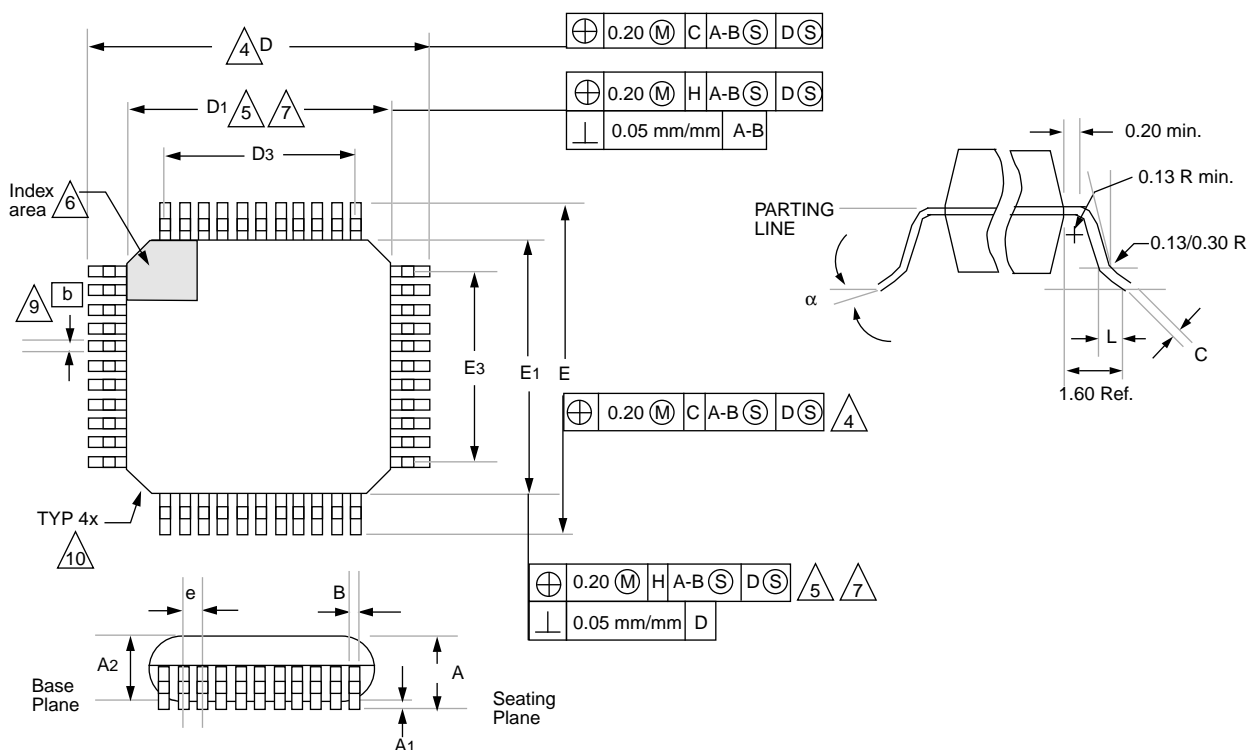
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## 21.2 40-Lead Plastic Dual In-line (600 mil)



Package Group: Plastic Dual In-Line (PLA)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
$\alpha$	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	—		0.015	—	
A2	3.175	4.064		0.125	0.160	
B	0.355	0.559		0.014	0.022	
B1	1.270	1.778	Typical	0.050	0.070	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	51.181	52.197		2.015	2.055	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875		0.600	0.625	
E1	13.462	13.970		0.530	0.550	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	40	40		40	40	
S	1.270	—		0.050	—	
S1	0.508	—		0.020	—	

## 21.4 44-Lead Plastic Surface Mount (MQFP 10x10 mm Body 1.6/0.15 mm Lead Form)



Package Group: Plastic MQFP						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
$\alpha$	0°	7°		0°	7°	
A	2.000	2.350		0.078	0.093	
A1	0.050	0.250		0.002	0.010	
A2	1.950	2.100		0.768	0.083	
b	0.300	0.450	Typical	0.011	0.018	Typical
C	0.150	0.180		0.006	0.007	
D	12.950	13.450		0.510	0.530	
D1	9.900	10.100		0.390	0.398	
D3	8.000	8.000	Reference	0.315	0.315	Reference
E	12.950	13.450		0.510	0.530	
E1	9.900	10.100		0.390	0.398	
E3	8.000	8.000	Reference	0.315	0.315	Reference
e	0.800	0.800		0.031	0.032	
L	0.730	1.030		0.028	0.041	
N	44	44		44	44	
CP	0.102	—		0.004	—	

## E.5 PIC16C7X Family of Devices

	Clock		Memory		Peripherals					Features				
	Maximum Frequency of Operation (MHz)	EPROM Program Memory (Kx4 words)	Data Memory (bytes)	Timer Modules(s)	Capture/Compare/PWM Modules(s)	Serial Ports (SPI/I <sup>2</sup> C, USART)	A/D Converter (8-bit) Channels	Interrupt Sources	I/O Pins	Voltage Range (Volts)	In-Circuit Serial Programming	Brown-out Reset	Packages	
PIC16C710	20	512	36	TMR0	—	—	—	4	4	13	3.0-6.0	Yes	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C71	20	1K	36	TMR0	—	—	—	4	4	13	3.0-6.0	Yes	—	18-pin DIP, SOIC
PIC16C711	20	1K	68	TMR0	—	—	—	4	4	13	3.0-6.0	Yes	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C72	20	2K	128	TMR0, TMR1, TMR2	1 SPI/I <sup>2</sup> C	—	—	5	8	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC, SSOP
PIC16C73	20	4K	192	TMR0, TMR1, TMR2	2 SPI/I <sup>2</sup> C, USART	—	—	5	11	22	3.0-6.0	Yes	—	28-pin SDIP, SOIC
PIC16C73A <sup>(1)</sup>	20	4K	192	TMR0, TMR1, TMR2	2 SPI/I <sup>2</sup> C, USART	—	—	5	11	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC
PIC16C74	20	4K	192	TMR0, TMR1, TMR2	2 SPI/I <sup>2</sup> C, USART	Yes	Yes	8	12	33	3.0-6.0	Yes	—	40-pin DIP; 44-pin PLCC, MQFP
PIC16C74A <sup>(1)</sup>	20	4K	192	TMR0, TMR1, TMR2	2 SPI/I <sup>2</sup> C, USART	Yes	Yes	8	12	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

All PIC16C7X Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.

## PIN COMPATIBILITY

Devices that have the same package type and VDD, Vss and MCLR pin locations are said to be pin compatible. This allows these different devices to operate in the same socket. Compatible devices may only requires minor software modification to allow proper operation in the application socket (ex., PIC16C56 and PIC16C61 devices). Not all devices in the same package size are pin compatible; for example, the PIC16C62 is compatible with the PIC16C63, but not the PIC16C55.

Pin compatibility does not mean that the devices offer the same features. As an example, the PIC16C54 is pin compatible with the PIC16C71, but does not have an A/D converter, weak pull-ups on PORTB, or interrupts.

**TABLE E-1: PIN COMPATIBLE DEVICES**

Pin Compatible Devices	Package
PIC12C508, PIC12C509	8-pin
PIC16C54, PIC16C54A, PIC16CR54A, PIC16C56, PIC16C58A, PIC16CR58A, PIC16C61, PIC16C554, PIC16C556, PIC16C558 PIC16C620, PIC16C621, PIC16C622, PIC16C710, PIC16C71, PIC16C711, PIC16F83, PIC16CR83, PIC16C84, PIC16F84A, PIC16CR84	18-pin 20-pin
PIC16C55, PIC16C57, PIC16CR57B	28-pin
PIC16C62, PIC16CR62, PIC16C62A, PIC16C63, PIC16C72, PIC16C73, PIC16C73A	28-pin
PIC16C64, PIC16CR64, PIC16C64A, PIC16C65, PIC16C65A, PIC16C74, PIC16C74A	40-pin
PIC17C42, PIC17CR42, PIC17C42A, PIC17C43, PIC17CR43, PIC17C44	40-pin
PIC16C923, PIC16C924	64/68-pin

# PIC17C4X

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NOTES: