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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Obsolete
PIC
8-Bit
33MHz
UART/USART
POR, PWM, WDT
33
8KB (4K x 16)
OTP
-
454 x 8
4.5V ~ 6V
-
External
-40°C ~ 125°C (TA)
Through Hole
40-DIP (0.600", 15.24mm)
40-PDIP
https://www.e-xfl.com/product-detail/microchip-technology/pic17c43-33e-p

5.3 <u>Peripheral Interrupt Request Register</u> (PIR)

This register contains the individual flag bits for the peripheral interrupts.

These bits will be set by the specified condition, even if the corresponding interrupt enable bit is cleared (interrupt disabled), or the GLINTD bit is set (all interrupts disabled). Before enabling an interrupt, the user may wish to clear the interrupt flag to ensure that the program does not immediately branch to the peripheral interrupt service routine.

FIGURE 5-4: PIR REGISTER (ADDRESS: 16h, BANK 1)

R/W - (0 R/W - 0 R - 1 R - 0 TMR3IF TMR2IF TMR1IF CA2IF CA1IF TXIF RCIF R = Readable bit
	N/ N/ 11 12
bit7	bit0 W = Writable bit -n = Value at POR reset
bit 7:	RBIF: PORTB Interrupt on Change Flag bit 1 = One of the PORTB inputs changed (Software must end the mismatch condition) 0 = None of the PORTB inputs have changed
bit 6:	TMR3IF: Timer3 Interrupt Flag bit If Capture1 is enabled (CA1/PR3 = 1) 1 = Timer3 overflowed 0 = Timer3 did not overflow
	If Capture1 is disabled (CA1/ $\overline{PR3}$ = 0) 1 = Timer3 value has rolled over to 0000h from equalling the period register (PR3H:PR3L) value 0 = Timer3 value has not rolled over to 0000h from equalling the period register (PR3H:PR3L) value
bit 5:	TMR2IF : Timer2 Interrupt Flag bit 1 = Timer2 value has rolled over to 0000h from equalling the period register (PR2) value 0 = Timer2 value has not rolled over to 0000h from equalling the period register (PR2) value
bit 4:	TMR1IF: Timer1 Interrupt Flag bit If Timer1 is in 8-bit mode (T16 = 0) 1 = Timer1 value has rolled over to 0000h from equalling the period register (PR) value 0 = Timer1 value has not rolled over to 0000h from equalling the period register (PR2) value
	If Timer1 is in 16-bit mode (T16 = 1) 1 = TMR1:TMR2 value has rolled over to 0000h from equalling the period register (PR1:PR2) value 0 = TMR1:TMR2 value has not rolled over to 0000h from equalling the period register (PR1:PR2) value
bit 3:	CA2IF: Capture2 Interrupt Flag bit 1 = Capture event occurred on RB1/CAP2 pin 0 = Capture event did not occur on RB1/CAP2 pin
bit 2:	CA1IF: Capture1 Interrupt Flag bit 1 = Capture event occurred on RB0/CAP1 pin 0 = Capture event did not occur on RB0/CAP1 pin
bit 1:	TXIF: USART Transmit Interrupt Flag bit 1 = Transmit buffer is empty 0 = Transmit buffer is full
bit 0:	RCIF: USART Receive Interrupt Flag bit 1 = Receive buffer is full 0 = Receive buffer is empty

Note:

8.0 HARDWARE MULTIPLIER

All PIC17C4X devices except the PIC17C42, have an 8 x 8 hardware multiplier included in the ALU of the device. By making the multiply a hardware operation, it completes in a single instruction cycle. This is an unsigned multiply that gives a 16-bit result. The result is stored into the 16-bit PRODuct register (PRODH:PRODL). The multiplier does not affect any flags in the ALUSTA register.

Making the 8 x 8 multiplier execute in a single cycle gives the following advantages:

- · Higher computational throughput
- Reduces code size requirements for multiply algorithms

The performance increase allows the device to be used in applications previously reserved for Digital Signal Processors.

Table 8-1 shows a performance comparison between the PIC17C42 and all other PIC17CXX devices, which have the single cycle hardware multiply.

Example 8-1 shows the sequence to do an 8 x 8 unsigned multiply. Only one instruction is required when one argument of the multiply is already loaded in the WREG register.

Example 8-2 shows the sequence to do an 8×8 signed multiply. To account for the sign bits of the arguments, each argument's most significant bit (MSb) is tested and the appropriate subtractions are done.

EXAMPLE 8-1: 8 x 8 MULTIPLY ROUTINE

```
MOVFP ARG1, WREG
MULWF ARG2 ; ARG1 * ARG2 ->
; PRODH:PRODL
```

EXAMPLE 8-2: 8 x 8 SIGNED MULTIPLY ROUTINE

```
ARG1, WREG
MOVFP
        ARG2
MULWF
                   ; ARG1 * ARG2 ->
                   ; PRODH:PRODL
        ARG2, SB
                   ; Test Sign Bit
BTFSC
        PRODH, F
SUBWF
                   ; PRODH = PRODH
                            - ARG1
MOVFP
        ARG2, WREG
BTFSC
        ARG1, SB ; Test Sign Bit
SUBWF
        PRODH, F
                   ; PRODH = PRODH
                            - ARG2
```

TABLE 8-1: PERFORMANCE COMPARISON

Bastina	Davida	Program Memory	OI (M)	Tir	ne
Routine	Device	(Words)	Cycles (Max)	@ 25 MHz	@ 33 MHz
8 x 8 unsigned	PIC17C42	13	69	11.04 μs	N/A
	All other PIC17CXX devices	1	1	160 ns	121 ns
8 x 8 signed	PIC17C42	_	_	_	N/A
	All other PIC17CXX devices	6	6	960 ns	727 ns
16 x 16 unsigned	PIC17C42	21	242	38.72 μs	N/A
	All other PIC17CXX devices	24	24	3.84 µs	2.91 μs
16 x 16 signed	PIC17C42	52	254	40.64 μs	N/A
	All other PIC17CXX devices	36	36	5.76 µs	4.36 μs

Peripheral Data in RBPU (PORTA<7>) Weak Pull-Up Match Signal_ from other, port pins **RBIF** Port Input Latch Data Bus RD_DDRB (Q2) RD_PORTB (Q2) D $\overline{\mathsf{OE}}$ WR_DDRB (Q4) **~**CK D Port Q Data WR_PORTB (Q4) PWM_output PWM_select Note: I/O pins have protection diodes to VDD and Vss.

FIGURE 9-5: **BLOCK DIAGRAM OF RB3 AND RB2 PORT PINS**

Example 9-1 shows the instruction sequence to initialize PORTB. The Bank Select Register (BSR) must be selected to Bank 0 for the port to be initialized.

EXAMPLE 9-1: INITIALIZING PORTB

MOVLB 0 ; Select Bank 0

CLRF PORTB ; Initialize PORTB by clearing

; output data latches

MOVLW 0xCF ; Value used to initialize

; data direction

MOVWF DDRB ; Set RB<3:0> as inputs

RB<5:4> as outputs RB<7:6> as inputs

TABLE 9-3: PORTB FUNCTIONS

Name	Bit	Buffer Type	Function
RB0/CAP1	bit0	ST	Input/Output or the RB0/CAP1 input pin. Software programmable weak pullup and interrupt on change features.
RB1/CAP2	bit1	ST	Input/Output or the RB1/CAP2 input pin. Software programmable weak pullup and interrupt on change features.
RB2/PWM1	bit2	ST	Input/Output or the RB2/PWM1 output pin. Software programmable weak pull-up and interrupt on change features.
RB3/PWM2	bit3	ST	Input/Output or the RB3/PWM2 output pin. Software programmable weak pull-up and interrupt on change features.
RB4/TCLK12	bit4	ST	Input/Output or the external clock input to Timer1 and Timer2. Software programmable weak pull-up and interrupt on change features.
RB5/TCLK3	bit5	ST	Input/Output or the external clock input to Timer3. Software programmable weak pull-up and interrupt on change features.
RB6	bit6	ST	Input/Output pin. Software programmable weak pull-up and interrupt on change features.
RB7	bit7	ST	Input/Output pin. Software programmable weak pull-up and interrupt on change features.

Legend: ST = Schmitt Trigger input.

TABLE 9-4: REGISTERS/BITS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
12h, Bank 0	PORTB	PORTB d	ata latch							xxxx xxxx	uuuu uuuu
11h, Bank 0	DDRB	Data dired	ction registe	er for PORTE	3					1111 1111	1111 1111
10h, Bank 0	PORTA	RBPU		RA5	RA4	RA3	RA2	RA1/T0CKI	RA0/INT	0-xx xxxx	0-uu uuuu
06h, Unbanked	CPUSTA	_	_	STKAV	GLINTD	TO	PD	_	_	11 11	11 qq
07h, Unbanked	INTSTA	PEIF	T0CKIF	TOIF	INTF	PEIE	T0CKIE	TOIE	INTE	0000 0000	0000 0000
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA10VF	PWM2ON	PWM10N	CA1/PR3	TMR3ON	TMR2ON	TMR10N	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = Value depends on condition.

Shaded cells are not used by PORTB.

Note 1: Other (non power-up) resets include: external reset through MCLR and the Watchdog Timer Reset.

14.0 SPECIAL FEATURES OF THE CPU

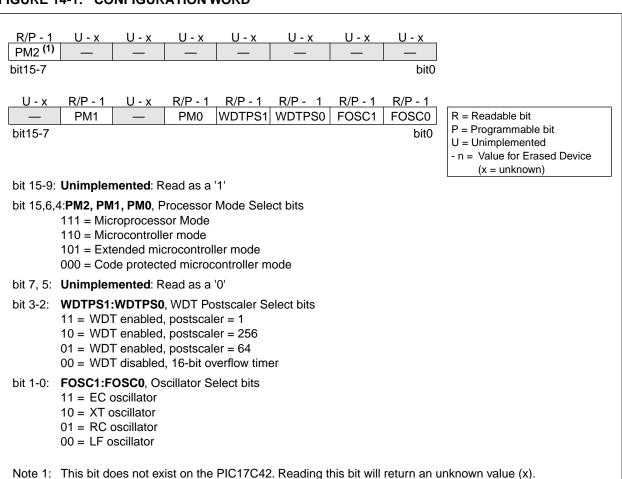
What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC17CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- · OSC selection
- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- · Code protection

The PIC17CXX has a Watchdog Timer which can be shut off only through EPROM bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 96 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake from SLEEP through external reset, Watchdog Timer Reset or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LF crystal option saves power. Configuration bits are used to select various options. This configuration word has the format shown in Figure 14-1.

FIGURE 14-1: CONFIGURATION WORD



MOVFP	Move f to p
Syntax:	[label] MOVFP f,p
Operands:	$0 \le f \le 255$ $0 \le p \le 31$
Operation:	$(f) \rightarrow (p)$
Status Affected:	None
Encoding:	011p pppp ffff ffff
Description:	Move data from data memory location 'f' to data memory location 'p'. Location 'f' can be anywhere in the 256 word data space (00h to FFh) while 'p' can be 00h to 1Fh. Either 'p' or 'f' can be WREG (a useful special situation).
	MOVFP is particularly useful for transfer- ring a data memory location to a periph- eral register (such as the transmit buffer or an I/O port). Both 'f' and 'p' can be indirectly addressed.
Words:	1

Cycles: Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Execute	Write
	register 'f'		register 'p'

Example: MOVFP REG1, REG2

1

Before Instruction

REG1 = 0x33, REG2 = 0x11

After Instruction

REG1 = 0x33, REG2 = 0x33 MOVLB Move Literal to low nibble in BSR

Syntax: [label] MOVLB k

Operands: $0 \le k \le 15$

Operation: $k \rightarrow (BSR<3:0>)$

Status Affected: None

Encoding: 1011 1000 uuuu kkkk

Description: The four bit literal 'k' is loaded in the Bank Select Register (BSR). Only the low 4-bits of the Bank Select Register are affected. The upper half of the BSR is unchanged. The assembler will

encode the "u" fields as '0'.

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'u:k'	Execute	Write literal
			BSR<3:0>

Example: MOVLB 0x5

Before Instruction

BSR register = 0x22

After Instruction

BSR register = 0x25

Note: For the PIC17C42, only the low four bits of the BSR register are physically implemented. The upper nibble is read as '0'.

NOTES:

Applicable Devices 42 R42 42A 43 R43 44

17.1 DC CHARACTERISTICS:

PIC17C42-16 (Commercial, Industrial) PIC17C42-25 (Commercial, Industrial)

			Standard	d Opera	ating C	ondition	ns (unless otherwise stated)
DC CHARA	Operating	g tempe	erature				
DC CHARA	CILINIC	31103				-40°C	≤ TA ≤ +85°C for industrial and
						0°C	≤ Ta ≤ +70°C for commercial
Parameter							
No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	4.5	_	5.5	V	
D002	VDR	RAM Data Retention Voltage (Note 1)	1.5 *	_	_	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	_	Vss	_	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.060*	_	_	mV/ms	See section on Power-on Reset for details
D010	IDD	Supply Current	_	3	6	mA	Fosc = 4 MHz (Note 4)
D011		(Note 2)	_	6	12 *	mA	Fosc = 8 MHz
D012			_	11	24 *	mA	Fosc = 16 MHz
D013			_	19	38	mA	Fosc = 25 MHz
D014			_	95	150	μΑ	Fosc = 32 kHz
							WDT enabled (EC osc configuration)
D020	IPD	Power-down Current	_	10	40	μΑ	VDD = 5.5V, WDT enabled
D021		(Note 3)	_	< 1	5	μΑ	VDD = 5.5V, WDT disabled

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD or Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

Current consumed from the oscillator and I/O's driving external capacitive or resistive loads need to be considered.

For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as: VDD / (2 • R). For capacitive loads, The current can be estimated (for an individual I/O pin) as (CL • VDD) • f

CL = Total capacitive load on the I/O pin; f = average frequency on the I/O pin switches.

The capacitive currents are most significant when the device is configured for external execution (includes extended microcontroller mode).

- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, all I/O pins in hi-impedance state and tied to VDD or Vss.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

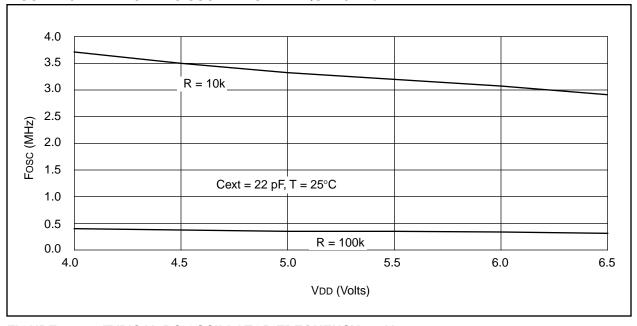


FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

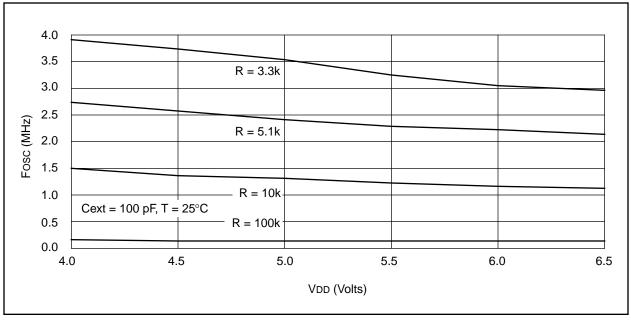


FIGURE 18-13: WDT TIMER TIME-OUT PERIOD vs. VDD

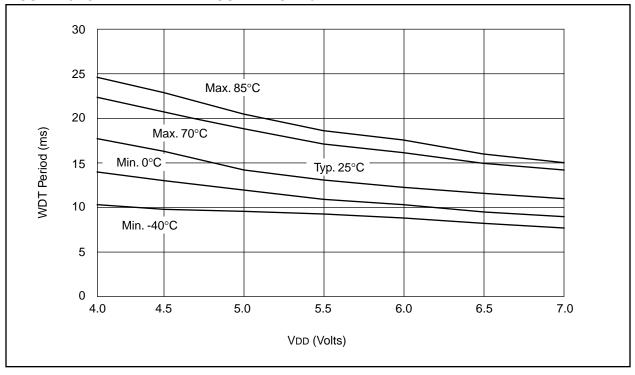


FIGURE 18-14: IOH vs. VOH, VDD = 3V

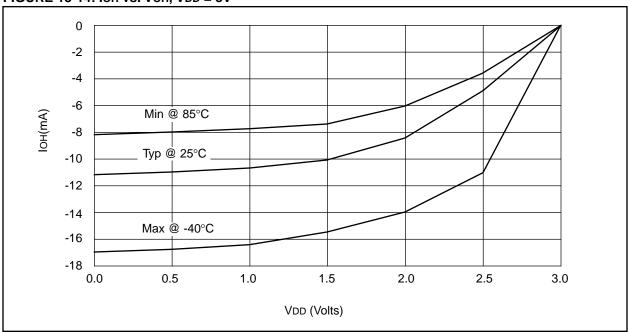


FIGURE 18-15: IOH vs. VOH, VDD = 5V

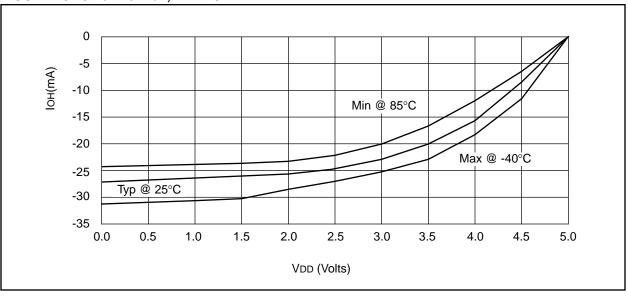
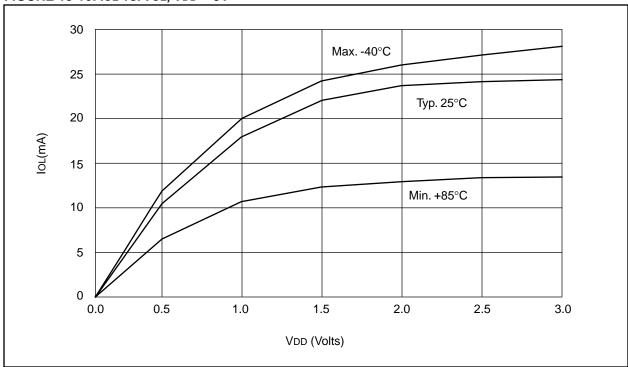


FIGURE 18-16: IOL vs. VOL, VDD = 3V



Applicable Devices 42 R42 42A 43 R43 44

FIGURE 18-17: IoL vs. Vol, VDD = 5V

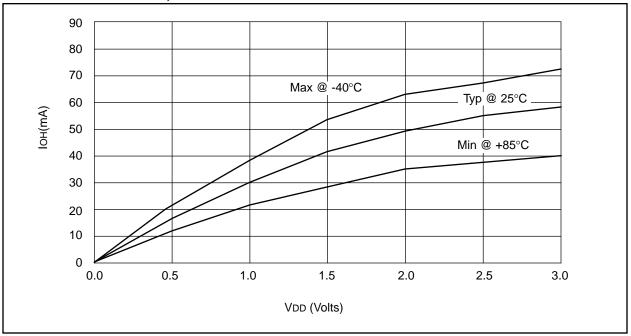
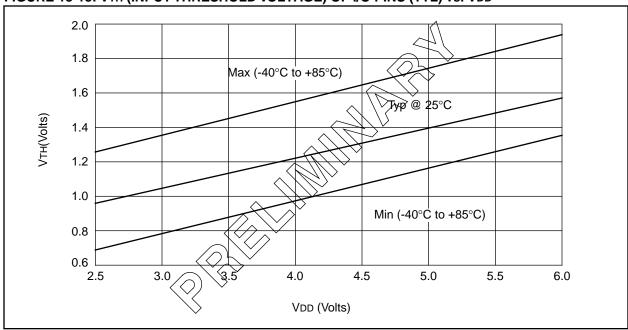


FIGURE 18-18: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS (TTL) VS. VDD



NOTES:

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FIGURE 19-12: MEMORY INTERFACE READ TIMING (NOT SUPPORTED IN PIC17LC4X DEVICES)

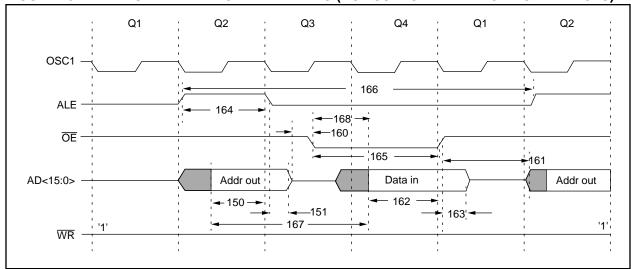


TABLE 19-12: MEMORY INTERFACE READ REQUIREMENTS (NOT SUPPORTED IN PIC17LC4X DEVICES)

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
150	TadV2alL	AD15:AD0 (address) valid to ALE↓ (address setup time)	0.25Tcy - 10	_	_	ns	
151	TalL2adl	ALE↓ to address out invalid (address hold time)	5*	_	_	ns	
160	TadZ2oeL	AD15:AD0 hi-impedance to OE ↓	0*	_	_	ns	
161	ToeH2adD	OE↑ to AD15:AD0 driven	0.25Tcy - 15	_	_	ns	
162	162 TadV2oeH Data in valid before OE ↑ (data setup time)		35	_	_	ns	
163	ToeH2adl	OE↑to data in invalid (data hold time)	0	_	_	ns	
164	TalH	ALE pulse width	_	0.25Tcy §	_	ns	
165	ToeL	OE pulse width	0.5Tcy - 35 §	_	_	ns	
166	TalH2alH	ALE↑ to ALE↑(cycle time)	_	Tcy §	_	ns	
167	Tacc	Address access time	_	_	0.75Tcy - 30	ns	
168	Toe	Output enable access time (OE low to Data Valid)	_	_	0.5Tcy - 45	ns	

^{*} These parameters are characterized but not tested.

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

[§] This specification ensured by design.

FIGURE 20-5: TRANSCONDUCTANCE (gm) OF LF OSCILLATOR vs. VDD

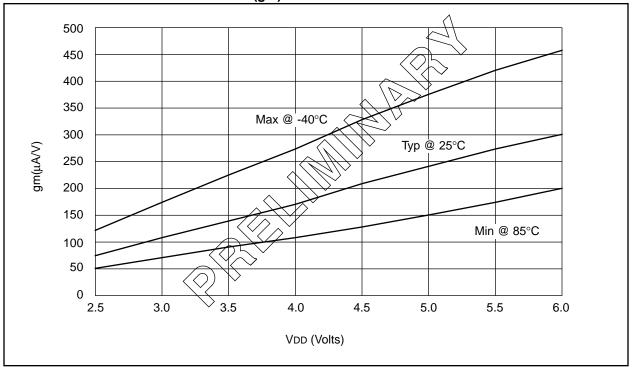
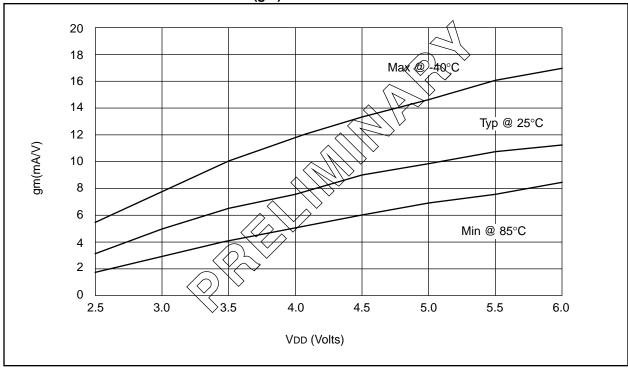


FIGURE 20-6: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD



PIC16CXXX Family of Devices E.3

				Clock	Memory	lory	$ \downarrow $	Perip	Peripherals	\rightarrow	Features
			Tollege	Tours done le					One of		
		Vig.	8 6 TO TO	W 1+)	(§. 1)			ON BOUG			to signature of the sig
	TON	College Book of the College of the C	10	TOON TOUTON ERC	ALDOW SOUTH	* Ruleilli	To letter	Suid Of Religion	SUL SUL	(16 00 14 OC)	Secretary Mounote Selos
PIC16C554	20	512	80	TMR0			3	13	2.5-6.0		18-pin DIP, SOIC; 20-pin SSOP
PIC16C556	20	,	80	TMR0	I	I	3	13	2.5-6.0	ı	18-pin DIP, SOIC; 20-pin SSOP
PIC16C558	20	2K	128	TMR0	ı	I	3	13	2.5-6.0	I	18-pin DIP, SOIC; 20-pin SSOP
PIC16C620	20	512	80	TMR0	2	Yes	4	13	2.5-6.0	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C621	20	*	80	TMR0	2	Yes	4	13	2.5-6.0	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C622	20	2K	128	TMR0	2	Yes	4	13	2.5-6.0	Yes	18-pin DIP, SOIC; 20-pin SSOP
AII DIC16/17		oivo o viio	0,0400	Doug	Pose+	20000	N olde	Jodoto,	Timor	10000	Ermily devised bours on Deast colonatable Westchard Times colonatable and and bigh I/O

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

All PIC16C6XXX Family devices use serial programming with clock pin RB6 and data pin RB7.

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nitializing PORTC		INTEDG	
nitializing PORTD		Interrupt on Change Feature	, -
nitializing PORTE		Interrupt Status Register (INTSTA)	
nstruction Flow/Pipelining		Interrupt Status Register (INTSTA)	22
		•	07
nstruction Set		Context Saving	∠۱
ADDLW		Flag bits	0.4
ADDWF		TMR1IE	
ADDWFC	113	TMR1IF	
ANDLW	113	TMR2IE	21
ANDWF	114	TMR2IF	21
BCF	114	TMR3IE	21
BSF	115	TMR3IF	21
BTFSC	115	Interrupts	21
BTFSS		Logic	
BTG		Operation	
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		IORLW	
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LCALL		IORWF	125
MOVFP			
MOVLB	_	L	
MOVLR		-	
MOVLW	127	LCALL	126
MOVPF	128		
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MULWF	129	М	
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