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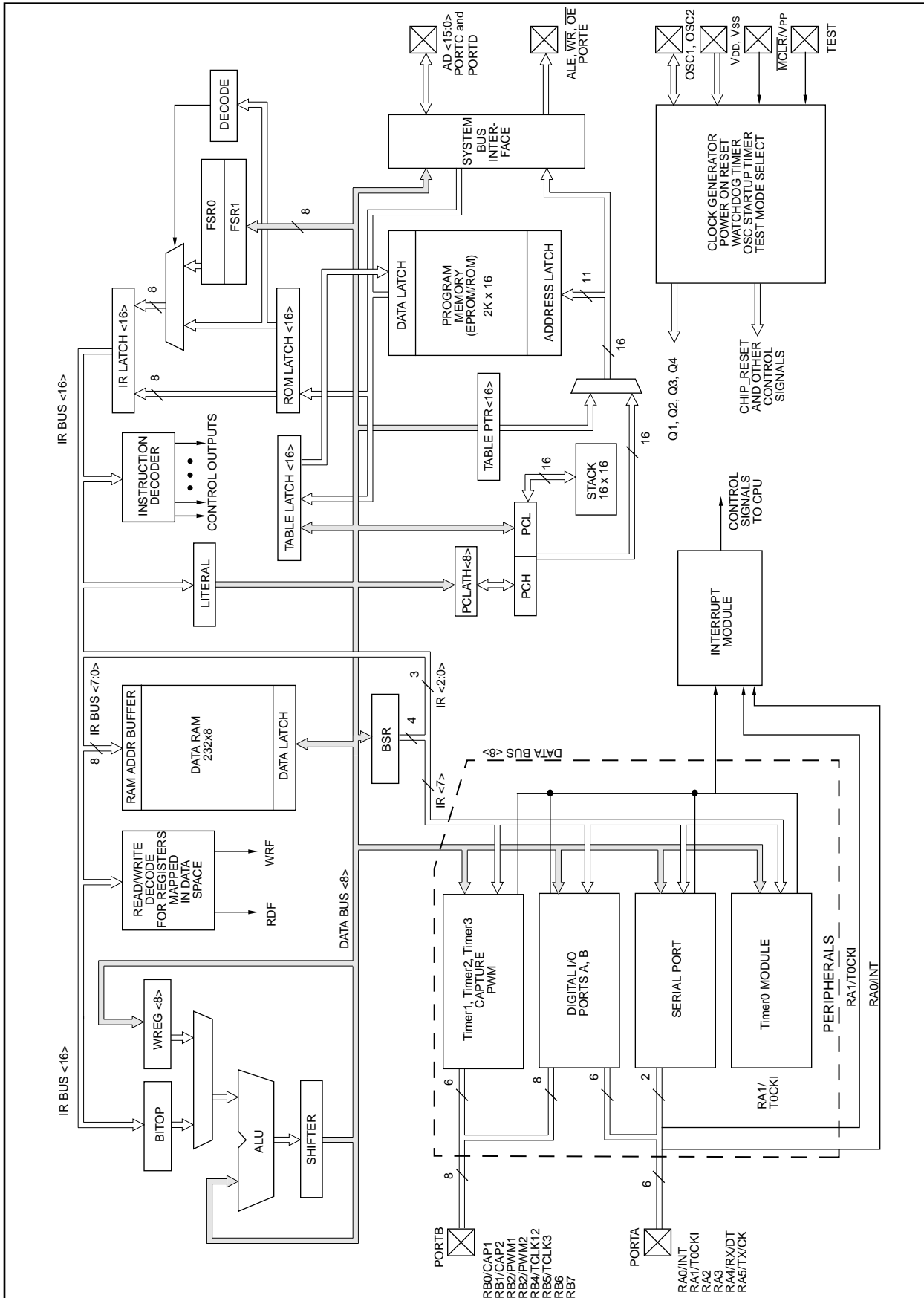
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	33
Program Memory Size	8KB (4K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	454 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic17c43t-16i-l">https://www.e-xfl.com/product-detail/microchip-technology/pic17c43t-16i-l</a>

FIGURE 3-1: PIC17C42 BLOCK DIAGRAM



# PIC17C4X

**TABLE 3-1: PINOUT DESCRIPTIONS**

Name	DIP No.	PLCC No.	QFP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	19	21	37	I	ST	Oscillator input in crystal/resonator or RC oscillator mode. External clock input in external clock mode.
OSC2/CLKOUT	20	22	38	O	—	Oscillator output. Connects to crystal or resonator in crystal oscillator mode. In RC oscillator or external clock modes OSC2 pin outputs CLKOUT which has one fourth the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/VPP	32	35	7	I/P	ST	Master clear (reset) input/Programming Voltage (VPP) input. This is the active low reset input to the chip.
RA0/INT	26	28	44	I	ST	<p>PORTA is a bi-directional I/O Port except for RA0 and RA1 which are input only.</p> <p>RA0/INT can also be selected as an external interrupt input. Interrupt can be configured to be on positive or negative edge.</p> <p>RA1/T0CKI can also be selected as an external interrupt input, and the interrupt can be configured to be on positive or negative edge. RA1/T0CKI can also be selected to be the clock input to the Timer0 timer/counter.</p> <p>High voltage, high current, open drain input/output port pins.</p> <p>High voltage, high current, open drain input/output port pins.</p> <p>RA4/RX/DT can also be selected as the USART (SCI) Asynchronous Receive or USART (SCI) Synchronous Data.</p> <p>RA5/TX/CK can also be selected as the USART (SCI) Asynchronous Transmit or USART (SCI) Synchronous Clock.</p>
RA1/T0CKI	25	27	43	I	ST	
RA2	24	26	42	I/O	ST	
RA3	23	25	41	I/O	ST	
RA4/RX/DT	22	24	40	I/O	ST	
RA5/TX/CK	21	23	39	I/O	ST	
RB0/CAP1	11	13	29	I/O	ST	<p>PORTB is a bi-directional I/O Port with software configurable weak pull-ups.</p> <p>RB0/CAP1 can also be the CAP1 input pin.</p> <p>RB1/CAP2 can also be the CAP2 input pin.</p> <p>RB2/PWM1 can also be the PWM1 output pin.</p> <p>RB3/PWM2 can also be the PWM2 output pin.</p> <p>RB4/TCLK12 can also be the external clock input to Timer1 and Timer2.</p> <p>RB5/TCLK3 can also be the external clock input to Timer3.</p>
RB1/CAP2	12	14	30	I/O	ST	
RB2/PWM1	13	15	31	I/O	ST	
RB3/PWM2	14	16	32	I/O	ST	
RB4/TCLK12	15	17	33	I/O	ST	
RB5/TCLK3	16	18	34	I/O	ST	
RB6	17	19	35	I/O	ST	
RB7	18	20	36	I/O	ST	
RC0/AD0	2	3	19	I/O	TTL	<p>PORTC is a bi-directional I/O Port.</p> <p>This is also the lower half of the 16-bit wide system bus in microprocessor mode or extended microcontroller mode. In multiplexed system bus configuration, these pins are address output as well as data input or output.</p>
RC1/AD1	3	4	20	I/O	TTL	
RC2/AD2	4	5	21	I/O	TTL	
RC3/AD3	5	6	22	I/O	TTL	
RC4/AD4	6	7	23	I/O	TTL	
RC5/AD5	7	8	24	I/O	TTL	
RC6/AD6	8	9	25	I/O	TTL	
RC7/AD7	9	10	26	I/O	TTL	

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input.

## 4.0 RESET

The PIC17CXX differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$  reset during normal operation
- WDT Reset (normal operation)

Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are forced to a "reset state" on Power-on Reset (POR), on  $\overline{\text{MCLR}}$  or WDT Reset and on  $\overline{\text{MCLR}}$  reset during SLEEP. They are not affected by a WDT Reset during SLEEP, since this reset is viewed as the resumption of normal operation. The  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits are set or cleared differently in different reset situations as indicated in Table 4-3. These bits are used in software to determine the nature of reset. See Table 4-4 for a full description of reset states of all registers.

**Note:** While the device is in a reset state, the internal phase clock is held in the Q1 state. Any processor mode that allows external execution will force the RE0/ALE pin as a low output and the RE1/ $\overline{\text{OE}}$  and RE2/ $\overline{\text{WR}}$  pins as high outputs.

A simplified block diagram of the on-chip reset circuit is shown in Figure 4-1.

## 4.1 Power-on Reset (POR), Power-up Timer (PWRT), and Oscillator Start-up Timer (OST)

### 4.1.1 POWER-ON RESET (POR)

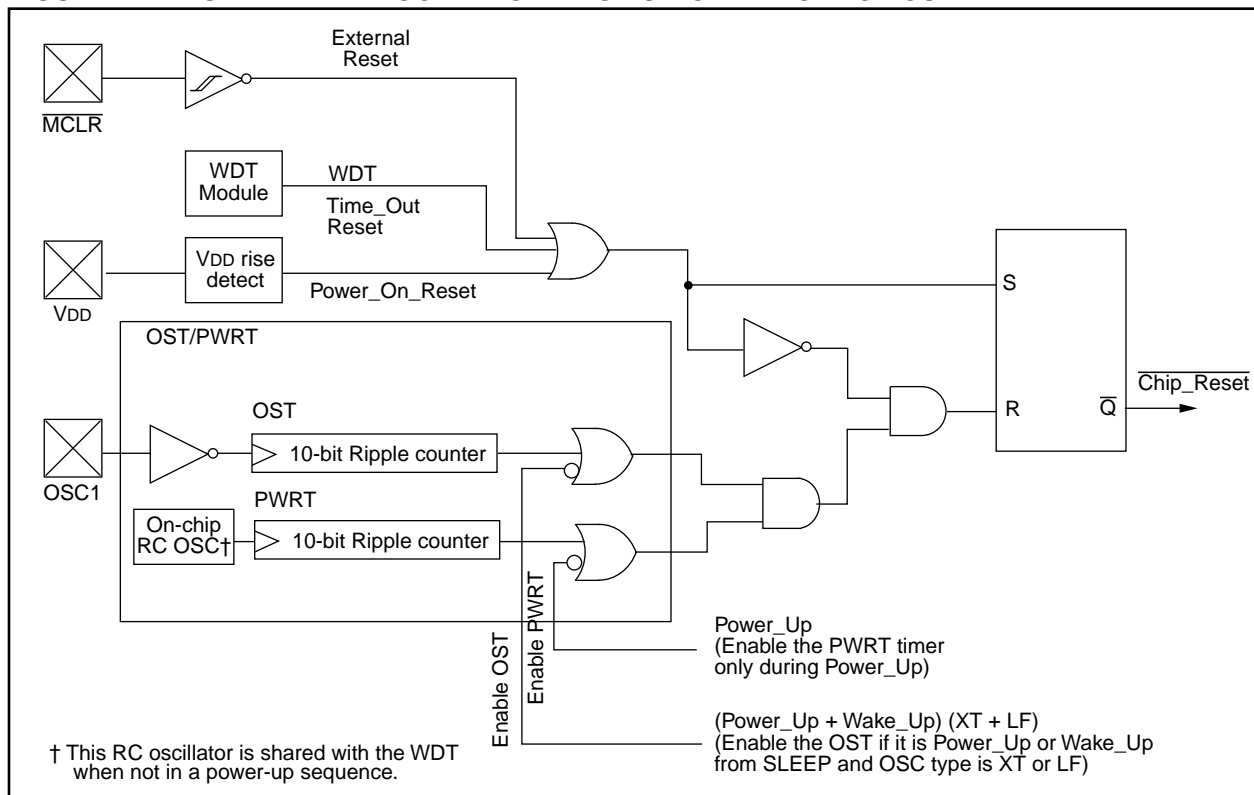
The Power-on Reset circuit holds the device in reset until  $V_{DD}$  is above the trip point (in the range of 1.4V - 2.3V). The PIC17C42 does not produce an internal reset when  $V_{DD}$  declines. All other devices will produce an internal reset for both rising and falling  $V_{DD}$ . To take advantage of the POR, just tie the  $\overline{\text{MCLR}}/\text{VPP}$  pin directly (or through a resistor) to  $V_{DD}$ . This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for  $V_{DD}$  is required. See Electrical Specifications for details.

### 4.1.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 96 ms time-out (nominal) on power-up. This occurs from rising edge of the POR signal and after the first rising edge of  $\overline{\text{MCLR}}$  (detected high). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. In most cases the PWRT delay allows the  $V_{DD}$  to rise to an acceptable level.

The power-up time delay will vary from chip to chip and to  $V_{DD}$  and temperature. See DC parameters for details.

**FIGURE 4-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**



## 6.2.2.1 ALU STATUS REGISTER (ALUSTA)

The ALUSTA register contains the status bits of the Arithmetic and Logic Unit and the mode control bits for the indirect addressing register.

As with all the other registers, the ALUSTA register can be the destination for any instruction. If the ALUSTA register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Therefore, the result of an instruction with the ALUSTA register as destination may be different than intended.

For example, `CLRF ALUSTA` will clear the upper four bits and set the Z bit. This leaves the ALUSTA register as 0000u1uu (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions be used to alter the ALUSTA register because these instructions do not affect any status bit. To see how other instructions affect the status bits, see the "Instruction Set Summary."

**Note 1:** The C and DC bits operate as a borrow out bit in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

**Note 2:** The overflow bit will be set if the 2's complement result exceeds +127 or is less than -128.

Arithmetic and Logic Unit (ALU) is capable of carrying out arithmetic or logical operations on two operands or a single operand. All single operand instructions operate either on the WREG register or a file register. For two operand instructions, one of the operands is the WREG register and the other one is either a file register or an 8-bit immediate constant.

**FIGURE 6-7: ALUSTA REGISTER (ADDRESS: 04h, UNBANKED)**

R/W - 1	R/W - 1	R/W - 1	R/W - 1	R/W - x	R/W - x	R/W - x	R/W - x
FS3	FS2	FS1	FS0	OV	Z	DC	C
bit7							bit0

R = Readable bit  
W = Writable bit  
-n = Value at POR reset  
(x = unknown)

bit 7-6: **FS3:FS2:** FSR1 Mode Select bits  
 00 = Post auto-decrement FSR1 value  
 01 = Post auto-increment FSR1 value  
 1x = FSR1 value does not change

bit 5-4: **FS1:FS0:** FSR0 Mode Select bits  
 00 = Post auto-decrement FSR0 value  
 01 = Post auto-increment FSR0 value  
 1x = FSR0 value does not change

bit 3: **OV:** Overflow bit  
 This bit is used for signed arithmetic (2's complement). It indicates an overflow of the 7-bit magnitude, which causes the sign bit (bit7) to change state.  
 1 = Overflow occurred for signed arithmetic, (in this arithmetic operation)  
 0 = No overflow occurred

bit 2: **Z:** Zero bit  
 1 = The result of an arithmetic or logic operation is zero  
 0 = The results of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/borrow bit  
 For `ADDWF` and `ADDLW` instructions.  
 1 = A carry-out from the 4th low order bit of the result occurred  
 0 = No carry-out from the 4th low order bit of the result  
 Note: For borrow the polarity is reversed.

bit 0: **C:** carry/borrow bit  
 For `ADDWF` and `ADDLW` instructions.  
 1 = A carry-out from the most significant bit of the result occurred  
 Note that a subtraction is executed by adding the two's complement of the second operand. For rotate (`RRCF`, `RLCF`) instructions, this bit is loaded with either the high or low order bit of the source register.  
 0 = No carry-out from the most significant bit of the result  
 Note: For borrow the polarity is reversed.

# PIC17C4X

## 6.2.2.3 TMR0 STATUS/CONTROL REGISTER (T0STA)

This register contains various control bits. Bit7 (INTEDG) is used to control the edge upon which a signal on the RA0/INT pin will set the RB0/INT interrupt flag. The other bits configure the Timer0 prescaler and clock source. (Figure 11-1).

**FIGURE 6-9: T0STA REGISTER (ADDRESS: 05h, UNBANKED)**

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	U - 0
INTEDG	T0SE	T0CS	PS3	PS2	PS1	PS0	—
bit7							bit0

R = Readable bit  
W = Writable bit  
U = Unimplemented, reads as '0'  
-n = Value at POR reset

bit 7: **INTEDG:** RA0/INT Pin Interrupt Edge Select bit  
This bit selects the edge upon which the interrupt is detected.  
1 = Rising edge of RA0/INT pin generates interrupt  
0 = Falling edge of RA0/INT pin generates interrupt

bit 6: **T0SE:** Timer0 Clock Input Edge Select bit  
This bit selects the edge upon which TMR0 will increment.  
When T0CS = 0  
1 = Rising edge of RA1/T0CKI pin increments TMR0 and/or generates a T0CKIF interrupt  
0 = Falling edge of RA1/T0CKI pin increments TMR0 and/or generates a T0CKIF interrupt  
When T0CS = 1  
Don't care

bit 5: **T0CS:** Timer0 Clock Source Select bit  
This bit selects the clock source for Timer0.  
1 = Internal instruction clock cycle (TCY)  
0 = T0CKI pin

bit 4-1: **PS3:PS0:** Timer0 Prescale Selection bits  
These bits select the prescale value for Timer0.

PS3:PS0	Prescale Value
0000	1:1
0001	1:2
0010	1:4
0011	1:8
0100	1:16
0101	1:32
0110	1:64
0111	1:128
1xxx	1:256

bit 0: **Unimplemented:** Read as '0'

Example 9-1 shows the instruction sequence to initialize PORTB. The Bank Select Register (BSR) must be selected to Bank 0 for the port to be initialized.

## EXAMPLE 9-1: INITIALIZING PORTB

```
MOVLB 0      ; Select Bank 0
CLRF  PORTB  ; Initialize PORTB by clearing
              ; output data latches
MOVLW 0xCF   ; Value used to initialize
              ; data direction
MOVWF DDRB   ; Set RB<3:0> as inputs
              ; RB<5:4> as outputs
              ; RB<7:6> as inputs
```

**TABLE 9-3: PORTB FUNCTIONS**

Name	Bit	Buffer Type	Function
RB0/CAP1	bit0	ST	Input/Output or the RB0/CAP1 input pin. Software programmable weak pull-up and interrupt on change features.
RB1/CAP2	bit1	ST	Input/Output or the RB1/CAP2 input pin. Software programmable weak pull-up and interrupt on change features.
RB2/PWM1	bit2	ST	Input/Output or the RB2/PWM1 output pin. Software programmable weak pull-up and interrupt on change features.
RB3/PWM2	bit3	ST	Input/Output or the RB3/PWM2 output pin. Software programmable weak pull-up and interrupt on change features.
RB4/TCLK12	bit4	ST	Input/Output or the external clock input to Timer1 and Timer2. Software programmable weak pull-up and interrupt on change features.
RB5/TCLK3	bit5	ST	Input/Output or the external clock input to Timer3. Software programmable weak pull-up and interrupt on change features.
RB6	bit6	ST	Input/Output pin. Software programmable weak pull-up and interrupt on change features.
RB7	bit7	ST	Input/Output pin. Software programmable weak pull-up and interrupt on change features.

Legend: ST = Schmitt Trigger input.

**TABLE 9-4: REGISTERS/BITS ASSOCIATED WITH PORTB**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
12h, Bank 0	PORTB	PORTB data latch								xxxx xxxx	uuuu uuuu
11h, Bank 0	DDRB	Data direction register for PORTB								1111 1111	1111 1111
10h, Bank 0	PORTA	RBPU	—	RA5	RA4	RA3	RA2	RA1/T0CKI	RA0/INT	0-xx xxxx	0-uu uuuu
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	T0	PD	—	—	--11 11--	--11 qq--
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/PR3	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = Value depends on condition.

Shaded cells are not used by PORTB.

Note 1: Other (non power-up) resets include: external reset through  $\overline{\text{MCLR}}$  and the Watchdog Timer Reset.

## 9.4.1 PORTE AND DDRE REGISTER

PORTE is a 3-bit bi-directional port. The corresponding data direction register is DDRE. A '1' in DDRE configures the corresponding port pin as an input. A '0' in the DDRE register configures the corresponding port pin as an output. Reading PORTE reads the status of the pins, whereas writing to it will write to the port latch. PORTE is multiplexed with the system bus. When operating as the system bus, PORTE contains the control signals for the address/data bus (AD15:AD0). These control signals are Address Latch Enable (ALE), Output Enable ( $\overline{OE}$ ), and Write ( $\overline{WR}$ ). The control signals  $\overline{OE}$  and  $\overline{WR}$  are active low signals. The timing for the system bus is shown in the Electrical Characteristics section.

**Note:** This port is configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O.

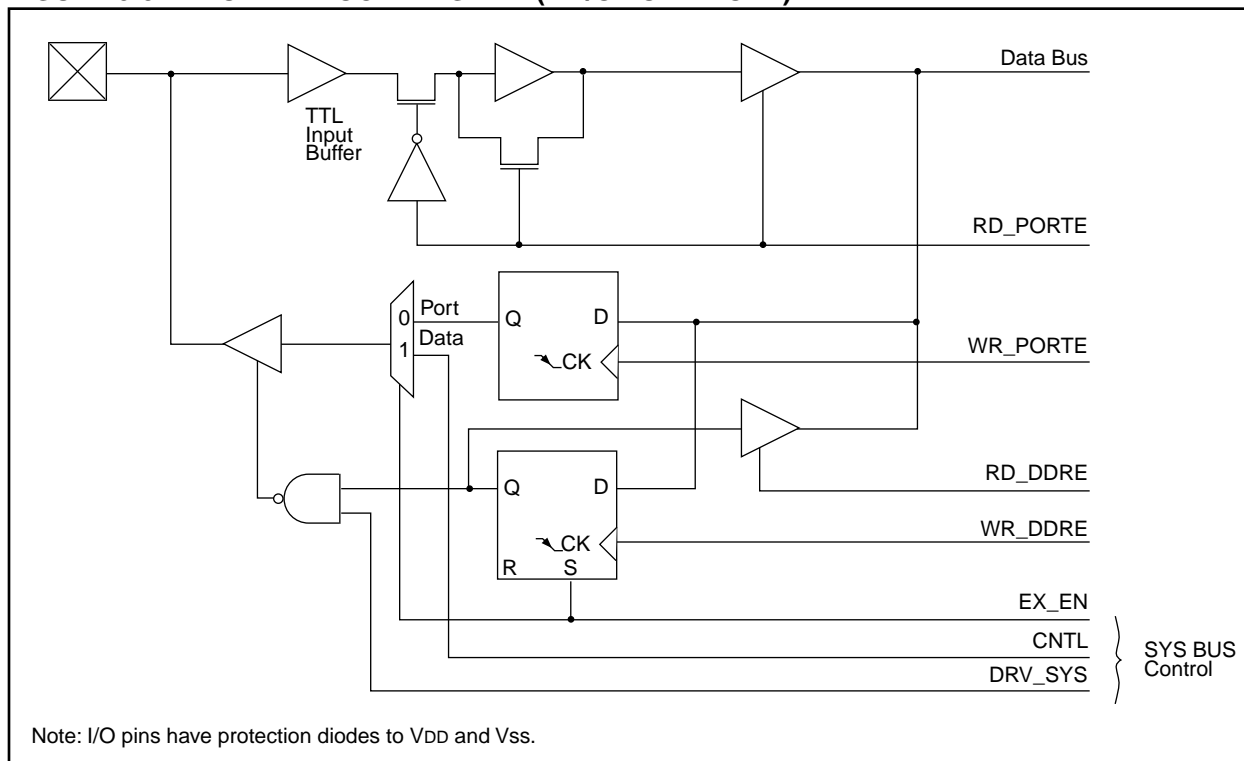
Example 9-4 shows the instruction sequence to initialize PORTE. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

### EXAMPLE 9-4: INITIALIZING PORTE

```

MOVLB 1           ; Select Bank 1
CLRF  PORTE       ; Initialize PORTE data
                  ; latches before setting
                  ; the data direction
                  ; register
MOVLW 0x03        ; Value used to initialize
                  ; data direction
MOVWF DDRE        ; Set RE<1:0> as inputs
                  ; RE<2> as outputs
                  ; RE<7:3> are always
                  ; read as '0'
    
```

**FIGURE 9-8: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)**





## 10.0 OVERVIEW OF TIMER RESOURCES

The PIC17C4X has four timer modules. Each module can generate an interrupt to indicate that an event has occurred. These timers are called:

- Timer0 - 16-bit timer with programmable 8-bit prescaler
- Timer1 - 8-bit timer
- Timer2 - 8-bit timer
- Timer3 - 16-bit timer

For enhanced time-base functionality, two input Captures and two Pulse Width Modulation (PWM) outputs are possible. The PWMs use the TMR1 and TMR2 resources and the input Captures use the TMR3 resource.

### 10.1 Timer0 Overview

The Timer0 module is a simple 16-bit overflow counter. The clock source can be either the internal system clock ( $F_{osc}/4$ ) or an external clock.

The Timer0 module also has a programmable prescaler option. The PS3:PS0 bits (T0STA<4:1>) determine the prescaler value. TMR0 can increment at the following rates: 1:1, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, 1:256.

When Timer0's clock source is an external clock, the Timer0 module can be selected to increment on either the rising or falling edge.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher than the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

### 10.2 Timer1 Overview

The Timer1 module is an 8-bit timer/counter with an 8-bit period register (PR1). When the TMR1 value rolls over from the period match value to 0h, the TMR1IF flag is set, and an interrupt will be generated when enabled. In counter mode, the clock comes from the RB4/TCLK12 pin, which can also be selected to be the clock for the Timer2 module.

TMR1 can be concatenated to TMR2 to form a 16-bit timer. The TMR1 register is the LSB and TMR2 is the MSB. When in the 16-bit timer mode, there is a corresponding 16-bit period register (PR2:PR1). When the TMR2:TMR1 value rolls over from the period match value to 0h, the TMR1IF flag is set, and an interrupt will be generated when enabled.

### 10.3 Timer2 Overview

The TMR2 module is an 8-bit timer/counter with an 8-bit period register (PR2). When the TMR2 value rolls over from the period match value to 0h, the TMR2IF flag is set, and an interrupt will be generated when enabled. In counter mode, the clock comes from the RB4/TCLK12 pin, which can also be selected to be the clock for the TMR1 module.

TMR1 can be concatenated to TMR2 to form a 16-bit timer. The TMR2 register is the MSB and TMR1 is the LSB. When in the 16-bit timer mode, there is a corresponding 16-bit period register (PR2:PR1). When the TMR2:TMR1 value rolls over from the period match value to 0h, the TMR1IF flag is set, and an interrupt will be generated when enabled.

### 10.4 Timer3 Overview

The Timer3 module is a 16-bit timer/counter with a 16-bit period register. When the TMR3H:TMR3L value rolls over to 0h, the TMR3IF bit is set and an interrupt will be generated when enabled. In counter mode, the clock comes from the RB5/TCLK3 pin.

When operating in the dual capture mode, the period registers become the second 16-bit capture register.

### 10.5 Role of the Timer/Counters

The timer modules are general purpose, but have dedicated resources associated with them. Timer1 and Timer2 are the time-bases for the two Pulse Width Modulation (PWM) outputs, while Timer3 is the time-base for the two input captures.

NOTES:

TABLE 13-7:    REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
13h, Bank 0	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
16h, Bank 0	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	xxxx xxxx	uuuu uuuu
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 0	SPBRG	Baud rate generator register								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used for synchronous master transmission.  
Note 1: Other (non power-up) resets include: external reset through  $\overline{\text{MCLR}}$  and Watchdog Timer Reset.

FIGURE 13-9:    SYNCHRONOUS TRANSMISSION

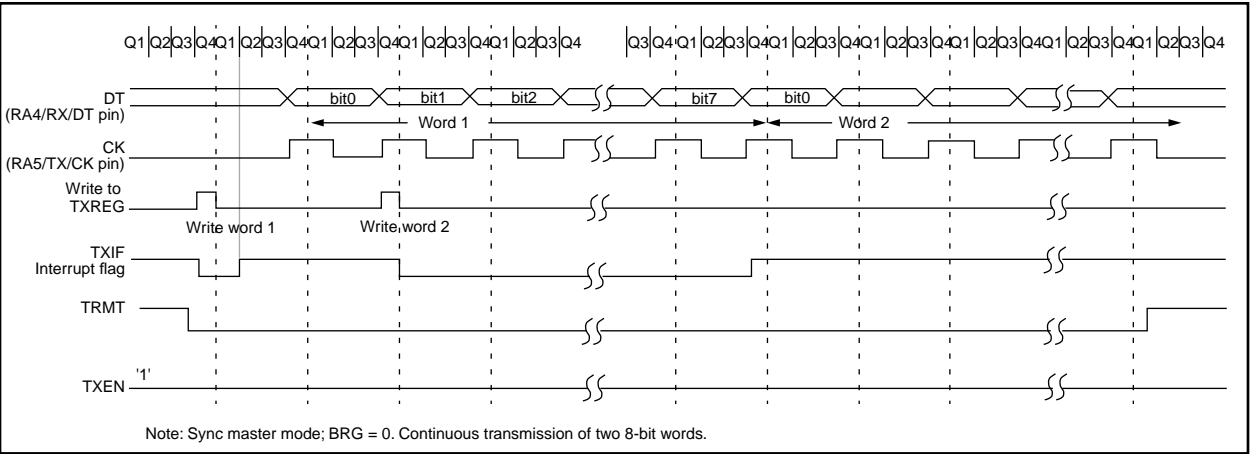
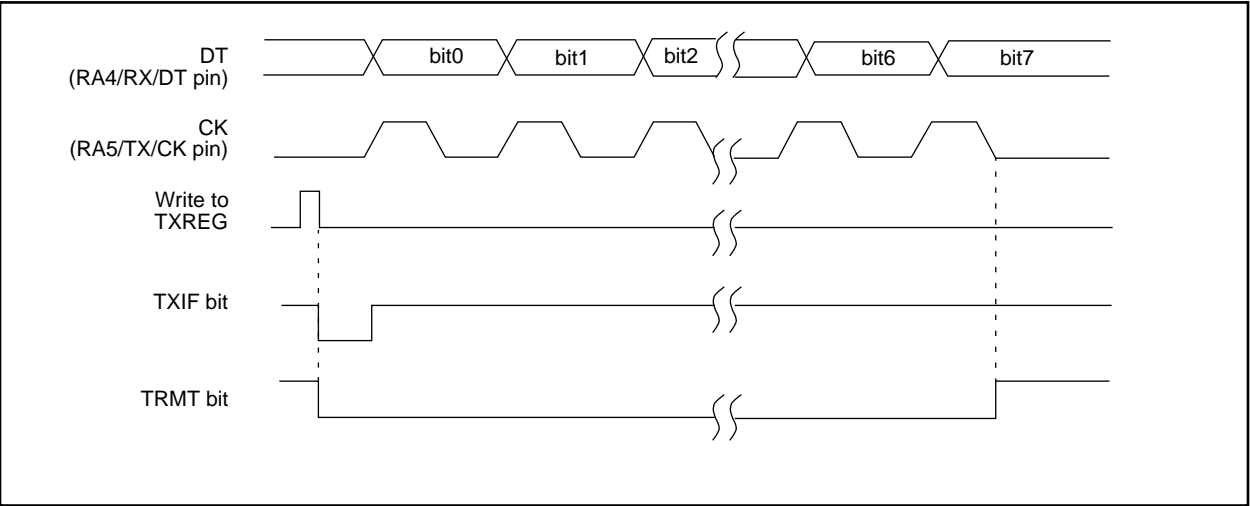


FIGURE 13-10: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



**TABLE 13-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
13h, Bank 0	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
16h, Bank 0	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	xxxx xxxx	uuuu uuuu
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 0	SPBRG	Baud rate generator register								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used for synchronous slave transmission.

Note 1: Other (non power-up) resets include: external reset through  $\overline{\text{MCLR}}$  and Watchdog Timer Reset.

**TABLE 13-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
13h, Bank0	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
14h, Bank0	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	xxxx xxxx	uuuu uuuu
17h, Bank1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank0	SPBRG	Baud rate generator register								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used for synchronous slave reception.

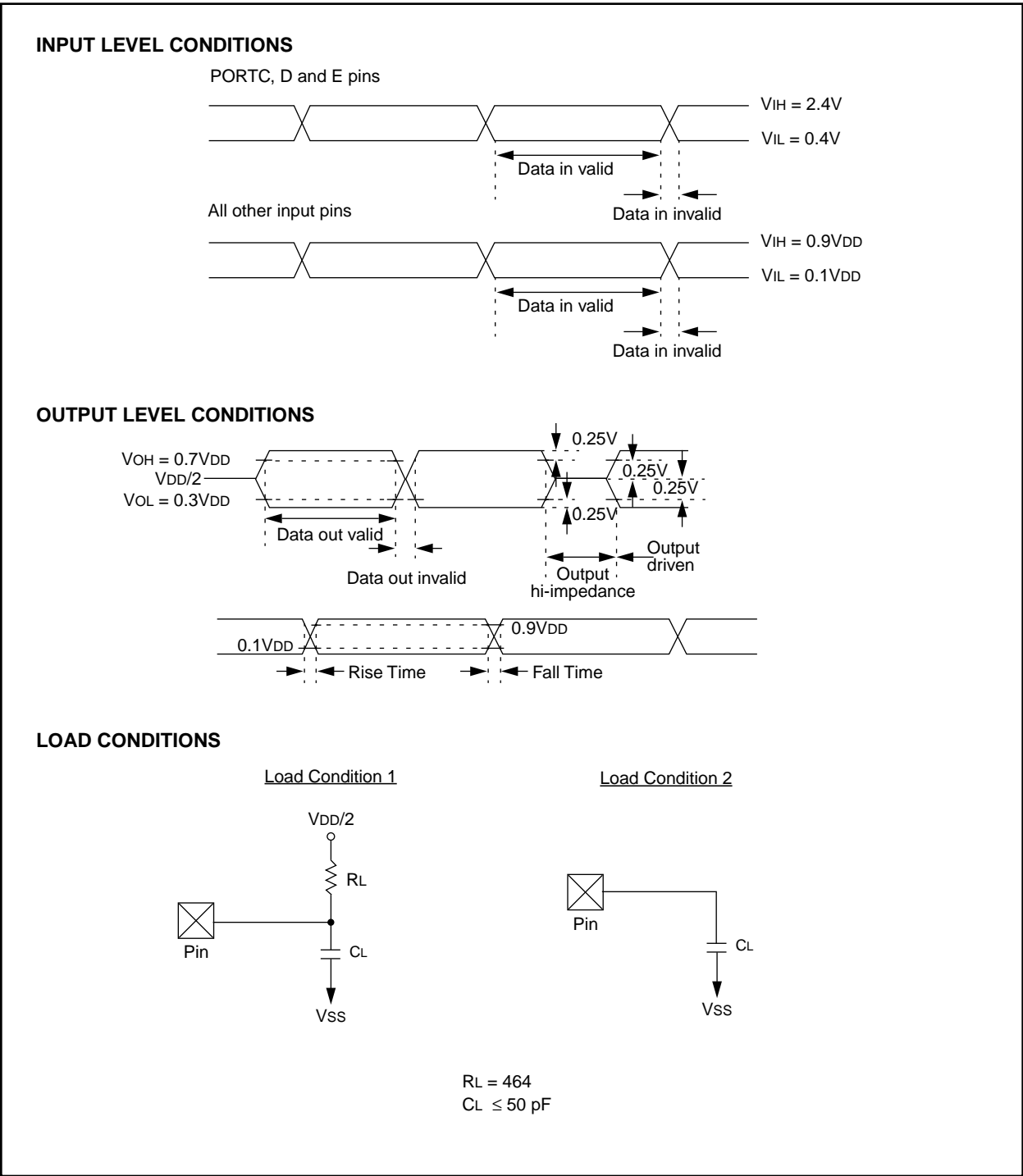
Note 1: Other (non power-up) resets include: external reset through  $\overline{\text{MCLR}}$  and Watchdog Timer Reset.

# PIC17C4X

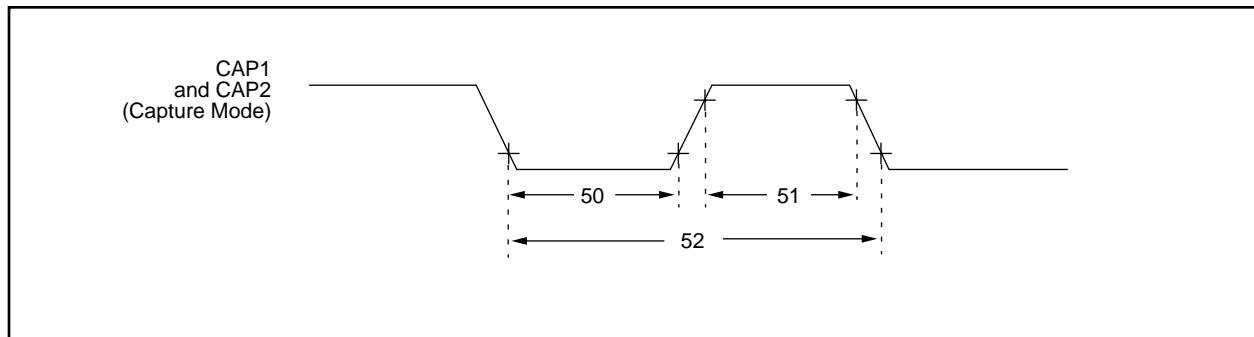
Applicable Devices 42 R42 42A 43 R43 44

FIGURE 17-1: PARAMETER MEASUREMENT INFORMATION

All timings are measure between high and low measurement points as indicated in the figures below.



**FIGURE 17-7: CAPTURE TIMINGS**



**TABLE 17-7: CAPTURE REQUIREMENTS**

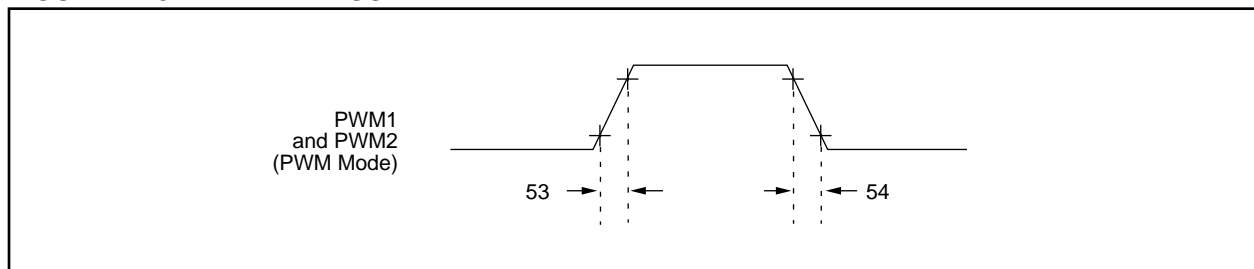
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
50	TccL	Capture1 and Capture2 input low time	10 *	—	—	ns	
51	TccH	Capture1 and Capture2 input high time	10 *	—	—	ns	
52	TccP	Capture1 and Capture2 input period	$\frac{2 T_{CY}}{N}$ §	—	—	ns	N = prescale value (4 or 16)

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

**FIGURE 17-8: PWM TIMINGS**



**TABLE 17-8: PWM REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
53	TccR	PWM1 and PWM2 output rise time	—	10 *	35 *§	ns	
54	TccF	PWM1 and PWM2 output fall time	—	10 *	35 *§	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

## 18.0 PIC17C42 DC AND AC CHARACTERISTICS

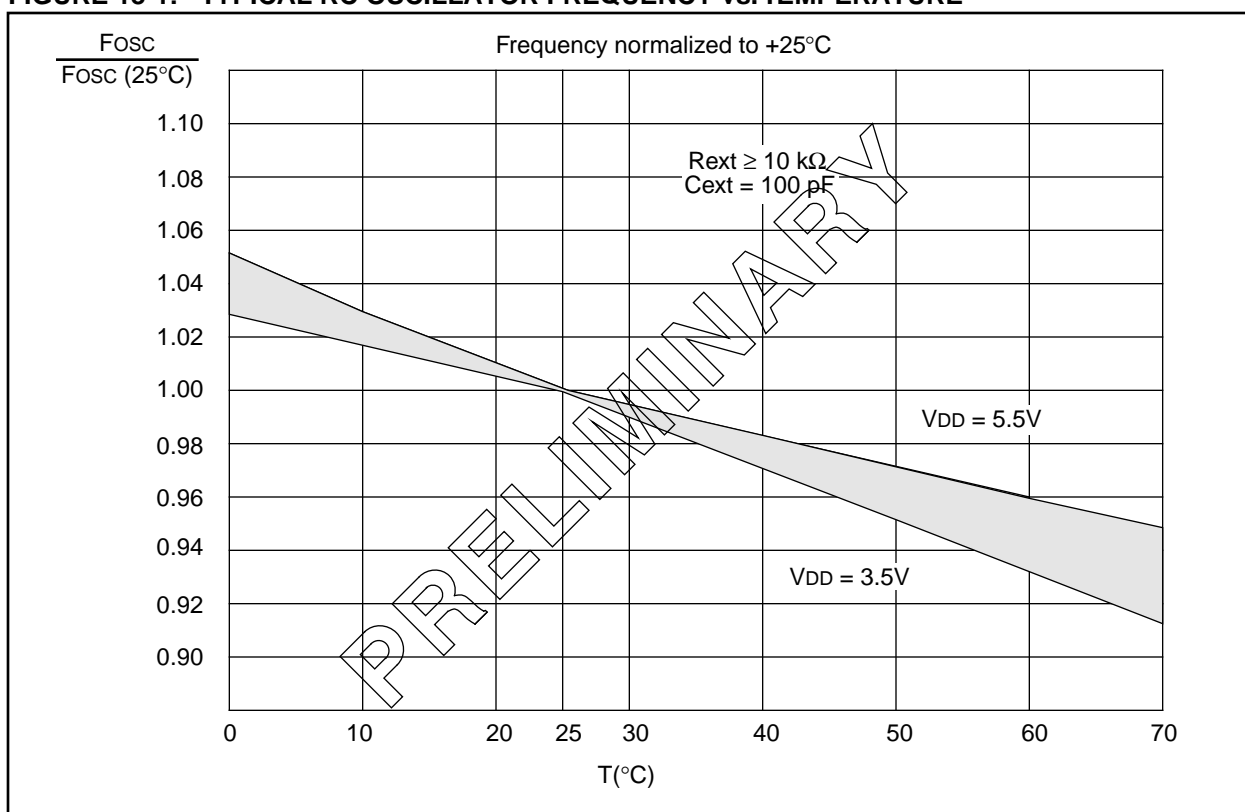
The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified  $V_{DD}$  range). This is for information only and devices are ensured to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents  $(\text{mean} + 3\sigma)$  and  $(\text{mean} - 3\sigma)$  respectively where  $\sigma$  is standard deviation.

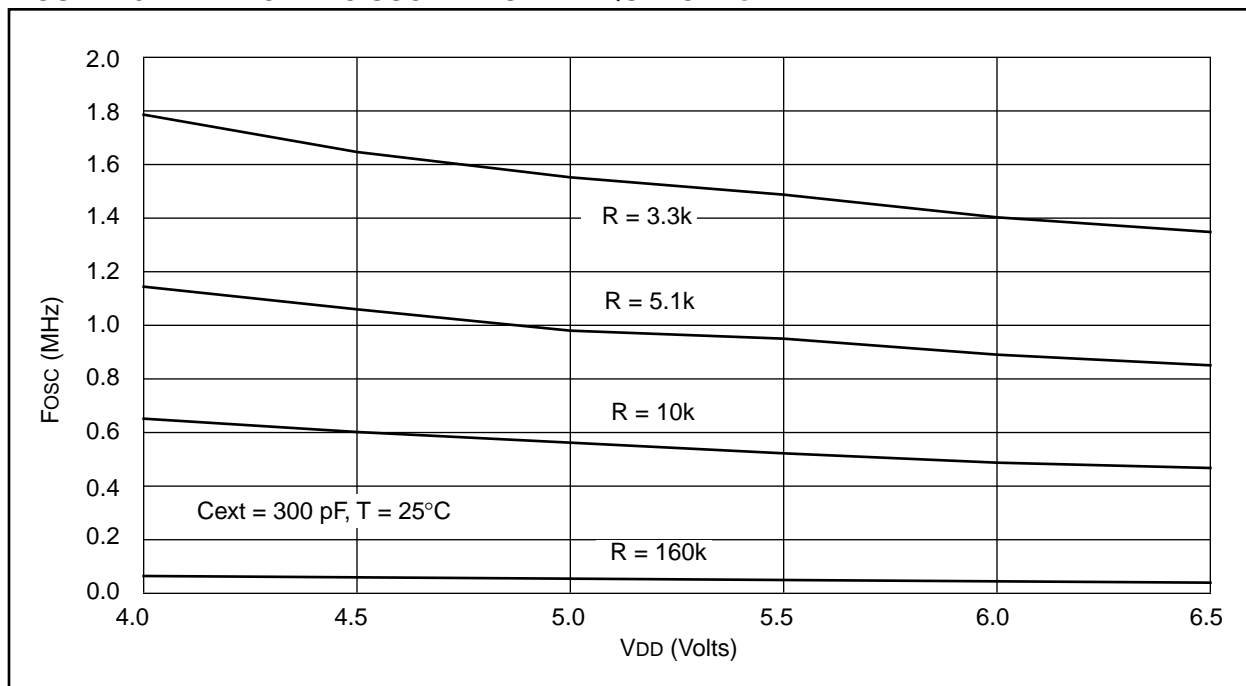
**TABLE 18-1: PIN CAPACITANCE PER PACKAGE TYPE**

Pin Name	Typical Capacitance (pF)			
	40-pin DIP	44-pin PLCC	44-pin MQFP	44-pin TQFP
All pins, except $\overline{\text{MCLR}}$ , $V_{DD}$ , and $V_{SS}$	10	10	10	10
$\overline{\text{MCLR}}$ pin	20	20	20	20

**FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE**



**FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. V<sub>DD</sub>**

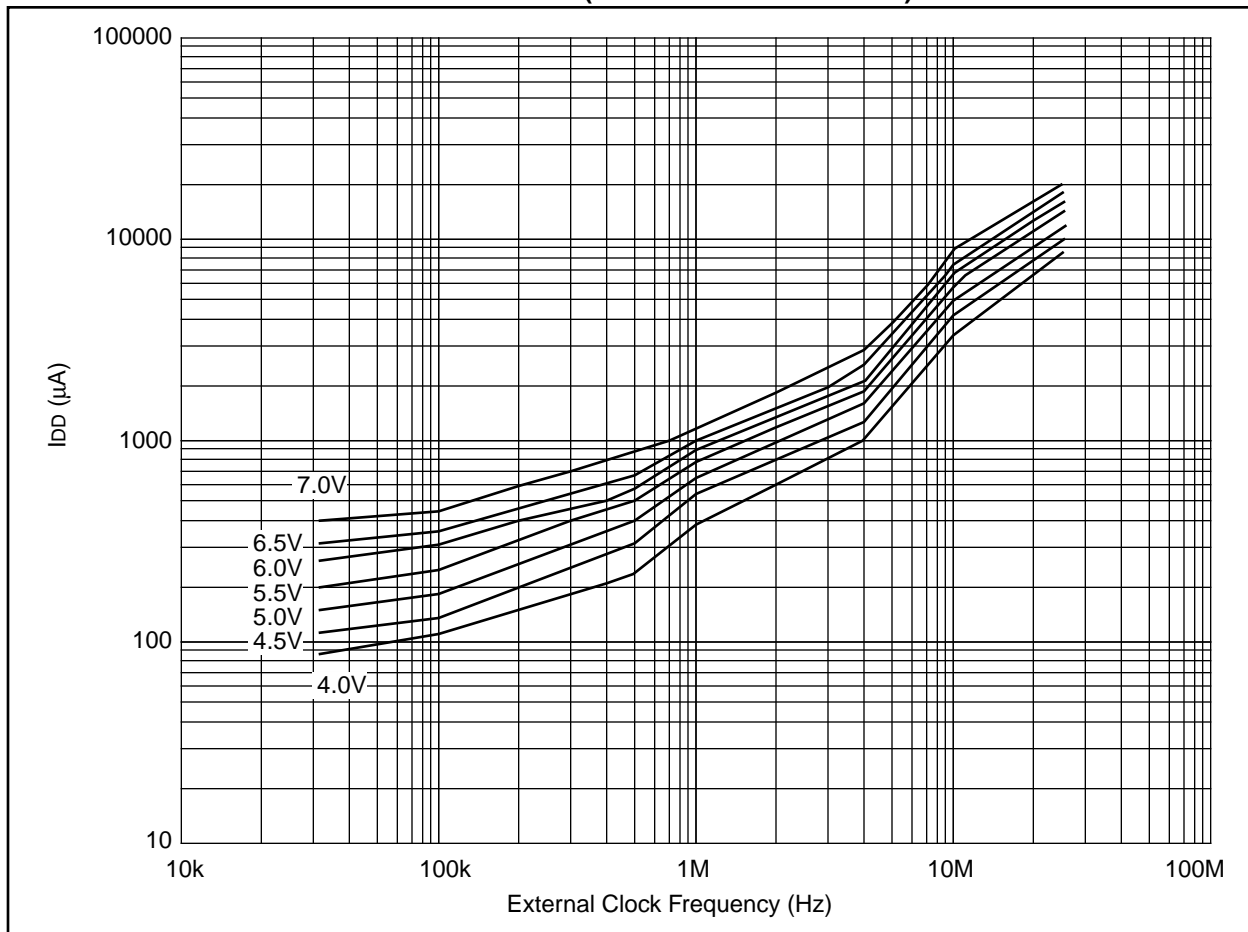


**TABLE 18-2: RC OSCILLATOR FREQUENCIES**

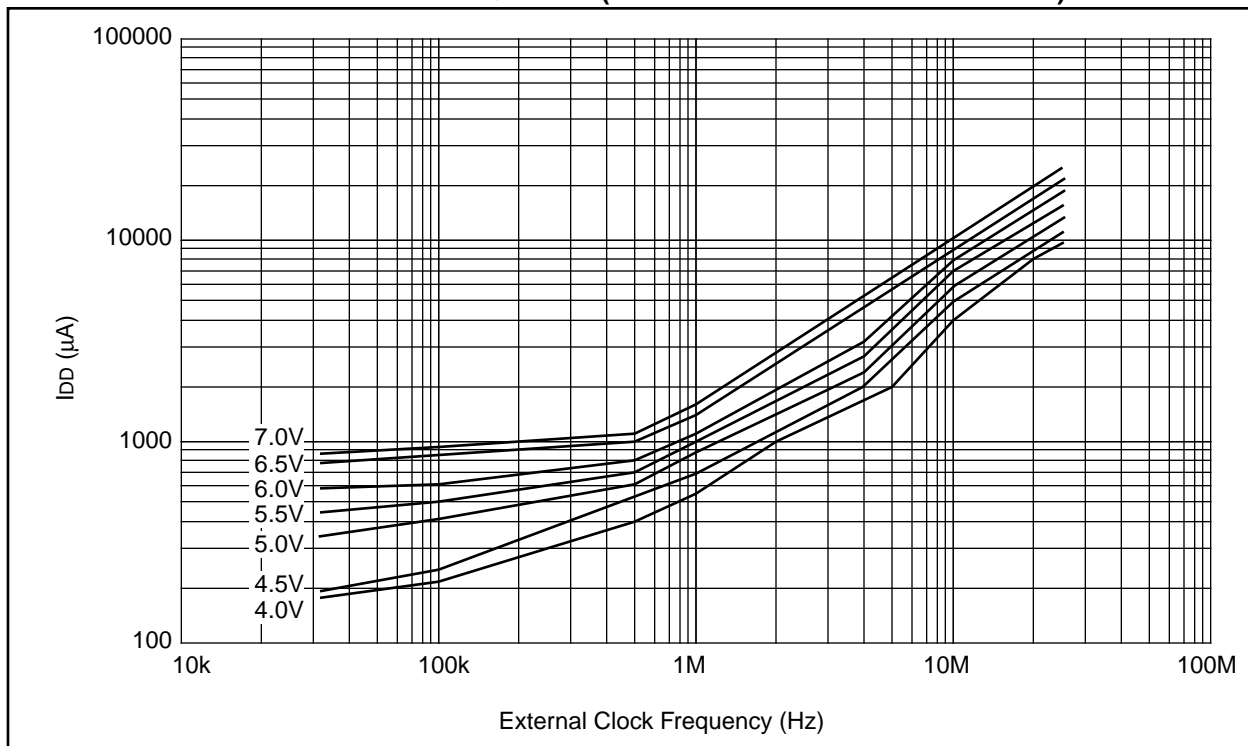
Cext	Rext	Average Fosc @ 5V, 25°C	
22 pF	10k	3.33 MHz	± 12%
	100k	353 kHz	± 13%
100 pF	3.3k	3.54 MHz	± 10%
	5.1k	2.43 MHz	± 14%
	10k	1.30 MHz	± 17%
	100k	129 kHz	± 10%
300 pF	3.3k	1.54 MHz	± 14%
	5.1k	980 kHz	± 12%
	10k	564 kHz	± 16%
	160k	35 kHz	± 18%



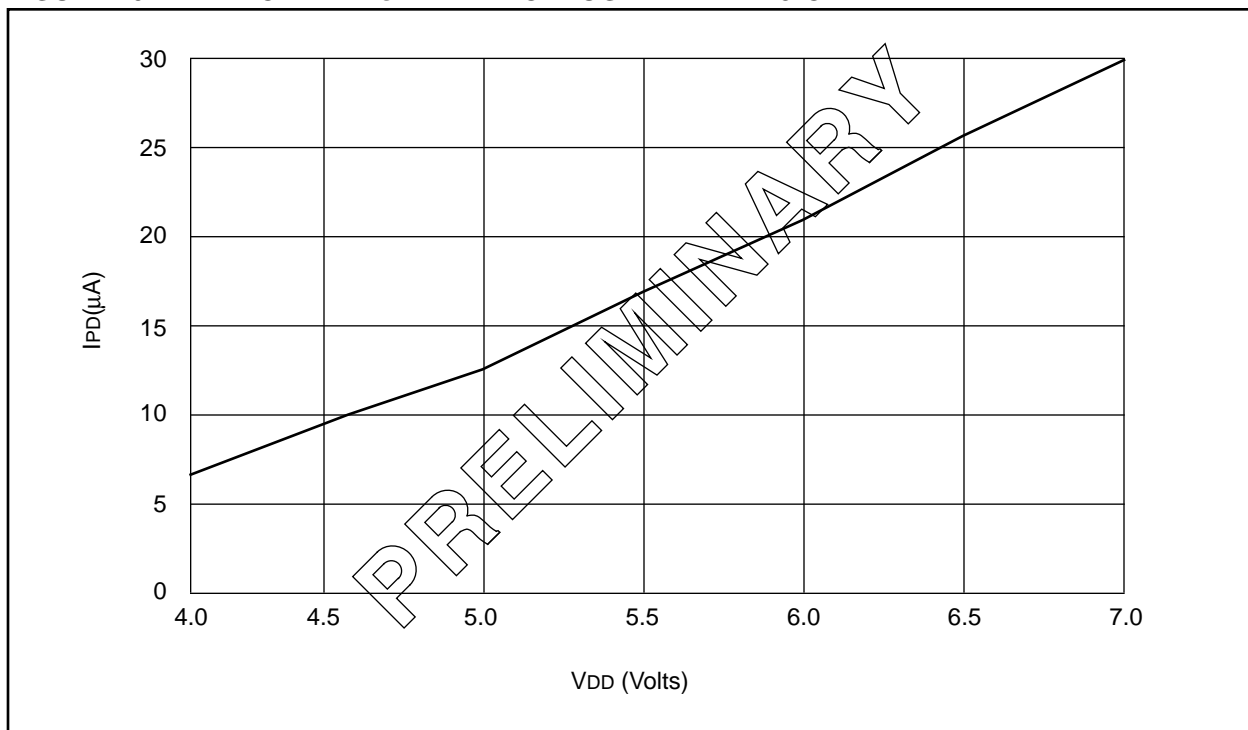
**FIGURE 18-7: TYPICAL  $I_{DD}$  vs. FREQUENCY (EXTERNAL CLOCK 25°C)**



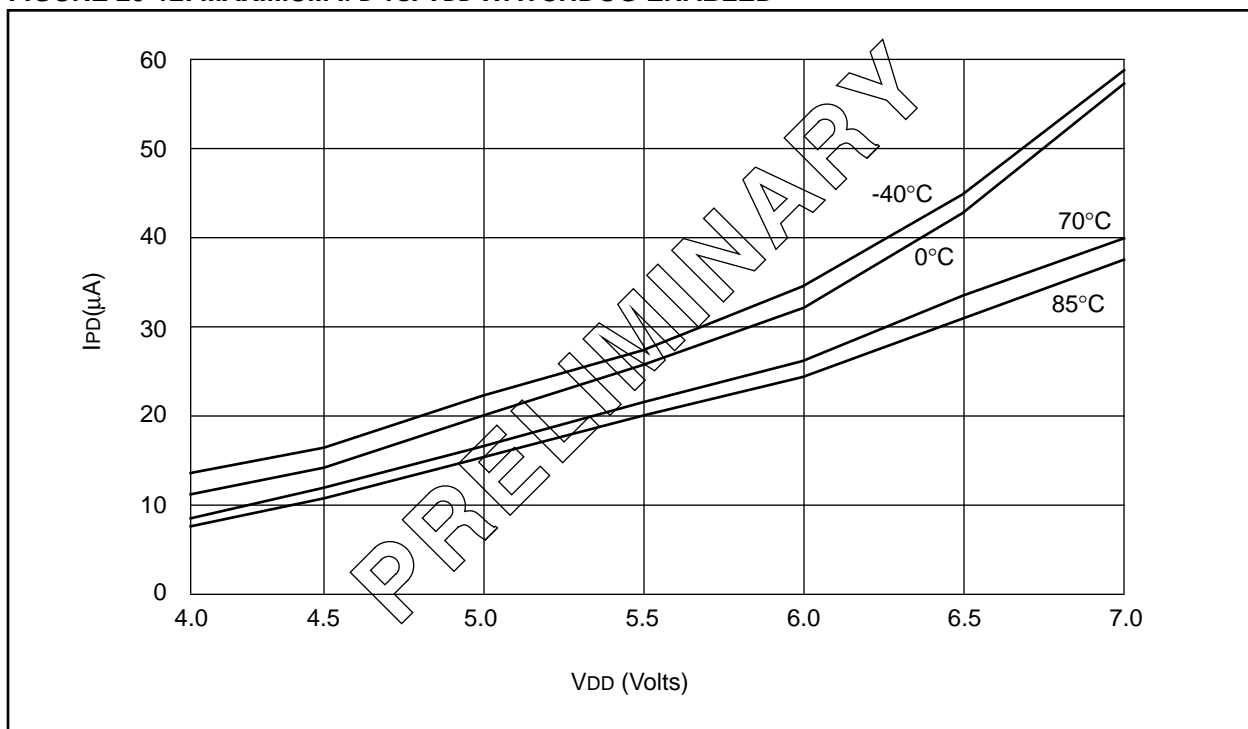
**FIGURE 18-8: MAXIMUM  $I_{DD}$  vs. FREQUENCY (EXTERNAL CLOCK 125°C TO -40°C)**



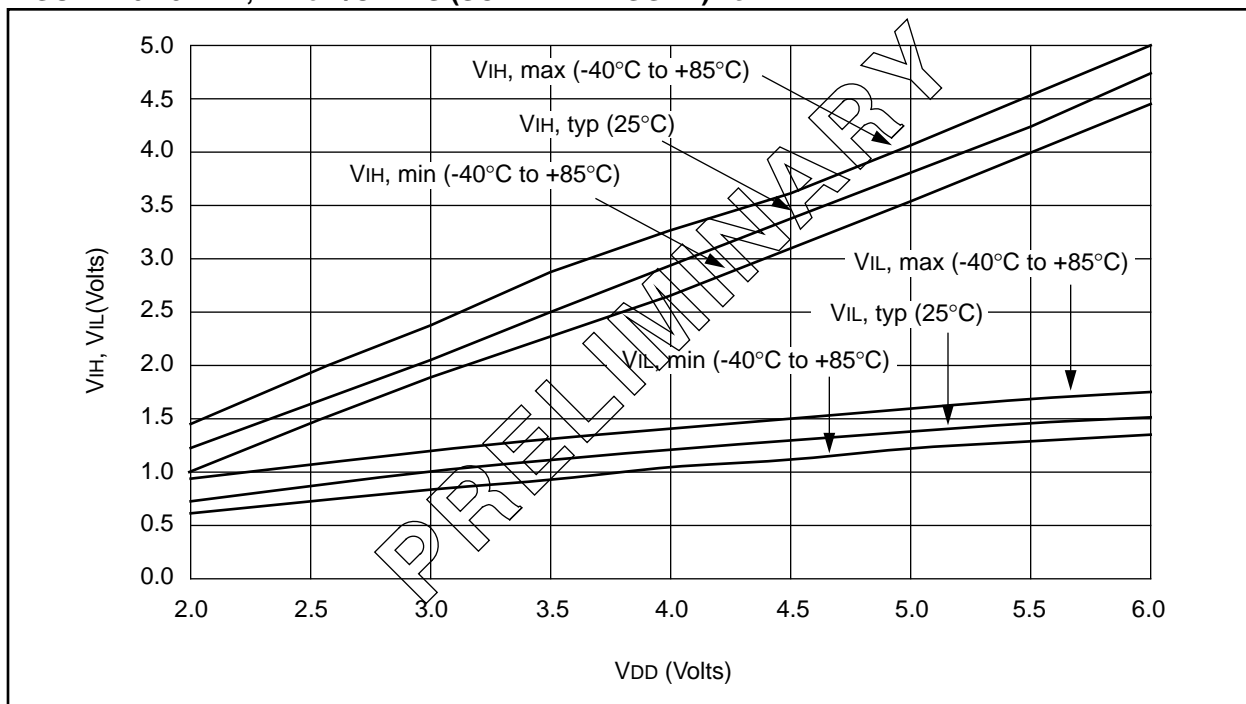
**FIGURE 20-11: TYPICAL  $I_{PD}$  vs.  $V_{DD}$  WATCHDOG ENABLED 25°C**



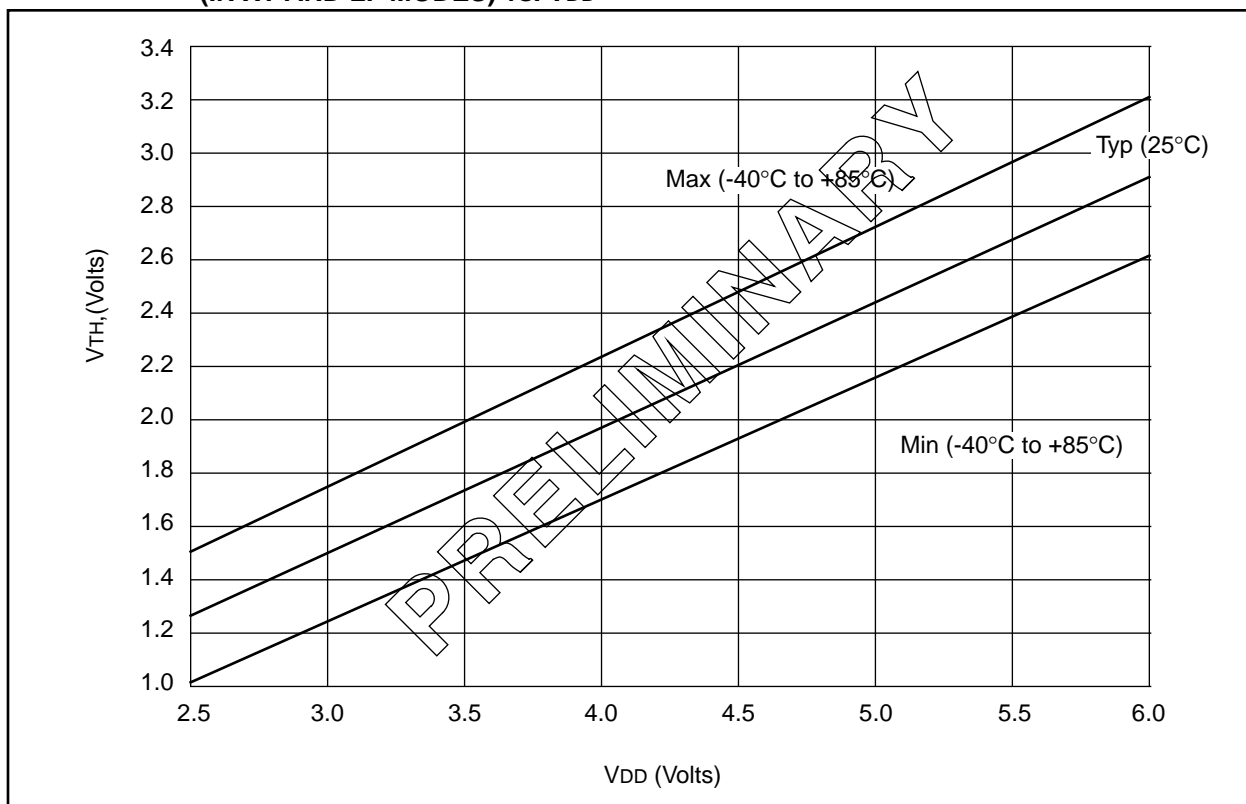
**FIGURE 20-12: MAXIMUM  $I_{PD}$  vs.  $V_{DD}$  WATCHDOG ENABLED**



**FIGURE 20-19:  $V_{IH}$ ,  $V_{IL}$  of I/O PINS (SCHMITT TRIGGER) vs.  $V_{DD}$**



**FIGURE 20-20:  $V_{TH}$  (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT AND LF MODES) vs.  $V_{DD}$**



# PIC17C4X

## E.8 PIC17CXX Family of Devices

	Clock			Memory			Peripherals				Features		
	Maximum Frequency of Operation (MHz)	ROM	Program Memory (Words)	RAM Data Memory (bytes)	Timer Module(s)	Captures/PWMs	Serial Port(s) (USART)	Hardware Multiply	External Interrupts	Interrupt Sources	I/O Pins	Voltage Range (Volts)	Packages
PIC17C42	25	2K	—	232	TMR0, TMR1, TMR2, TMR3	2 2	Yes	—	Yes	11	33	4.5-5.5	40-pin DIP; 44-pin PLCC, MQFP
PIC17C42A	25	2K	—	232	TMR0, TMR1, TMR2, TMR3	2 2	Yes	Yes	Yes	11	33	2.5-6.0	40-pin DIP; 44-pin PLCC, TQFP, MQFP
PIC17CR42	25	—	2K	232	TMR0, TMR1, TMR2, TMR3	2 2	Yes	Yes	Yes	11	33	2.5-6.0	40-pin DIP; 44-pin PLCC, TQFP, MQFP
PIC17C43	25	4K	—	454	TMR0, TMR1, TMR2, TMR3	2 2	Yes	Yes	Yes	11	33	2.5-6.0	40-pin DIP; 44-pin PLCC, TQFP, MQFP
PIC17CR43	25	—	4K	454	TMR0, TMR1, TMR2, TMR3	2 2	Yes	Yes	Yes	11	33	2.5-6.0	40-pin DIP; 44-pin PLCC, TQFP, MQFP
PIC17C44	25	8K	—	454	TMR0, TMR1, TMR2, TMR3	2 2	Yes	Yes	Yes	11	33	2.5-6.0	40-pin DIP; 44-pin PLCC, TQFP, MQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

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