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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	33
Program Memory Size	16KB (8K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	454 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c44-16e-pt

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTES:

6.2 Data Memory Organization

Data memory is partitioned into two areas. The first is the General Purpose Registers (GPR) area, while the second is the Special Function Registers (SFR) area. The SFRs control the operation of the device.

Portions of data memory are banked, this is for both areas. The GPR area is banked to allow greater than 232 bytes of general purpose RAM. SFRs are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the Bank Select Register (BSR). If an access is made to a location outside this banked region, the BSR bits are ignored. Figure 6-5 shows the data memory map organization for the PIC17C42 and Figure 6-6 for all of the other PIC17C4X devices.

Instructions MOVPF and MOVFP provide the means to move values from the peripheral area ("P") to any location in the register file ("F"), and vice-versa. The definition of the "P" range is from 0h to 1Fh, while the "F" range is 0h to FFh. The "P" range has six more locations than peripheral registers (eight locations for the PIC17C42 device) which can be used as General Purpose Registers. This can be useful in some applications where variables need to be copied to other locations in the general purpose RAM (such as saving status information during an interrupt).

The entire data memory can be accessed either directly or indirectly through file select registers FSR0 and FSR1 (Section 6.4). Indirect addressing uses the appropriate control bits of the BSR for accesses into the banked areas of data memory. The BSR is explained in greater detail in Section 6.8.

6.2.1 GENERAL PURPOSE REGISTER (GPR)

All devices have some amount of GPR area. The GPRs are 8-bits wide. When the GPR area is greater than 232, it must be banked to allow access to the additional memory space.

Only the PIC17C43 and PIC17C44 devices have banked memory in the GPR area. To facilitate switching between these banks, the MOVLR bank instruction has been added to the instruction set. GPRs are not initialized by a Power-on Reset and are unchanged on all other resets.

6.2.2 SPECIAL FUNCTION REGISTERS (SFR)

The SFRs are used by the CPU and peripheral functions to control the operation of the device (Figure 6-5 and Figure 6-6). These registers are static RAM.

The SFRs can be classified into two sets, those associated with the "core" function and those related to the peripheral functions. Those registers related to the "core" are described here, while those related to a peripheral feature are described in the section for each peripheral feature.

The peripheral registers are in the banked portion of memory, while the core registers are in the unbanked region. To facilitate switching between the peripheral banks, the MOVLB bank instruction has been provided.

6.2.2.2 CPU STATUS REGISTER (CPUSTA)

The CPUSTA register contains the status and control bits for the CPU. This register is used to globally enable/disable interrupts. If only a specific interrupt is desired to be enabled/disabled, please refer to the INTerrupt STAtus (INTSTA) register and the Peripheral Interrupt Enable (PIE) register. This register also indicates if the stack is available and contains the Power-down (PD) and Time-out (TO) bits. The TO, PD, and STKAV bits are not writable. These bits are set and cleared according to device logic. Therefore, the result of an instruction with the CPUSTA register as destination may be different than intended.

FIGURE 6-8: CPUSTA REGISTER (ADDRESS: 06h, UNBANKED)



12.1 <u>Timer1 and Timer2</u>

12.1.1 TIMER1, TIMER2 IN 8-BIT MODE

Both Timer1 and Timer2 will operate in 8-bit mode when the T16 bit is clear. These two timers can be independently configured to increment from the internal instruction cycle clock or from an external clock source on the RB4/TCLK12 pin. The timer clock source is configured by the TMRxCS bit (x = 1 for Timer1 or = 2 for Timer2). When TMRxCS is clear, the clock source is internal and increments once every instruction cycle (Fosc/4). When TMRxCS is set, the clock source is the RB4/TCLK12 pin, and the timer will increment on every falling edge of the RB4/TCLK12 pin.

The timer increments from 00h until it equals the Period register (PRx). It then resets to 00h at the next increment cycle. The timer interrupt flag is set when the timer is reset. TMR1 and TMR2 have individual interrupt flag bits. The TMR1 interrupt flag bit is latched into TMR1IF, and the TMR2 interrupt flag bit is latched into TMR2IF.

Each timer also has a corresponding interrupt enable bit (TMRxIE). The timer interrupt can be enabled by setting this bit and disabled by clearing this bit. For peripheral interrupts to be enabled, the Peripheral Interrupt Enable bit must be enabled (PEIE is set) and global interrupts must be enabled (GLINTD is cleared).

The timers can be turned on and off under software control. When the Timerx On control bit (TMRxON) is set, the timer increments from the clock source. When TMRxON is cleared, the timer is turned off and cannot cause the timer interrupt flag to be set.

12.1.1.1 EXTERNAL CLOCK INPUT FOR TIMER1 OR TIMER2

When TMRxCS is set, the clock source is the RB4/TCLK12 pin, and the timer will increment on every falling edge on the RB4/TCLK12 pin. The TCLK12 input is synchronized with internal phase clocks. This causes a delay from the time a falling edge appears on TCLK12 to the time TMR1 or TMR2 is actually incremented. For the external clock input timing requirements, see the Electrical Specification section.



FIGURE 12-3: TIMER1 AND TIMER2 IN TWO 8-BIT TIMER/COUNTER MODE

12.2.2 DUAL CAPTURE REGISTER MODE

This mode is selected by setting CA1/PR3. A block diagram is shown in Figure 12-8. In this mode, TMR3 runs without a period register and increments from 0000h to FFFFh and rolls over to 0000h. The TMR3 interrupt Flag (TMR3IF) is set on this roll over. The TMR3IF bit must be cleared in software.

Registers PR3H/CA1H and PR3L/CA1L make a 16-bit capture register (Capture1). It captures events on pin RB0/CAP1. Capture mode is configured by the CA1ED1 and CA1ED0 bits. Capture1 Interrupt Flag bit (CA1IF) is set on the capture event. The corresponding interrupt mask bit is CA1IE. The Capture1 Overflow Status bit is CA1OVF.

The Capture2 overflow status flag bit is double buffered. The master bit is set if one captured word is already residing in the Capture2 register and another "event" has occurred on the RB1/CA2 pin. The new event will not transfer the TMR3 value to the capture register which protects the previous unread capture value. When the user reads both the high and the low bytes (in any order) of the Capture2 register, the master overflow bit is transferred to the slave overflow bit (CA2OVF) and then the master bit is reset. The user can then read TCON2 to determine the value of CA2OVF.

The operation of the Capture1 feature is identical to Capture2 (as described in Section 12.2.1).





TABLE 12-5: REGISTERS ASSOCIATED WITH CAPTURE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA10VF	PWM2ON	PWM1ON	CA1/PR3	TMR3ON	TMR2ON	TMR10N	0000 0000	0000 0000
12h, Bank 2	TMR3L	TMR3 reg	ister; low by	/te						xxxx xxxx	uuuu uuuu
13h, Bank 2	TMR3H	TMR3 reg	ister; high b	oyte						xxxx xxxx	uuuu uuuu
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
06h, Unbanked	CPUSTA	—	_	STKAV	GLINTD	TO	PD	—	—	11 11	11 qq
16h, Bank 2	PR3L/CA1L	Timer3 pe	riod registe	r, low byte/ca	apture1 regis	ter, low byte	e			xxxx xxxx	uuuu uuuu
17h, Bank 2	PR3H/CA1H	Timer3 pe	riod registe	r, high byte/c	apture1 regi	ster, high b	yte			xxxx xxxx	uuuu uuuu
14h, Bank 3	CA2L	Capture2	low byte							xxxx xxxx	uuuu uuuu
15h, Bank 3	CA2H	Capture2	high byte							xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q - value depends on condition, shaded cells are not used by Capture.

Note 1: Other (non power-up) resets include: external reset through MCLR and WDT Timer Reset.



FIGURE 12-10: TMR1, TMR2, AND TMR3 OPERATION IN TIMER MODE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA10VF	PWM2ON	PWM1ON	CA1/PR3	TMR3ON	TMR2ON	TMR10N	0000 0000	0000 0000
10h, Bank 2	TMR1	Timer1 re	gister							xxxx xxxx	uuuu uuuu
11h, Bank 2	TMR2	Timer2 re	gister							xxxx xxxx	uuuu uuuu
12h, Bank 2	TMR3L	TMR3 reg	ister; low by	⁄te						xxxx xxxx	uuuu uuuu
13h, Bank 2	TMR3H	TMR3 reg	ister; high b	yte						xxxx xxxx	uuuu uuuu
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	TOIE	INTE	0000 0000	0000 0000
06h, Unbanked	CPUSTA	—	-	STKAV	GLINTD	TO	PD	—	—	11 11	11 qq
14h, Bank 2	PR1	Timer1 pe	riod registe	r		•				xxxx xxxx	uuuu uuuu
15h, Bank 2	PR2	Timer2 pe	riod registe	r						xxxx xxxx	uuuu uuuu
16h, Bank 2	PR3L/CA1L	Timer3 pe	riod/capture	e1 register; l	ow byte					xxxx xxxx	uuuu uuuu
17h, Bank 2	PR3H/CA1H	Timer3 pe	riod/capture	e1 register; l	high byte					xxxx xxxx	uuuu uuuu
10h, Bank 3	PW1DCL	DC1	DC0	—	_	—	—	—	—	xx	uu
11h, Bank 3	PW2DCL	DC1	DC0	TM2PW2	_	—	—	—	—	xx0	uu0
12h, Bank 3	PW1DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
13h, Bank 3	PW2DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
14h, Bank 3	CA2L	Capture2	low byte							xxxx xxxx	uuuu uuuu
15h, Bank 3	CA2H	Capture2	high byte							xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q - value depends on condition, shaded cells are not used by TMR1, TMR2 or TMR3.

Note 1: Other (non power-up) resets include: external reset through MCLR and WDT Timer Reset.

TABLE 13-3:	BAUD RATES FOR SYNCHRONOUS MODE

BAUD RATE (K)	Fosc = 3	3 MHz %ERROR	SPBRG value (decimal)	Fosc = 2	5 MHz %ERROR	SPBRG value (decimal)	FOSC = 2	0 MHz %ERROR	SPBRG value (decimal)	Fosc = 1	6 MHz %ERROR	SPBRG value (decimal)
()		/02111011	(accinal)		<i>x</i> 021111011	(40011141)		<i>/</i> 021111011	(uconnai)		<i>/</i> 021111011	(uconnai)
0.3	NA	_	_	NA	—	_	NA	_	_	NA	_	—
1.2	NA	_	_	NA	—	_	NA	_	_	NA	_	_
2.4	NA	—	—	NA	—	—	NA	—	—	NA	—	—
9.6	NA	_	—	NA	_	—	NA	_	—	NA	_	_
19.2	NA	—	_	NA	—	_	19.53	+1.73	255	19.23	+0.16	207
76.8	77.10	+0.39	106	77.16	+0.47	80	76.92	+0.16	64	76.92	+0.16	51
96	95.93	-0.07	85	96.15	+0.16	64	96.15	+0.16	51	95.24	-0.79	41
300	294.64	-1.79	27	297.62	-0.79	20	294.1	-1.96	16	307.69	+2.56	12
500	485.29	-2.94	16	480.77	-3.85	12	500	0	9	500	0	7
HIGH	8250	—	0	6250	—	0	5000	—	0	4000	—	0
LOW	32.22	_	255	24.41	_	255	19.53	_	255	15.625	_	255

BAUD	Fosc = 10 M	Hz	SPBRG	Fosc = 7.159) MHz	SPBRG	FOSC = 5.068	3 MHz	SPBRG
RATE (K)	KBAUD	%ERROR	value (decimal)	KBAUD	%ERROR	value (decimal)	KBAUD	%ERROR	value (decimal)
0.3	NA	_	_	NA	_	_	NA	_	
1.2	NA	_	_	NA	_	_	NA	_	_
2.4	NA	_	_	NA	_	_	NA	_	_
9.6	9.766	+1.73	255	9.622	+0.23	185	9.6	0	131
19.2	19.23	+0.16	129	19.24	+0.23	92	19.2	0	65
76.8	75.76	-1.36	32	77.82	+1.32	22	79.2	+3.13	15
96	96.15	+0.16	25	94.20	-1.88	18	97.48	+1.54	12
300	312.5	+4.17	7	298.3	-0.57	5	316.8	+5.60	3
500	500	0	4	NA	_	_	NA	_	_
HIGH	2500	_	0	1789.8	_	0	1267	_	0
LOW	9.766	_	255	6.991	_	255	4.950	_	255
BAUD	Fosc = 3.579	MHz	SPBRG	Fosc = 1 MH	Z	SPBRG	Fosc = 32.76	8 kHz	SPBRG
BAUD RATE (K)	Fosc = 3.579 KBAUD	MHz %ERROR	SPBRG value (decimal)	Fosc = 1 MH KBAUD	z %ERROR	SPBRG value (decimal)	Fosc = 32.76 KBAUD	68 kHz %ERROR	SPBRG value (decimal)
BAUD RATE (K)	Fosc = 3.579 KBAUD NA	MHz %ERROR —	SPBRG value (decimal)	Fosc = 1 MH KBAUD NA	z %ERROR —	SPBRG value (decimal)	Fosc = 32.76 KBAUD 0.303	68 kHz %ERROR +1.14	SPBRG value (decimal) 26
BAUD RATE (K) 0.3 1.2	Fosc = 3.579 KBAUD NA NA	MHz %ERROR — —	SPBRG value (decimal) —	Fosc = 1 MH KBAUD NA 1.202	z %ERROR — +0.16	SPBRG value (decimal) — 207	Fosc = 32.76 KBAUD 0.303 1.170	58 kHz %ERROR +1.14 -2.48	SPBRG value (decimal) 26 6
BAUD RATE (K) 0.3 1.2 2.4	Fosc = 3.579 KBAUD NA NA NA	MHz %ERROR — — —	SPBRG value (decimal) — —	Fosc = 1 MH KBAUD NA 1.202 2.404	z %ERROR +0.16 +0.16	SPBRG value (decimal) — 207 103	FOSC = 32.76 KBAUD 0.303 1.170 NA	68 kHz %ERROR +1.14 -2.48 —	SPBRG value (decimal) 26 6 —
BAUD RATE (K) 0.3 1.2 2.4 9.6	Fosc = 3.579 KBAUD NA NA 9.622	MHz %ERROR +0.23	SPBRG value (decimal) — — — 92	Fosc = 1 MH KBAUD NA 1.202 2.404 9.615	z %ERROR 	SPBRG value (decimal) — 207 103 25	FOSC = 32.76 KBAUD 0.303 1.170 NA NA	8 kHz %ERROR +1.14 -2.48 	SPBRG value (decimal) 26 6
BAUD RATE (K) 0.3 1.2 2.4 9.6 19.2	Fosc = 3.579 KBAUD NA NA 9.622 19.04	MHz %ERROR +0.23 -0.83	SPBRG value (decimal) — — — 92 46	Fosc = 1 MH KBAUD NA 1.202 2.404 9.615 19.24	z %ERROR 	SPBRG value (decimal) — 207 103 25 12	Fosc = 32.76 KBAUD 0.303 1.170 NA NA NA	58 kHz %ERROR +1.14 -2.48 	SPBRG value (decimal) 26 6
BAUD RATE (K) 0.3 1.2 2.4 9.6 19.2 76.8	Fosc = 3.579 KBAUD NA NA 9.622 19.04 74.57	MHz %ERROR — — +0.23 -0.83 -2.90	SPBRG value (decimal) — — 92 46 11	FOSC = 1 MH KBAUD NA 1.202 2.404 9.615 19.24 83.34	Z %ERROR +0.16 +0.16 +0.16 +0.16 +0.16 +8.51	SPBRG value (decimal) — 207 103 25 12 2 2	Fosc = 32.76 KBAUD 0.303 1.170 NA NA NA NA	58 kHz %ERROR +1.14 -2.48 	SPBRG value (decimal) 26 6
BAUD RATE (K) 0.3 1.2 2.4 9.6 19.2 76.8 96	Fosc = 3.579 KBAUD NA NA 9.622 19.04 74.57 99.43	MHz %ERROR — — +0.23 -0.83 -2.90 _3.57	SPBRG value (decimal) — — — 92 46 11 8	FOSC = 1 MH KBAUD NA 1.202 2.404 9.615 19.24 83.34 NA	z <u>~</u> +0.16 +0.16 +0.16 +0.16 +8.51 _	SPBRG value (decimal) — 207 103 25 12 2 2 	Fosc = 32.76 KBAUD 0.303 1.170 NA NA NA NA NA	58 kHz %ERROR +1.14 -2.48 	SPBRG value (decimal) 26 6
BAUD RATE (K) 0.3 1.2 2.4 9.6 19.2 76.8 96 300	Fosc = 3.579 KBAUD NA NA 9.622 19.04 74.57 99.43 298.3	MHz %ERROR — +0.23 -0.83 -2.90 _3.57 -0.57	SPBRG value (decimal) — — 92 46 11 8 2	Fosc = 1 MH KBAUD NA 1.202 2.404 9.615 19.24 83.34 NA NA	Z %ERROR +0.16 +0.16 +0.16 +0.16 +8.51 	SPBRG value (decimal) — 207 103 25 12 2 2 — 2 —	Fosc = 32.76 KBAUD 0.303 1.170 NA NA NA NA NA NA	68 kHz %ERROR +1.14 -2.48 	SPBRG value (decimal) 26 6
BAUD RATE (K) 0.3 1.2 2.4 9.6 19.2 76.8 96 300 500	Fosc = 3.579 KBAUD NA NA 9.622 19.04 74.57 99.43 298.3 NA	MHz %ERROR — +0.23 -0.83 -2.90 _3.57 -0.57 —	SPBRG value (decimal) — — 92 46 11 8 2 	Fosc = 1 MH KBAUD NA 1.202 2.404 9.615 19.24 83.34 NA NA NA	Z %ERROR +0.16 +0.16 +0.16 +0.16 +8.51 	SPBRG value (decimal) 207 103 25 12 2 2 2 	Fosc = 32.76 KBAUD 0.303 1.170 NA NA NA NA NA NA NA	58 kHz %ERROR +1.14 -2.48 	SPBRG value (decimal) 26 6
BAUD RATE (K) 0.3 1.2 2.4 9.6 19.2 76.8 96 300 500 HIGH	Fosc = 3.579 KBAUD NA NA 9.622 19.04 74.57 99.43 298.3 NA 894.9	MHz %ERROR — +0.23 -0.83 -2.90 _3.57 -0.57 — _ _	SPBRG value (decimal) — — 92 46 11 8 2 _ _ 0	Fosc = 1 MH KBAUD NA 1.202 2.404 9.615 19.24 83.34 NA NA NA NA 250	Z %ERROR +0.16 +0.16 +0.16 +0.16 +8.51 	SPBRG value (decimal) 207 103 25 12 2 2 0	Fosc = 32.76 KBAUD 0.303 1.170 NA NA NA NA NA NA NA NA NA S.192	68 kHz %ERROR +1.14 -2.48 	SPBRG value (decimal) 26 6 0

AND	DWF	AND WRI	EG with	f			
Synt	tax:	[label] A	[label] ANDWF f,d				
Ope	rands:	$\begin{array}{l} 0 \leq f \leq 25 \\ d \in \ [0,1] \end{array}$	$0 \le f \le 255$ $d \in [0,1]$				
Ope	ration:	(WREG) .	AND. (f)	ightarrow (dest)	1		
Stat	us Affected:	Z					
Enco	oding:	0000	101d	ffff	ffff		
Des	cription:	The conten register 'f'. in WREG. I back in reg	its of WR If 'd' is 0 f 'd' is 1 t ister 'f'.	EG are AN the result he result is	D'ed with is stored s stored		
Wor	ds:	1					
Cycl	es:	1					
QC	ycle Activity:						
	Q1	Q2	Q	3	Q4		
	Decode	Read register 'f'	Exect	ute V de:	Vrite to stination		
<u>Exa</u>	<u>mple</u> :	ANDWF	REG, 1				
	Before Instru WREG REG	iction = 0x17 = 0xC2					
	After Instruct WREG REG	tion = 0x17 = 0x02					

BCF		Bit Clear	f					
Synt	tax:	[label] E	[<i>label</i>] BCF f,b					
Ope	rands:	$\begin{array}{l} 0 \leq f \leq 25 \\ 0 \leq b \leq 7 \end{array}$	5					
Ope	ration:	$0 \rightarrow (f < b >$	-)					
Stat	us Affected:	None						
Enc	oding:	1000	1bbb	fff	f	ffff		
Des	cription:	Bit 'b' in re	gister 'f' is	s clear	ed.			
Wor	ds:	1						
Cycl	es:	1						
QC	ycle Activity:							
	Q1	Q2	Q3	3		Q4		
	Decode	Read register 'f'	Execu	ute	re	Write gister 'f'		
Exa	mple:	BCF	FLAG_R	EG,	7			
	Before Instru FLAG_R	iction EG = 0xC7						
	After Instruct FLAG_R	tion EG = 0x47						

IORWF	Inclusive		with f	LCA	LL	Long C	all		
Syntax:	[label]	IORWF f,d		Syn	tax:	[label]	LCALL	k	
Operands:	$0 \le f \le 255$	5		Ope	rands:	$0 \le k \le 2$	255		
	d ∈ [0,1]			Ope	ration:	PC + 1 ·	\rightarrow TOS;		
Operation:	(WREG) .	$OR.\left(f ight) ightarrow\left(de ight)$	est)			$k\toPC$	L, (PCLAT	$H) \rightarrow PC$	СН
Status Affected:	Z			Stat	us Affected:	None			
Encoding:	0000	100d ff:	ff ffff	Enc	oding:	1011	0111	kkkk	kkkk
Description:	Inclusive O 'd' is 0 the r 'd' is 1 the r ter 'f'.	R WREG with result is placed result is placed	register 'f'. If I in WREG. If I back in regis-	Des	cription:	LCALL al tine call t gram me First, the	llows an und o anywhere mory space return addr	conditiona within th ess (PC -	al subrou- e 64k pro- + 1) is
Words:	1					pushed c	onto the stac	ck. A 16-I	bit desti-
Cycles:	1					program	counter. Th	en loaded 1e lower 8	Into the B-bits of
Q Cycle Activity:						the destin	nation addre	ess is em	bedded in
Q1	Q2	Q3	Q4			the instru	from PC hi	upper 8-b ah holdin	oits of PC
Decode	Read	Execute	Write to			PCLATH.		9	9,
	register i		uesunation	Wor	ds:	1			
Example:	IORWF R	esult, O		Сус	es:	2			
Before Instru	iction			QC	ycle Activity:				
WREG	$= 0x^{13}$ = 0x91				Q1	Q2	Q3		Q4
After Instruct	tion				Decode	Read literal 'k'	Execu	ite reg	Write ister PCL
WREG	= 0x13 = 0x93				Forced NOP	NOP	Execu	ite	NOP
				<u>Exa</u>	<u>mple</u> :	MOVLW MOVPF LCALL	HIGH(SUB WREG, PC LOW(SUBR	ROUTINE LATH OUTINE)])

Before Instruction

SUBROUTINE PC	= =	16-bit Address ?
After Instruction		

PC = Address (SUBI

RRN	ICF	Rotate R	light f (n	o carry)	
Synt	ax:	[label]	RRNCF	f,d	
Ope	rands:	0 ≤ f ≤ 25 d ∈ [0,1]	55		
Ope	ration:	$f < n > \rightarrow c$ $f < 0 > \rightarrow c$	l <n-1>; l<7></n-1>		
Statu	us Affected:	None			
Enco	oding:	0010	000d	ffff	ffff
Desc	cription:	The conte one bit to placed in placed ba	nts of regi the right. I WREG. If ck in regis	ster 'f' are f 'd' is 0 the d' is 1 the ter 'f'.	rotated e result is result is
			► re	gister f	
Word	ds:	1			
Cycl	es:	1			
	cle Activity.				
_ Q O J	, 0.0 / .0				
Q 0)	Q1	Q2	Q3	8	Q4
	Q1 Decode	Q2 Read register 'f'	Q3 Exect	ute V des	Q4 Vrite to stination
Exar	Q1 Decode nple 1:	Q2 Read register 'f'	Q3 Exect REG, 1	ute V de:	Q4 Vrite to stination
Exar	Q1 Decode mple 1: Before Instru WREG REG	Q2 Read register 'f' RRNCF Inction = ? = 1101	Q3 Exect REG, 1 0111	ute V de:	Q4 Vrite to stination
Exar	Q1 Decode mple 1: Before Instru WREG REG After Instruct WREG REG	Q2 Read register 'f' RRNCF action = ? = 1101 tion = 0 = 1110	Q3 Exect REG, 1 0111	ute V de:	Q4 Vrite to stination
Exar Exar	Q1 Decode mple 1: Before Instru WREG REG After Instruct WREG REG	Q2 Read register 'f' RRNCF action = ? = 1101 tion = 0 = 1110 RRNCF	Q3 Exect REG, 1 0111 REG, 0	ute V de:	Q4 Vrite to stination
Exar	Q1 Decode mple 1: Before Instru WREG REG After Instruct WREG REG mple 2: Before Instru WREG REG	Q2 Read register 'f' RRNCF action = ? = 1101 tion = 0 = 1110 RRNCF action = ? = 1101	Q3 Exect REG, 1 0111 REG, 0 0111	ute V de:	Q4 Vrite to stination

SETF	S	et f			
Syntax:	[/	abel]	SETF	f,s	
Operands:	0 s	≤ f ≤ 25 ∈ [0,1]	5		
Operation:	FI FI	$Fh \rightarrow f;$ $Fh \rightarrow d$			
Status Affected:	Ν	one			
Encoding:		0010	101s	ffff	ffff
Description:	lf 'f' or to	's' is 0, b and WR nly the da FFh.	oth the da EG are se ata memo	ta memo et to FFh. ry locatio	ry location If 's' is 1 n 'f' is set
Words:	1				
Cycles:	1				
Q Cycle Activity:					
Q1		Q2	Q	3	Q4
Decode	re	Read gister 'f'	Exect	ute re a s	Write egister 'f' nd other pecified register
Example1:	SI	STF	REG, 0		
Before Instru REG WREG	uctio = =	n 0xDA 0x05			
After Instruct REG WREG	tion = =	0xFF 0xFF			
Example2:	SE	TF	REG, 1		
Before Instru REG WREG	uctio = =	n 0xDA 0x05			
After Instruct REG WREG	tion = =	0xFF 0x05			

TLW	л	Та	able Lato	ch Write		TSTF	SZ	Test f, sk	ip if 0	
Synt	ax:	[/	<i>abel</i>] T	LWT t,f		Synta	ax:	[label]	TSTFSZ f	
Ope	rands:	0	≤ f ≤ 255	5		Oper	ands:	$0 \le f \le 25$	5	
		t e	₌ [0,1]			Oper	ation:	skip if f =	0	
Ope	ration:	lf	t = 0,			Statu	s Affected:	None		
		lf	$t \rightarrow IB$ t = 1.	LAIL;		Enco	ding:	0011	0011 f:	fff ffff
			$f \rightarrow TB$	LATH		Desc	ription:	If 'f' = 0, th	e next instruc	tion, fetched
State	us Affected:	Ν	one					during the	current instru	ction execution,
Enco	oding:	Γ	1010	01tx ff	ff ffff			making this	s a two-cycle	instruction.
Des	cription:	Da	ata from fi	le register 'f' is	s written into	Word	ls:	1		
		th	e 16-bit ta	ble latch (TBL	_AT).	Cycle	es:	1 (2)		
		lt i lf i	t = 1; high t = 0: low l	byte is written	n	Q Cy	cle Activity:			
		" Tł	nis instruc	tion is used in	conjunction		Q1	Q2	Q3	Q4
		wi	th TABLW	⊤ to transfer d	ata from data		Decode	Read	Execute	NOP
		m	emory to p	program mem	ory.	lf okir	<u>.</u>	register 'f'		
VVor	ds:	1				II SKI	J. 01	02	03	∩4
Cycl	es:	1				Γ	Forced NOP	NOP	Execute	NOP
QC	ycle Activity:			•	<u>.</u>	L L				
	Q1 Decede		Q2 Road	Q3	Q4	Exam	<u>ipie</u> :	NZERO	:	1.1.
	Decode	reg	gister 'f'	Execute	register			ZERO :		
					TBLATH or	E	Before Instru	uction		
					IBLAIL		PC = Ad	dress(HERE)		
<u>Exa</u>	<u>mple</u> :	TI	LWT t	, RAM			After Instruc	tion – Ov	(00	
	Before Instru	ictio	n				PC	= A	ddress (ZERC))
	t RAM	=	0 0xB7				If CNT	≠ 0×	(00,	
	TBLAT	=	0x0000	(TBLATH =	0x00)		PC	= A	ddress (NZEF	20)
				(TBLATL = 0)	0x00)					
	After Instruc	tion								
	RAM	=	0xB7		0.00					
	IBLAI	=	0X00B7	(TBLATH = (TBLATL = (0x00) 0xB7)					
	Before Instru	uctio	n							
	t	=	1							
	RAM	=	0xB7							
	TBLAT	=	0x0000	(TBLATH = (TBLATL = (0x00) 0x00)					
	After Instruc	tion								
		=	0xB7							
	IDLAI	=	0,00	(TBLATL = 0)	0x00)					

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DC CHARA	CTERI	STICS	Standard C Operating te Operating v	perating emperatu	g Conditic ire -40°C DD range a	ons (ur C ≤ TA : s desc	nless otherwise stated) ≤ +40°C cribed in Section 17.1
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		Internal Program Memory Programming Specs (Note 4)					
D110 D111	Vpp Vddp	Voltage on MCLR/VPP pin Supply voltage during programming	12.75 4.75	_ 5.0	13.25 5.25	V V	Note 5
D112	IPP	Current into MCLR/VPP pin	-	25 ‡	50 ‡	mA	
D113	IDDP	Supply current during programming	_	_	30 ‡	mA	
D114	TPROG	Programming pulse width	10	100	1000	μs	Terminated via internal/exter- nal interrupt or a reset

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

t These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17CXX Programming Specifications (Literature number DS30139).

5: The MCLR/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

Note: When using the Table Write for internal programming, the device temperature must be less than 40°C.

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FIGURE 20-13: WDT TIMER TIME-OUT PERIOD vs. VDD



FIGURE 20-14: IOH vs. VOH, VDD = 3V



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FIGURE 20-16: IOL vs. VOL, VDD = 3V



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21.0 PACKAGING INFORMATION

21.1 40-Lead Ceramic CERDIP Dual In-line, and CERDIP Dual In-line with Window (600 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
		Millimeters			Inches	
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
В	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
С	0.203	0.381	Typical	0.008	0.015	Typical
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	14.986	16.002	Typical	0.590	0.630	Typical
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	40	40		40	40	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

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E.4 PIC16C6X Family of Devices

					Clock M	lemo	≥		6	eriphe	erals	F		Features
			ToL BIT		FLO (SQ 10, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5,			AND OF OF	THOMAS	TAX HOLD			(SHOT)	63111111183601d 1833
	Carlor I	XI LENDER		HOL	NN FOLIDIAN RECOVERED	CC SON	solute Col	STIDD T	ale ale	S ANIHO	Suiton Suite	Se age	Sitolite	SWILL COLOGE
PIC16C62	20	2K	Ι	128	TMR0, TMR1, TMR2	,	SPI/I ² C	Ι	7	22	3.0-6.0	Yes	Ι	28-pin SDIP, SOIC, SSOP
PIC16C62A ⁽¹⁾	20	2K	Ι	128	TMR0, TMR1, TMR2	~	SPI/I ² C	I	7	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC, SSOP
PIC16CR62 ⁽¹⁾	20	Ι	2K	128	TMR0, TMR1, TMR2	-	SPI/I ² C	I	7	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC, SSOP
PIC16C63	20	4K	Ι	192	TMR0, TMR1, TMR2	2 6	sPI/I ² C, JSART	I	10	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC
PIC16CR63 ⁽¹⁾	20	Ι	4 X	192	TMR0, TMR1, TMR2	2	sPI/I ² C, JSART	I	10	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC
PIC16C64	20	2K	Ι	128	TMR0, TMR1, TMR2	~	SPI/I ² C	Yes	∞	33	3.0-6.0	Yes	I	40-pin DIP; 44-pin PLCC, MQFP
PIC16C64A ⁽¹⁾	20	2K	Ι	128	TMR0, TMR1, TMR2	~	SPI/I ² C	Yes	æ	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP
PIC16CR64 ⁽¹⁾	20	Ι	2K	128	TMR0, TMR1, TMR2	~	SPI/I ² C	Yes	æ	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP
PIC16C65	20	44 A	Ι	192	TMR0, TMR1, TMR2	2	sPI/I ² C, JSART	Yes	11	33	3.0-6.0	Yes		40-pin DIP; 44-pin PLCC, MQFP
PIC16C65A ⁽¹⁾	20	4K	Ι	192	TMR0, TMR1, TMR2	2	sPI/I ² C, JSART	Yes	11	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP
PIC16CR65 ⁽¹⁾	20		4K	192	TMR0, TMR1, TMR2	2 5	sPI/I²C, JSART	Yes	11	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP
All PI All PI	C16/17 C16C6	^r family	y devic ilv devi	ces hav ices us	e Power-on Rese e serial program	et, se mina	ectable with close	Watch ck pin I	dog Ti RB6 a	mer, s nd dat	electable c	id abo	otect,	and high I/O current capability.

All PIC16C6X family devices use serial programming with clock pin RB6 and data pin Note 1: Please contact your local sales office for availability of these devices. NOTES:

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