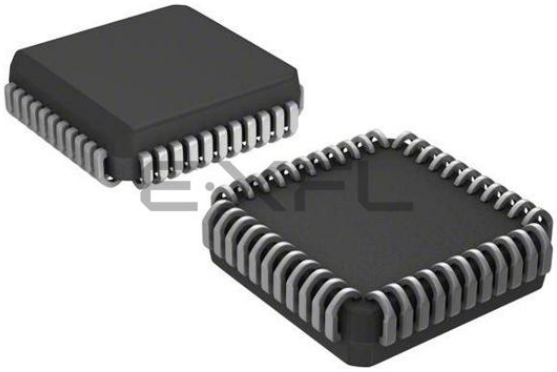

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 16KB (8K x 16) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 454 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic17c44t-16-l |

## 2.0 PIC17C4X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC17C4X Product Selection System section at the end of this data sheet. When placing orders, please use the "PIC17C4X Product Identification System" at the back of this data sheet to specify the correct part number.

For the PIC17C4X family of devices, there are four device "types" as indicated in the device number:

1. **C**, as in PIC17**C**42. These devices have EPROM type memory and operate over the standard voltage range.
2. **LC**, as in PIC17**LC**42. These devices have EPROM type memory, operate over an extended voltage range, and reduced frequency range.
3. **CR**, as in PIC17**CR**42. These devices have ROM type memory and operate over the standard voltage range.
4. **LCR**, as in PIC17**LCR**42. These devices have ROM type memory, operate over an extended voltage range, and reduced frequency range.

### 2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package, is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the configuration modes. Microchip's PRO MATE™ programmer supports programming of the PIC17C4X. Third party programmers also are available; refer to the *Third Party Guide* for a list of sources.

### 2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

### 2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

### 2.4 Serialized Quick-Turnaround Production (SQTP$^{SM}$) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

ROM devices do not allow serialization information in the program memory space.

For information on submitting ROM code, please contact your regional sales office.

### 2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, thus giving customers a low cost option for high volume, mature products.

For information on submitting ROM code, please contact your regional sales office.

**TABLE 9-7: PORTD FUNCTIONS**

| Name | Bit | Buffer Type | Function |
|---|---|---|---|
| RD0/AD8 | bit0 | TTL | Input/Output or system bus address/data pin. |
| RD1/AD9 | bit1 | TTL | Input/Output or system bus address/data pin. |
| RD2/AD10 | bit2 | TTL | Input/Output or system bus address/data pin. |
| RD3/AD11 | bit3 | TTL | Input/Output or system bus address/data pin. |
| RD4/AD12 | bit4 | TTL | Input/Output or system bus address/data pin. |
| RD5/AD13 | bit5 | TTL | Input/Output or system bus address/data pin. |
| RD6/AD14 | bit6 | TTL | Input/Output or system bus address/data pin. |
| RD7/AD15 | bit7 | TTL | Input/Output or system bus address/data pin. |

Legend: TTL = TTL input.

**TABLE 9-8: REGISTERS/BITS ASSOCIATED WITH PORTD**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset | Value on all other resets (Note1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 13h, Bank 1 | PORTD | RD7/ AD15 | RD6/ AD14 | RD5/ AD13 | RD4/ AD12 | RD3/ AD11 | RD2/ AD10 | RD1/ AD9 | RD0/ AD8 | xxxx xxxx | uuuu uuuu |
| 12h, Bank 1 | DDRD | Data direction register for PORTD | | | | | | | | 1111 1111 | 1111 1111 |

Legend: x = unknown, u = unchanged.

Note 1: Other (non power-up) resets include: external reset through $\overline{\text{MCLR}}$ and the Watchdog Timer Reset.

### 12.1.3 USING PULSE WIDTH MODULATION (PWM) OUTPUTS WITH TMR1 AND TMR2

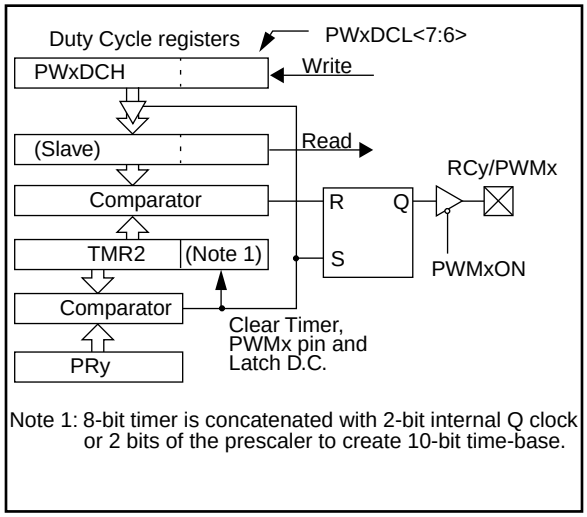
Two high speed pulse width modulation (PWM) outputs are provided. The PWM1 output uses Timer1 as its time-base, while PWM2 may be software configured to use either Timer1 or Timer2 as the time-base. The PWM outputs are on the RB2/PWM1 and RB3/PWM2 pins.

Each PWM output has a maximum resolution of 10-bits. At 10-bit resolution, the PWM output frequency is 24.4 kHz (@ 25 MHz clock) and at 8-bit resolution the PWM output frequency is 97.7 kHz. The duty cycle of the output can vary from 0% to 100%.

Figure 12-5 shows a simplified block diagram of the PWM module. The duty cycle register is double buffered for glitch free operation. Figure 12-6 shows how a glitch could occur if the duty cycle registers were not double buffered.

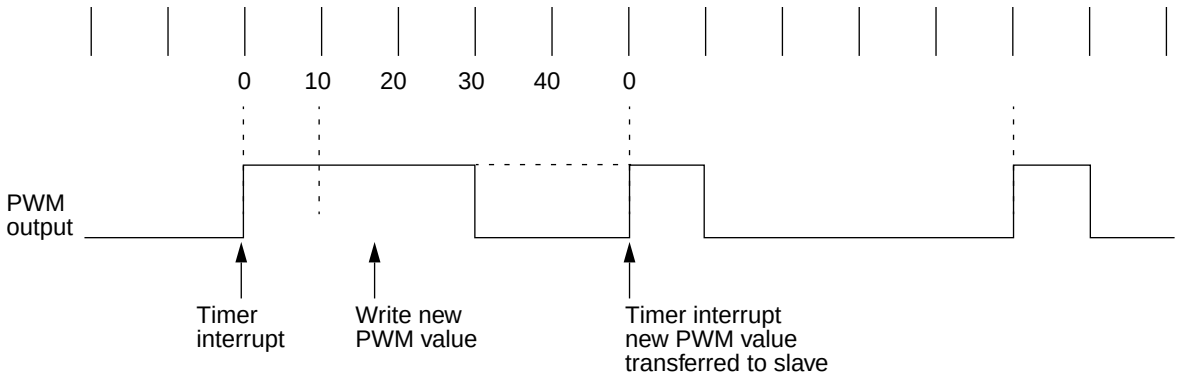
The user needs to set the PWM1ON bit (TCON2<4>) to enable the PWM1 output. When the PWM1ON bit is set, the RB2/PWM1 pin is configured as PWM1 output and forced as an output irrespective of the data direction bit (DDRB<2>). When the PWM1ON bit is clear, the pin behaves as a port pin and its direction is controlled by its data direction bit (DDRB<2>). Similarly, the PWM2ON (TCON2<5>) bit controls the configuration of the RB3/PWM2 pin.

**FIGURE 12-5: SIMPLIFIED PWM BLOCK DIAGRAM**




Note 1: 8-bit timer is concatenated with 2-bit internal Q clock or 2 bits of the prescaler to create 10-bit time-base.

**FIGURE 12-6: PWM OUTPUT**




Note The dotted line shows PWM output if duty cycle registers were not double buffered. If the new duty cycle is written after the timer has passed that value, then the PWM does not reset at all during the current cycle causing a “glitch”.

In this example, PWM period = 50. Old duty cycle is 30. New duty cycle value is 10.

12.1.3.3.1 MAX RESOLUTION/FREQUENCY FOR EXTERNAL CLOCK INPUT

The use of an external clock for the PWM time-base (Timer1 or Timer2) limits the PWM output to a maximum resolution of 8-bits. The PWxDCL<7:6> bits must be kept cleared. Use of any other value will distort the PWM output. All resolutions are supported when internal clock mode is selected. The maximum attainable frequency is also lower. This is a result of the timing requirements of an external clock input for a timer (see the Electrical Specification section). The maximum PWM frequency, when the timers clock source is the RB4/TCLK12 pin, is shown in Table 12-3 (standard resolution mode).

## 12.2 Timer3

Timer3 is a 16-bit timer consisting of the TMR3H and TMR3L registers. TMR3H is the high byte of the timer and TMR3L is the low byte. This timer has an associated 16-bit period register (PR3H/CA1H:PR3L/CA1L). This period register can be software configured to be a second 16-bit capture register.

When the TMR3CS bit (TCON1<2>) is clear, the timer increments every instruction cycle (Fosc/4). When TMR3CS is set, the timer increments on every falling edge of the RB5/TCLK3 pin. In either mode, the TMR3ON bit must be set for the timer to increment. When TMR3ON is clear, the timer will not increment or set the TMR3IF bit.

Timer3 has two modes of operation, depending on the CA1/$\overline{PR3}$ bit (TCON2<3>). These modes are:

- One capture and one period register mode
- Dual capture register mode

The PIC17C4X has up to two 16-bit capture registers that capture the 16-bit value of TMR3 when events are detected on capture pins. There are two capture pins (RB0/CAP1 and RB1/CAP2), one for each capture register. The capture pins are multiplexed with PORTB pins. An event can be:

- a rising edge
- a falling edge
- every 4th rising edge
- every 16th rising edge

Each 16-bit capture register has an interrupt flag associated with it. The flag is set when a capture is made. The capture module is truly part of the Timer3 block. Figure 12-7 and Figure 12-8 show the block diagrams for the two modes of operation.

**TABLE 12-4: REGISTERS/BITS ASSOCIATED WITH PWM**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset | Value on all other resets (Note1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 16h, Bank 3 | TCON1 | CA2ED1 | CA2ED0 | CA1ED1 | CA1ED0 | T16 | TMR3CS | TMR2CS | TMR1CS | 0000 0000 | 0000 0000 |
| 17h, Bank 3 | TCON2 | CA2OVF | CA1OVF | PWM2ON | PWM1ON | CA1/$\overline{PR3}$ | TMR3ON | TMR2ON | TMR1ON | 0000 0000 | 0000 0000 |
| 10h, Bank 2 | TMR1 | Timer1 register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 11h, Bank 2 | TMR2 | Timer2 register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 16h, Bank 1 | PIR | RBIF | TMR3IF | TMR2IF | TMR1IF | CA2IF | CA1IF | TXIF | RCIF | 0000 0010 | 0000 0010 |
| 17h, Bank 1 | PIE | RBIE | TMR3IE | TMR2IE | TMR1IE | CA2IE | CA1IE | TXIE | RCIE | 0000 0000 | 0000 0000 |
| 07h, Unbanked | INTSTA | PEIF | T0CKIF | T0IF | INTF | PEIE | T0CKIE | T0IE | INTE | 0000 0000 | 0000 0000 |
| 06h, Unbanked | CPUSTA | — | — | STKAV | GLINTD | $\overline{TO}$ | $\overline{PD}$ | — | — | --11 11-- | --11 qq-- |
| 10h, Bank 3 | PW1DCL | DC1 | DC0 | — | — | — | — | — | — | xx-- ---- | uu-- ---- |
| 11h, Bank 3 | PW2DCL | DC1 | DC0 | TM2PW2 | — | — | — | — | — | xx0- ---- | uu0- ---- |
| 12h, Bank 3 | PW1DCH | DC9 | DC8 | DC7 | DC6 | DC5 | DC4 | DC3 | DC2 | xxxx xxxx | uuuu uuuu |
| 13h, Bank 3 | PW2DCH | DC9 | DC8 | DC7 | DC6 | DC5 | DC4 | DC3 | DC2 | xxxx xxxx | uuuu uuuu |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends on conditions, shaded cells are not used by PWM.

**NOTES:**

## 14.1 Configuration Bits

The PIC17CXX has up to seven configuration locations (Table 14-1). These locations can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. Any write to a configuration location, regardless of the data, will program that configuration bit. A TABLWT instruction is required to write to program memory locations. The configuration bits can be read by using the TABLRD instructions. Reading any configuration location between FE00h and FE07h will read the low byte of the configuration word (Figure 14-1) into the TABLATL register. The TABLATH register will be FFh. Reading a configuration location between FE08h and FE0Fh will read the high byte of the configuration word into the TABLATL register. The TABLATH register will be FFh.

Addresses FE00h thorough FE0Fh are only in the program memory space for microcontroller and code protected microcontroller modes. A device programmer will be able to read the configuration word in any processor mode. See programming specifications for more detail.

**TABLE 14-1: CONFIGURATION LOCATIONS**

| Bit | Address |
|---|---|
| FOSC0 | FE00h |
| FOSC1 | FE01h |
| WDTPS0 | FE02h |
| WDTPS1 | FE03h |
| PM0 | FE04h |
| PM1 | FE06h |
| PM2 (1) | FE0Fh (1) |

Note 1: This location does not exist on the PIC17C42.

| | |
|---|---|
| **Note:** | When programming the desired configuration locations, they must be programmed in ascending order. Starting with address FE00h. |

## 14.2 Oscillator Configurations

### 14.2.1 OSCILLATOR TYPES

The PIC17CXX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

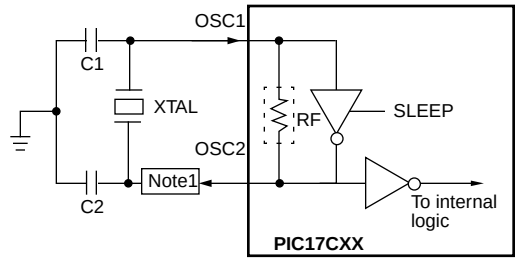
- LF: Low Power Crystal
- XT: Crystal/Resonator
- EC: External Clock Input
- RC: Resistor/Capacitor

### 14.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT or LF modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 14-2). The PIC17CXX Oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications.

For frequencies above 20 MHz, it is common for the crystal to be an overtone mode crystal. Use of overtone mode crystals require a tank circuit to attenuate the gain at the fundamental frequency. Figure 14-3 shows an example of this.

**FIGURE 14-2: CRYSTAL OR CERAMIC RESONATOR OPERATION (XT OR LF OSC CONFIGURATION)**




See Table 14-2 and Table 14-3 for recommended values of C1 and C2.

Note 1: A series resistor may be required for AT strip cut crystals.

**INFSNZ** **Increment f, skip if not 0**

Syntax: [*label*] INFSNZ f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) + 1 → (dest), skip if not 0

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 0010 | 010d | ffff | ffff |

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is placed back in register 'f'.
If the result is not 0, the next instruction, which is already fetched, is discarded, and an NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Execute | Write to destination |

If skip:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Forced NOP | NOP | Execute | NOP |

Example:
```
HERE    INFSNZ  REG, 1
ZERO
NZERO
```

Before Instruction
REG = REG

After Instruction
REG = REG + 1
If REG = 1;
PC = Address (ZERO)
If REG = 0;
PC = Address (NZERO)

**IORLW** **Inclusive OR Literal with WREG**

Syntax: [ *label* ] IORLW k

Operands: $0 \le k \le 255$

Operation: (WREG) .OR. (k) → (WREG)

Status Affected: Z

Encoding:

| | | | |
|---|---|---|---|
| 1011 | 0011 | kkkk | kkkk |

Description: The contents of WREG are OR'ed with the eight bit literal 'k'. The result is placed in WREG.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read literal 'k' | Execute | Write to WREG |

Example:
```
IORLW   0x35
```

Before Instruction
WREG = 0x9A

After Instruction
WREG = 0xBF

**SUBWF** **Subtract WREG from f**

Syntax: [ *label* ] SUBWF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) – (W) → (dest)

Status Affected: OV, C, DC, Z

Encoding:

| | | | |
|---|---|---|---|
| 0000 | 010d | ffff | ffff |

Description: Subtract WREG from register 'f' (2's complement method). If 'd' is 0 the result is stored in WREG. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Execute | Write to destination |

Example 1:
```
SUBWF   REG1, 1
```
Before Instruction
```
REG1    =   3
WREG    =   2
C       =   ?
```
After Instruction
```
REG1    =   1
WREG    =   2
C       =   1     ; result is positive
Z       =   0
```
Example 2:

Before Instruction
```
REG1    =   2
WREG    =   2
C       =   ?
```
After Instruction
```
REG1    =   0
WREG    =   2
C       =   1     ; result is zero
Z       =   1
```
Example 3:

Before Instruction
```
REG1    =   1
WREG    =   2
C       =   ?
```
After Instruction
```
REG1    =   FF
WREG    =   2
C       =   0     ; result is negative
Z       =   0
```

**SUBWFB** **Subtract WREG from f with Borrow**

Syntax: [ *label* ] SUBWFB f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) – (W) – $\overline{C}$ → (dest)

Status Affected: OV, C, DC, Z

Encoding:

| | | | |
|---|---|---|---|
| 0000 | 001d | ffff | ffff |

Description: Subtract WREG and the carry flag (borrow) from register 'f' (2's complement method). If 'd' is 0 the result is stored in WREG. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Execute | Write to destination |

Example 1:
```
SUBWFB  REG1, 1
```
Before Instruction
```
REG1    =   0x19    (0001 1001)
WREG    =   0x0D    (0000 1101)
C       =   1
```
After Instruction
```
REG1    =   0x0C    (0000 1011)
WREG    =   0x0D    (0000 1101)
C       =   1       ; result is positive
Z       =   0
```
Example2:
```
SUBWFB  REG1,0
```
Before Instruction
```
REG1    =   0x1B    (0001 1011)
WREG    =   0x1A    (0001 1010)
C       =   0
```
After Instruction
```
REG1    =   0x1B    (0001 1011)
WREG    =   0x00
C       =   1       ; result is zero
Z       =   1
```
Example3:
```
SUBWFB  REG1,1
```
Before Instruction
```
REG1    =   0x03    (0000 0011)
WREG    =   0x0E    (0000 1101)
C       =   1
```
After Instruction
```
REG1    =   0xF5    (1111 0100) [2's comp]
WREG    =   0x0E    (0000 1101)
C       =   0       ; result is negative
Z       =   0
```

**TLWT** **Table Latch Write**

Syntax: [ *label* ] TLWT t,f

Operands: $0 \le f \le 255$
$t \in [0,1]$

Operation: If t = 0,
$f \rightarrow$ TBLATL;
If t = 1,
$f \rightarrow$ TBLATH

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 1010 | 01tx | ffff | ffff |

Description: Data from file register 'f' is written into the 16-bit table latch (TBLAT).
If t = 1; high byte is written
If t = 0; low byte is written
This instruction is used in conjunction with TABLWT to transfer data from data memory to program memory.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Execute | Write register TBLATH or TBLATL |

Example:
```
TLWT    t, RAM
```
Before Instruction
t = 0
RAM = 0xB7
TBLAT = 0x0000 (TBLATH = 0x00)
(TBLATL = 0x00)

After Instruction
RAM = 0xB7
TBLAT = 0x00B7 (TBLATH = 0x00)
(TBLATL = 0xB7)

Before Instruction
t = 1
RAM = 0xB7
TBLAT = 0x0000 (TBLATH = 0x00)
(TBLATL = 0x00)

After Instruction
RAM = 0xB7
TBLAT = 0xB700 (TBLATH = 0xB7)
(TBLATL = 0x00)

**TSTFSZ** **Test f, skip if 0**

Syntax: [ *label* ] TSTFSZ f

Operands: $0 \le f \le 255$

Operation: skip if f = 0

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 0011 | 0011 | ffff | ffff |

Description: If 'f' = 0, the next instruction, fetched during the current instruction execution, is discarded and an NOP is executed making this a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Execute | NOP |

If skip:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Forced NOP | NOP | Execute | NOP |

Example:
```
HERE    TSTFSZ  CNT
NZERO   :
ZERO    :
```
Before Instruction
PC = Address(HERE)

After Instruction
If CNT = 0x00,
PC = Address (ZERO)
If CNT ≠ 0x00,
PC = Address (NZERO)

### 16.6 PICDEM-1 Low-Cost PIC16/17 Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-16B programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the PICMASTER emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

### 16.7 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-16C, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the $I^2C$ bus and separate headers for connection to an LCD module and a keypad.

### 16.8 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals. PICDEM-3 will be available in the 3rd quarter of 1996.

### 16.9 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
  - editor
  - emulator
  - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC16/17 tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
- Transfer data dynamically via DDE (soon to be replaced by OLE)
- Run up to four emulators on the same PC

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

### 16.10 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

## 17.0 PIC17C42 ELECTRICAL CHARACTERISTICS

**Absolute Maximum Ratings †**

Ambient temperature under bias ..... -55 to +125˚C

Storage temperature ..... -65˚C to +150˚C

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ (Note 2) ..... -0.6V to +14V

Voltage on RA2 and RA3 with respect to $V_{SS}$ ..... -0.6V to +12V

Voltage on all other pins with respect to $V_{SS}$ ..... -0.6V to $V_{DD}$ + 0.6V

Total power dissipation (Note 1) ..... 1.0W

Maximum current out of $V_{SS}$ pin(s) - Total ..... 250 mA

Maximum current into $V_{DD}$ pin(s) - Total ..... 200 mA

Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA

Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA

Maximum output current sunk by any I/O pin (except RA2 and RA3) ..... 35 mA

Maximum output current sunk by RA2 or RA3 pins ..... 60 mA

Maximum output current sourced by any I/O pin ..... 20 mA

Maximum current sunk by PORTA and PORTB (combined) ..... 150 mA

Maximum current sourced by PORTA and PORTB (combined) ..... 100 mA

Maximum current sunk by PORTC, PORTD and PORTE (combined) ..... 150 mA

Maximum current sourced by PORTC, PORTD and PORTE (combined) ..... 100 mA

**Note 1:** Power dissipation is calculated as follows: $Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

**Note 2:** Voltage spikes below $V_{SS}$ at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to $V_{SS}$.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

**FIGURE 17-7: CAPTURE TIMINGS**

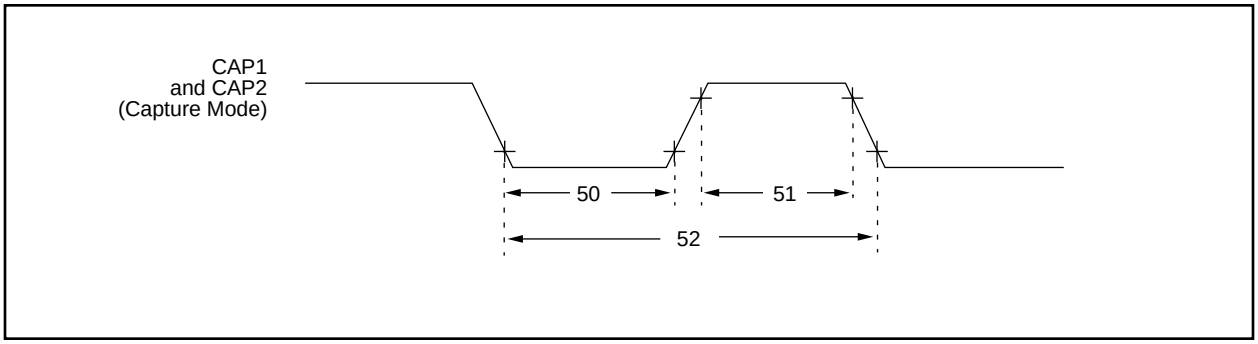



**TABLE 17-7: CAPTURE REQUIREMENTS**

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 50 | TccL | Capture1 and Capture2 input low time | 10 * | — | — | ns | |
| 51 | TccH | Capture1 and Capture2 input high time | 10 * | — | — | ns | |
| 52 | TccP | Capture1 and Capture2 input period | $\frac{2\ T_{CY}}{N}$ § | — | — | ns | N = prescale value (4 or 16) |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

**FIGURE 17-8: PWM TIMINGS**

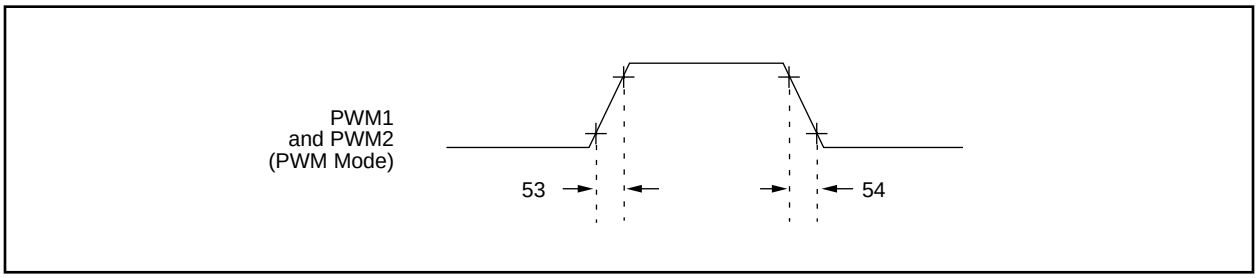



**TABLE 17-8: PWM REQUIREMENTS**

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 53 | TccR | PWM1 and PWM2 output rise time | — | 10 * | 35 *§ | ns | |
| 54 | TccF | PWM1 and PWM2 output fall time | — | 10 * | 35 *§ | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

**FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**

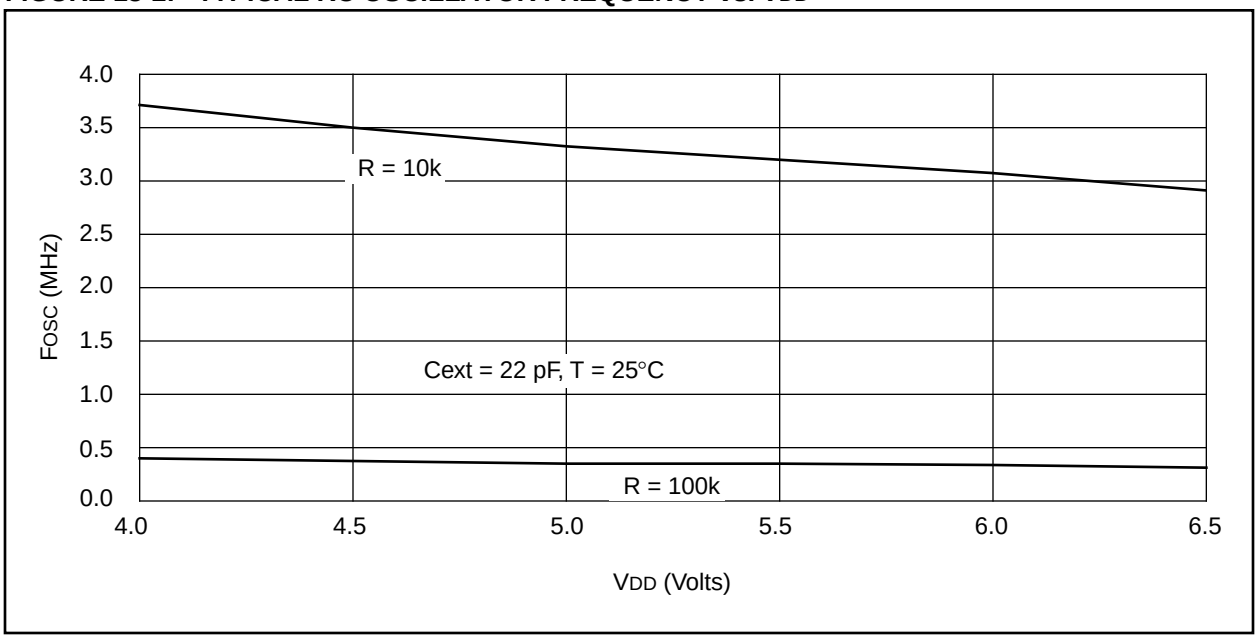
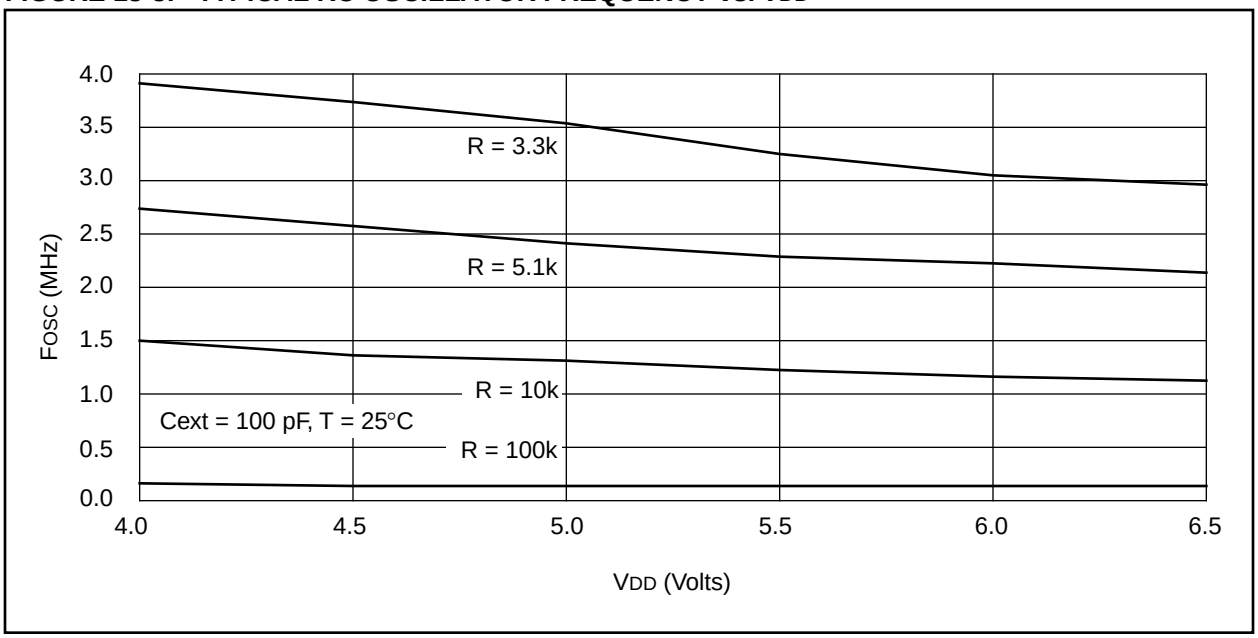



**FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**



| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

**TABLE 19-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)**

| OSC | PIC17LCR42-08<br>PIC17LC42A-08<br>PIC17LC43-08<br>PIC17LCR43-08<br>PIC17LC44-08 | PIC17CR42-16<br>PIC17C42A-16<br>PIC17C43-16<br>PIC17CR43-16<br>PIC17C44-16 | PIC17CR42-25<br>PIC17C42A-25<br>PIC17C43-25<br>PIC17CR43-25<br>PIC17C44-25 | PIC17CR42-33<br>PIC17C42A-33<br>PIC17C43-33<br>PIC17CR43-33<br>PIC17C44-33 | JW Devices<br>(Ceramic Windowed Devices) |
|---|---|---|---|---|---|
| RC | VDD: 2.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 6 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 4 MHz max. |
| XT | VDD: 2.5V to 6.0V<br>IDD: 12 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 8 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 24 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 16 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 25 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. |
| EC | VDD: 2.5V to 6.0V<br>IDD: 12 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 8 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 24 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 16 MHz Max | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 25 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 38 mA max.<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 33 MHz max. |
| LF | VDD: 2.5V to 6.0V<br>IDD: 150 µA max. at 32 kHz<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 95 µA typ. at 32 kHz<br>IPD: < 1 µA typ. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 95 µA typ. at 32 kHz<br>IPD: < 1 µA typ. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 4.5V to 6.0V<br>IDD: 95 µA typ. at 32 kHz<br>IPD: < 1 µA typ. at 5.5V WDT disabled<br>Freq: 2 MHz max. | VDD: 2.5V to 6.0V<br>IDD: 150 µA max. at 32 kHz<br>IPD: 5 µA max. at 5.5V WDT disabled<br>Freq: 2 MHz max. |

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

## 19.3 DC CHARACTERISTICS: PIC17CR42/42A/43/R43/44-16 (Commercial, Industrial) PIC17CR42/42A/43/R43/44-25 (Commercial, Industrial) PIC17CR42/42A/43/R43/44-33 (Commercial, Industrial) PIC17LCR42/42A/43/R43/44-08 (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature<br>-40°C ≤ TA ≤ +85°C for industrial and<br>0°C ≤ TA ≤ +70°C for commercial<br>Operating voltage VDD range as described in Section 19.1 | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter No.** | **Sym** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | | **Input Low Voltage** | | | | | |
| | VIL | I/O ports | | | | | |
| D030 | | with TTL buffer | VSS | – | 0.8 | V | 4.5V ≤ VDD ≤ 5.5V |
| | | | VSS | – | 0.2VDD | V | 2.5V ≤ VDD ≤ 4.5V |
| D031 | | with Schmitt Trigger buffer | VSS | – | 0.2VDD | V | |
| D032 | | $\overline{MCLR}$, OSC1 (in EC and RC mode) | Vss | – | 0.2VDD | V | Note1 |
| D033 | | OSC1 (in XT, and LF mode) | – | 0.5VDD | – | V | |
| | | **Input High Voltage** | | | | | |
| | VIH | I/O ports | | | | | |
| D040 | | with TTL buffer | 2.0 | – | VDD | V | 4.5V ≤ VDD ≤ 5.5V |
| | | | 1 + 0.2VDD | – | VDD | V | 2.5V ≤ VDD ≤ 4.5V |
| D041 | | with Schmitt Trigger buffer | 0.8VDD | – | VDD | V | |
| D042 | | $\overline{MCLR}$ | 0.8VDD | – | VDD | V | Note1 |
| D043 | | OSC1 (XT, and LF mode) | – | 0.5VDD | – | V | |
| D050 | VHYS | Hysteresis of Schmitt Trigger inputs | 0.15VDD * | – | – | V | |
| | | **Input Leakage Current** (Notes 2, 3) | | | | | |
| D060 | IIL | I/O ports (except RA2, RA3) | – | – | ±1 | µA | Vss ≤ VPIN ≤ VDD, I/O Pin at hi-impedance PORTB weak pull-ups disabled |
| D061 | | $\overline{MCLR}$ | – | – | ±2 | µA | VPIN = Vss or VPIN = VDD |
| D062 | | RA2, RA3 | | | ±2 | µA | Vss ≤ VRA2, VRA3 ≤ 12V |
| D063 | | OSC1, TEST (EC, RC modes) | – | – | ±1 | µA | Vss ≤ VPIN ≤ VDD |
| D063B | | OSC1, TEST (XT, LF modes) | – | – | VPIN | µA | RF ≥ 1 MΩ, see Figure 14.2 |
| D064 | | $\overline{MCLR}$ | – | – | 10 | µA | VMCLR = VPP = 12V (when not programming) |
| D070 | IPURB | PORTB weak pull-up current | 60 | 200 | 400 | µA | VPIN = VSS, $\overline{RBPU}$ = 0<br>4.5V ≤ VDD ≤ 6.0V |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

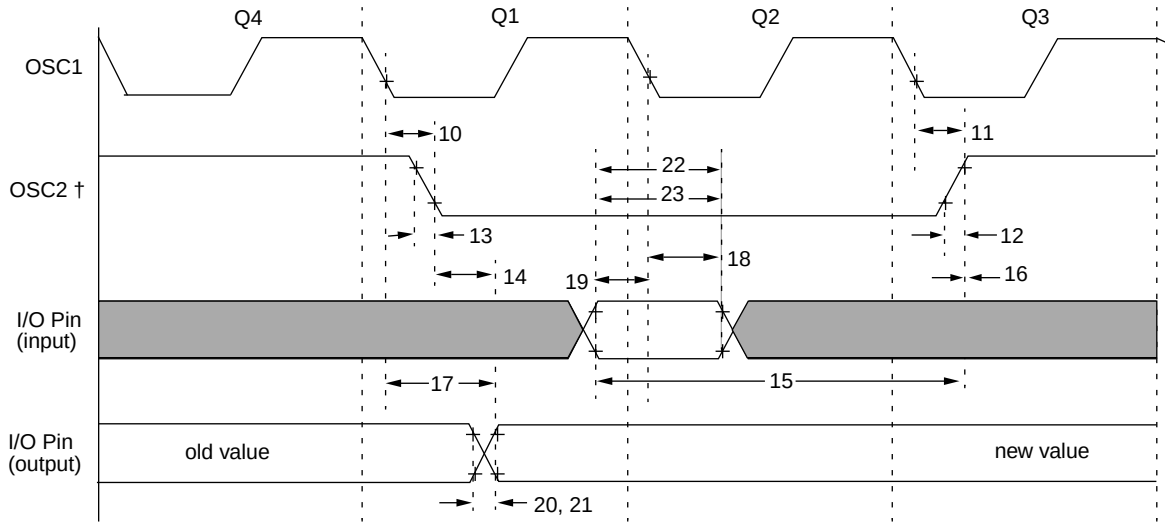
4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17CXX Programming Specifications (Literature number DS30139).

5: The $\overline{MCLR}$/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

**FIGURE 19-3: CLKOUT AND I/O TIMING**




† In EC and RC modes only.

**TABLE 19-3: CLKOUT AND I/O TIMING REQUIREMENTS**

| Parameter No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 10 | TosH2ckL | OSC1↓ to CLKOUT↓ | | — | 15 ‡ | 30 ‡ | ns | Note 1 |
| 11 | TosH2ckH | OSC1↓ to CLKOUT↑ | | — | 15 ‡ | 30 ‡ | ns | Note 1 |
| 12 | TckR | CLKOUT rise time | | — | 5 ‡ | 15 ‡ | ns | Note 1 |
| 13 | TckF | CLKOUT fall time | | — | 5 ‡ | 15 ‡ | ns | Note 1 |
| 14 | TckH2ioV | CLKOUT ↑ to Port out valid | PIC17CR42/42A/43/ R43/44 | — | — | 0.5TCY + 20 ‡ | ns | Note 1 |
| | | | PIC17LCR42/42A/43/ R43/44 | — | — | 0.5TCY + 50 ‡ | ns | Note 1 |
| 15 | TioV2ckH | Port in valid before CLKOUT↑ | PIC17CR42/42A/43/ R43/44 | 0.25TCY + 25 ‡ | — | — | ns | Note 1 |
| | | | PIC17LCR42/42A/43/ R43/44 | 0.25TCY + 50 ‡ | — | — | ns | Note 1 |
| 16 | TckH2ioI | Port in hold after CLKOUT↑ | | 0 ‡ | — | — | ns | Note 1 |
| 17 | TosH2ioV | OSC1↓ (Q1 cycle) to Port out valid | | — | — | 100 ‡ | ns | |
| 18 | TosH2ioI | OSC1↓ (Q2 cycle) to Port input invalid (I/O in hold time) | | 0 ‡ | — | — | ns | |
| 19 | TioV2osH | Port input valid to OSC1↓ (I/O in setup time) | | 30 ‡ | — | — | ns | |
| 20 | TioR | Port output rise time | | — | 10 ‡ | 35 ‡ | ns | |
| 21 | TioF | Port output fall time | | — | 10 ‡ | 35 ‡ | ns | |
| 22 | TinHL | INT pin high or low time | | 25 * | — | — | ns | |
| 23 | TrbHL | RB7:RB0 change INT high or low time | | 25 * | — | — | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Measurements are taken in EC Mode where CLKOUT output is 4 x TOSC.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

**FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER TIMING**

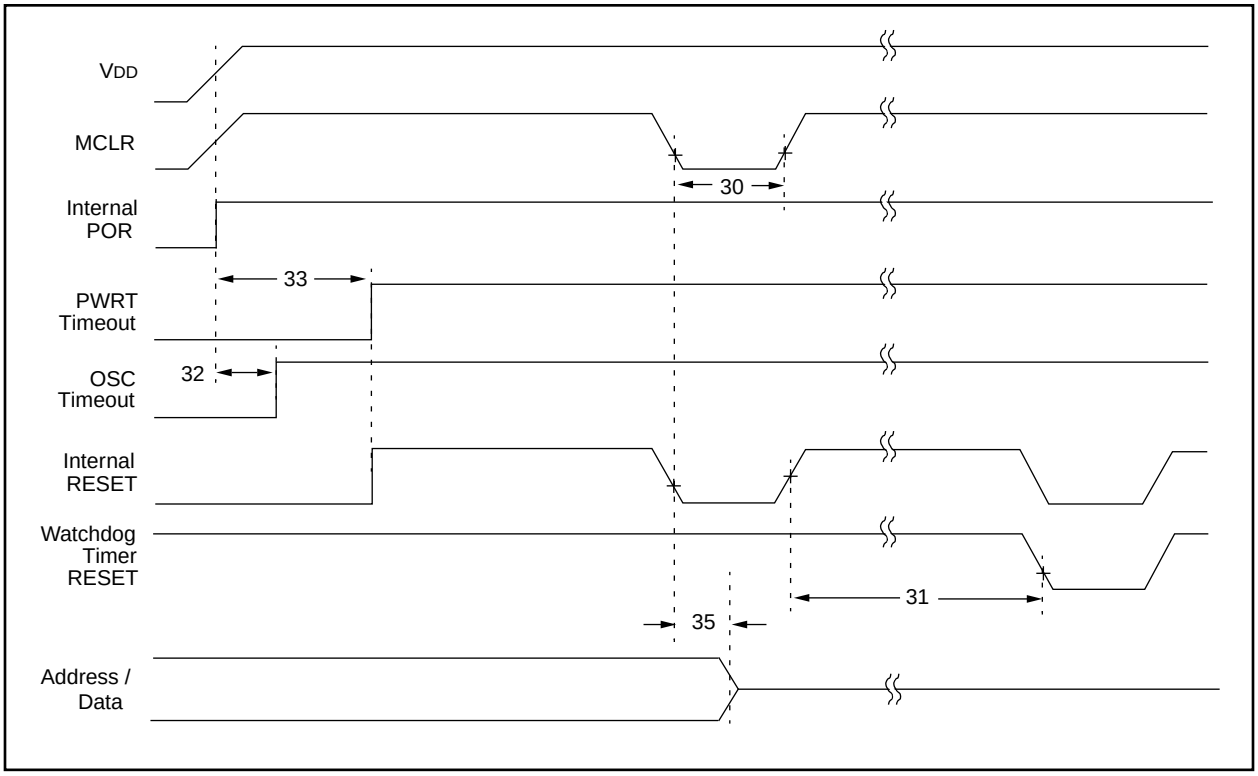



**TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS**

| Parameter No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | | 100 * | — | — | ns | VDD = 5V |
| 31 | Twdt | Watchdog Timer Time-out Period (Prescale = 1) | | 5 * | 12 | 25 * | ms | VDD = 5V |
| 32 | Tost | Oscillation Start-up Timer Period | | — | 1024TOSC§ | — | ms | TOSC = OSC1 period |
| 33 | Tpwrt | Power-up Timer Period | | 40 * | 96 | 200 * | ms | VDD = 5V |
| 35 | TmcL2adl | $\overline{\text{MCLR}}$ to System Interface bus (AD15:AD0>) invalid | PIC17CR42/42A/43/R43/44 | — | — | 100 * | ns | |
| | | | PIC17LCR42/42A/43/R43/44 | — | — | 120 * | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

§ This specification ensured by design.

| Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44 |
|---|---|---|---|---|---|---|

**FIGURE 20-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**

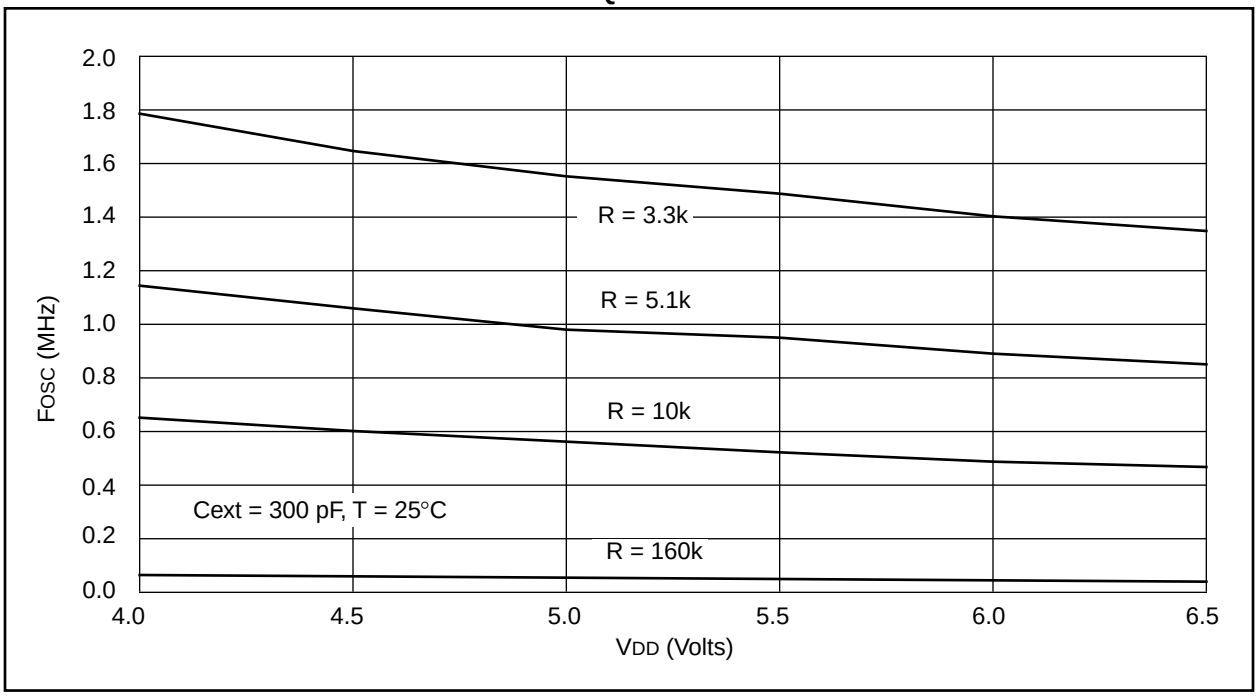



**TABLE 20-2: RC OSCILLATOR FREQUENCIES**

| Cext | Rext | Average Fosc @ 5V, 25°C | |
|---|---|---|---|
| 22 pF | 10k | 3.33 MHz | ± 12% |
| | 100k | 353 kHz | ± 13% |
| 100 pF | 3.3k | 3.54 MHz | ± 10% |
| | 5.1k | 2.43 MHz | ± 14% |
| | 10k | 1.30 MHz | ± 17% |
| | 100k | 129 kHz | ± 10% |
| 300 pF | 3.3k | 1.54 MHz | ± 14% |
| | 5.1k | 980 kHz | ± 12% |
| | 10k | 564 kHz | ± 16% |
| | 160k | 35 kHz | ± 18% |

## E.7 PIC16C9XX Family Of Devices

| | Clock | Memory | | | Peripherals | | | | | | | Features | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Maximum Frequency of Operation (MHz) | Program Memory | EPROM | Data Memory (bytes) | Timer Module(s) | Capture/Compare/PWM Module(s) | Serial Port(s) (SPI/I²C, USART) | Parallel Slave Port | A/D Converter (8-bit) Channels | LCD Module | Interrupt Sources | I/O Pins | Input Pins | Voltage Range (Volts) | In-Circuit Serial Programming | Brown-out Reset | Packages |
| PIC16C923 | 8 | 4K | 176 | | TMR0, TMR1, TMR2 | 1 | SPI/I²C | — | — | 4 Com 32 Seg | 8 | 25 | 27 | 3.0-6.0 | Yes | — | 64-pin SDIP(1), TQFP, 68-pin PLCC, DIE |
| PIC16C924 | 8 | 4K | 176 | | TMR0, TMR1, TMR2 | 1 | SPI/I²C | — | 5 | 4 Com 32 Seg | 9 | 25 | 27 | 3.0-6.0 | Yes | — | 64-pin SDIP(1), TQFP, 68-pin PLCC, DIE |

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.
All PIC16CXX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip representative for availability of this package.

**LIST OF EQUATIONS**