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#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	33
Program Memory Size	16KB (8K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	454 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c44t-16e-pt

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# TABLE 1-1: PIC17CXX FAMILY OF DEVICES

Features		PIC17C42	PIC17CR42	PIC17C42A	PIC17C43	PIC17CR43	PIC17C44
Maximum Frequency of O	peration	25 MHz	33 MHz	33 MHz	33 MHz	33 MHz	33 MHz
Operating Voltage Range		4.5 - 5.5V	2.5 - 6.0V	2.5 - 6.0V	2.5 - 6.0V	2.5 - 6.0V 2.5 - 6.0V	
Program Memory x16	(EPROM)	2K	-	2K	4K	-	8K
	(ROM)	-	2K	-	-	4K	-
Data Memory (bytes)		232	232	232	454	454	454
Hardware Multiplier (8 x 8)	)	-	Yes	Yes	Yes	Yes	Yes
Timer0 (16-bit + 8-bit post	scaler)	Yes	Yes	Yes	Yes	Yes	Yes
Timer1 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes
Timer2 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes
Timer3 (16-bit)		Yes	Yes	Yes	Yes	Yes	Yes
Capture inputs (16-bit)		2	2	2	2 2		2
PWM outputs (up to 10-bit	t)	2	2	2	2	2 2	
USART/SCI		Yes	Yes	Yes	Yes	Yes Yes	
Power-on Reset		Yes	Yes	Yes	Yes	Yes Yes	
Watchdog Timer		Yes	Yes	Yes	Yes Yes		Yes
External Interrupts		Yes	Yes	Yes	Yes	Yes Yes	
Interrupt Sources		11	11	11	11	11	11
Program Memory Code Pr	rotect	Yes	Yes	Yes	Yes	Yes	Yes
I/O Pins		33	33	33	33	33	33
I/O High Current Capabil-	Source	25 mA	25 mA				
ity	Sink	25 mA <sup>(1)</sup>	25 mA <sup>(1)</sup>				
Package Types		40-pin DIP	40-pin DIP				
		44-pin PLCC	44-pin PLCC				
		44-pin MQFP	44-pin MQFP				
			44-pin IQFP	44-pin IQFP	44-pin IQFP	44-pin IQFP	44-pin IQFP

Note 1: Pins RA2 and RA3 can sink up to 60 mA.

Name	DIP No.	PLCC No.	QFP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	19	21	37		ST	Oscillator input in crystal/resonator or RC oscillator mode. External clock input in external clock mode.
OSC2/CLKOUT	20	22	38	0	_	Oscillator output. Connects to crystal or resonator in crystal oscillator mode. In RC oscillator or external clock modes OSC2 pin outputs CLKOUT which has one fourth the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/Vpp	32	35	7	I/P	ST	Master clear (reset) input/Programming Voltage (VPP) input. This is the active low reset input to the chip.
						PORTA is a bi-directional I/O Port except for RA0 and RA1 which are input only.
RA0/INT	26	28	44	I	ST	RA0/INT can also be selected as an external interrupt input. Interrupt can be configured to be on positive or negative edge.
RA1/T0CKI	25	27	43	I	ST	RA1/T0CKI can also be selected as an external interrupt input, and the interrupt can be configured to be on posi- tive or negative edge. RA1/T0CKI can also be selected to be the clock input to the Timer0 timer/counter.
RA2	24	26	42	I/O	ST	High voltage, high current, open drain input/output port pins.
RA3	23	25	41	I/O	ST	High voltage, high current, open drain input/output port pins.
RA4/RX/DT	22	24	40	I/O	ST	RA4/RX/DT can also be selected as the USART (SCI) Asynchronous Receive or USART (SCI) Synchronous Data.
RA5/TX/CK	21	23	39	I/O	ST	RA5/TX/CK can also be selected as the USART (SCI) Asynchronous Transmit or USART (SCI) Synchronous Clock.
						PORTB is a bi-directional I/O Port with software configurable weak pull-ups.
RB0/CAP1	11	13	29	I/O	ST	RB0/CAP1 can also be the CAP1 input pin.
RB1/CAP2	12	14	30	I/O	ST	RB1/CAP2 can also be the CAP2 input pin.
RB2/PWM1	13	15	31	I/O	ST	RB2/PWM1 can also be the PWM1 output pin.
RB3/PWM2	14	16	32	I/O	ST	RB3/PWM2 can also be the PWM2 output pin.
RB4/TCLK12	15	17	33	I/O	ST	RB4/TCLK12 can also be the external clock input to
RB5/TCLK3	16	18	34	I/O	ST	Timer1 and Timer2. RB5/TCLK3 can also be the external clock input to Timer3
RB6	17	19	35	1/0	ST	Timero.
RB7	18	20	36	1/0	ST	
						PORTC is a bi-directional I/O Port.
RC0/AD0	2	3	19	I/O	TTL	This is also the lower half of the 16-bit wide system bus
RC1/AD1	3	4	20	I/O	TTL	in microprocessor mode or extended microcontroller
RC2/AD2	4	5	21	I/O	TTL	mode. In multiplexed system bus configuration, these
RC3/AD3	5	6	22	I/O	TTL	pins are address output as well as data input or output.
RC4/AD4	6	7	23	I/O	TTL	
RC5/AD5	7	8	24	I/O	TTL	
RC6/AD6	8	9	25	I/O	TTL	
RC7/AD7	9	10	26	I/O	TTL	

TABLE 3-1:PINOUT DESCRIPTIONS

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input.

## 5.9 Context Saving During Interrupts

During an interrupt, only the returned PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt; e.g. WREG, ALUSTA and the BSR registers. This requires implementation in software. Example 5-1 shows the saving and restoring of information for an interrupt service routine. The PUSH and POP routines could either be in each interrupt service routine or could be subroutines that were called. Depending on the application, other registers may also need to be saved, such as PCLATH.

#### EXAMPLE 5-1: SAVING STATUS AND WREG IN RAM

;							
; The addresses that are used to store the CPUSTA and WREG values							
; must be in the data memory address range of 18h - 1Fh. Up to							
; 8 loca	ations ca	an be saved and restor	red	d using			
; the MG	OVFP inst	truction. This instruc	ti	ion neither affects the status			
; bits,	nor cori	rupts the WREG registe	er.				
;							
;							
PUSH	MOVFP	WREG, TEMP_W	;	Save WREG			
	MOVFP	ALUSTA, TEMP_STATUS	;	Save ALUSTA			
	MOVFP	BSR, TEMP_BSR	;	Save BSR			
ISR	:		;	This is the interrupt service routine			
	:						
POP	MOVFP	TEMP_W, WREG	;	Restore WREG			
	MOVFP	TEMP_STATUS, ALUSTA	;	Restore ALUSTA			
	MOVFP	TEMP_BSR, BSR	;	Restore BSR			
	RETFIE		;	Return from Interrupts enabled			

### 6.3 <u>Stack Operation</u>

The PIC17C4X devices have a 16 x 16-bit wide hardware stack (Figure 6-1). The stack is not part of either the program or data memory space, and the stack pointer is neither readable nor writable. The PC is "PUSHed" onto the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is "POPed" in the event of a RETURN, RETLW, or a RETFIE instruction execution. PCLATH is not affected by a "PUSH" or a "POP" operation.

The stack operates as a circular buffer, with the stack pointer initialized to '0' after all resets. There is a stack available bit (STKAV) to allow software to ensure that the stack has not overflowed. The STKAV bit is set after a device reset. When the stack pointer equals Fh, STKAV is cleared. When the stack pointer rolls over from Fh to 0h, the STKAV bit will be held clear until a device reset.

- **Note 1:** There is not a status bit for stack underflow. The STKAV bit can be used to detect the underflow which results in the stack pointer being at the top of stack.
- Note 2: There are no instruction mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt vector.
- Note 3: After a reset, if a "POP" operation occurs before a "PUSH" operation, the STKAV bit will be cleared. This will appear as if the stack is full (underflow has occurred). If a "PUSH" operation occurs next (before another "POP"), the STKAV bit will be locked clear. Only a device reset will cause this bit to set.

After the device is "PUSHed" sixteen times (without a "POP"), the seventeenth push overwrites the value from the first push. The eighteenth push overwrites the second push (and so on).

## 6.4 Indirect Addressing

Indirect addressing is a mode of addressing data memory where the data memory address in the instruction is not fixed. That is, the register that is to be read or written can be modified by the program. This can be useful for data tables in the data memory. Figure 6-10 shows the operation of indirect addressing. This shows the moving of the value to the data memory address specified by the value of the FSR register.

Example 6-1 shows the use of indirect addressing to clear RAM in a minimum number of instructions. A similar concept could be used to move a defined number of bytes (block) of data to the USART transmit register (TXREG). The starting address of the block of data to be transmitted could easily be modified by the program.

### FIGURE 6-10: INDIRECT ADDRESSING



#### 12.1.3.1 PWM PERIODS

The period of the PWM1 output is determined by Timer1 and its period register (PR1). The period of the PWM2 output can be software configured to use either Timer1 or Timer2 as the time-base. When TM2PW2 bit (PW2DCL<5>) is clear, the time-base is determined by TMR1 and PR1. When TM2PW2 is set, the time-base is determined by Timer2 and PR2.

Running two different PWM outputs on two different timers allows different PWM periods. Running both PWMs from Timer1 allows the best use of resources by freeing Timer2 to operate as an 8-bit timer. Timer1 and Timer2 can not be used as a 16-bit timer if either PWM is being used.

The PWM periods can be calculated as follows:

period of PWM1 =[(PR1) + 1] x 4Tosc

period of PWM2 =[(PR1) + 1] x 4Tosc or [(PR2) + 1] x 4Tosc

The duty cycle of PWMx is determined by the 10-bit value DCx<9:0>. The upper 8-bits are from register PWxDCH and the lower 2-bits are from PWxDCL<7:6> (PWxDCH:PWxDCL<7:6>). Table 12-3 shows the maximum PWM frequency (FPWM) given the value in the period register.

The number of bits of resolution that the PWM can achieve depends on the operation frequency of the device as well as the PWM frequency (FPWM).

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{FOSC}{FPWM}\right)}{\log\left(2\right)} \quad \text{bits}$$

The PWMx duty cycle is as follows:

PWMx Duty Cycle =  $(DCx) \times TOSC$ 

where DCx represents the 10-bit value from PWxDCH:PWxDCL.

If DCx = 0, then the duty cycle is zero. If PRx = PWxDCH, then the PWM output will be low for one to four Q-clock (depending on the state of the PWxDCL<7:6> bits). For a Duty Cycle to be 100%, the PWxDCH value must be greater then the PRx value.

The duty cycle registers for both PWM outputs are double buffered. When the user writes to these registers, they are stored in master latches. When TMR1 (or TMR2) overflows and a new PWM period begins, the master latch values are transferred to the slave latches and the PWMx pin is forced high.

Note:	For PW1DCH, PW1DCL, PW2DCH and
	PW2DCL registers, a write operation
	writes to the "master latches" while a read
	operation reads the "slave latches". As a
	result, the user may not read back what
	was just written to the duty cycle registers.

The user should also avoid any "read-modify-write" operations on the duty cycle registers, such as: ADDWF PW1DCH. This may cause duty cycle outputs that are unpredictable.

TABLE 12-3:	PWM FREQUENCY vs.
	<b>RESOLUTION AT 25 MHz</b>

PWM	Frequency (kHz)						
Frequency	24.4	97.66	390.6				
PRx Value	0xFF	0x7F	0x5F	0x3F	0x0F		
High Resolution	10-bit	9-bit	8.5-bit	8-bit	6-bit		
Standard Resolution	8-bit	7-bit	6.5-bit	6-bit	4-bit		

#### 12.1.3.2 PWM INTERRUPTS

The PWM module makes use of TMR1 or TMR2 interrupts. A timer interrupt is generated when TMR1 or TMR2 equals its period register and is cleared to zero. This interrupt also marks the beginning of a PWM cycle. The user can write new duty cycle values before the timer roll-over. The TMR1 interrupt is latched into the TMR1IF bit and the TMR2 interrupt is latched into the TMR2IF bit. These flags must be cleared in software.

#### 12.1.3.3 EXTERNAL CLOCK SOURCE

The PWMs will operate regardless of the clock source of the timer. The use of an external clock has ramifications that must be understood. Because the external TCLK12 input is synchronized internally (sampled once per instruction cycle), the time TCLK12 changes to the time the timer increments will vary by as much as TCY (one instruction cycle). This will cause jitter in the duty cycle as well as the period of the PWM output.

This jitter will be  $\pm$ TCY, unless the external clock is synchronized with the processor clock. Use of one of the PWM outputs as the clock source to the TCLKx input, will supply a synchronized clock.

In general, when using an external clock source for PWM, its frequency should be much less than the device frequency (Fosc).

### 13.2 USART Asynchronous Mode

In this mode, the USART uses standard nonreturn-to-zero (NRZ) format (one start bit, eight or nine data bits, and one stop bit). The most common data format is 8-bits. An on-chip dedicated 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART's transmitter and receiver are functionally independent but use the same data format and baud rate. The baud rate generator produces a clock x64 of the bit shift rate. Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

The asynchronous mode is selected by clearing the SYNC bit (TXSTA<4>).

The USART Asynchronous module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

#### 13.2.1 USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 13-3. The heart of the transmitter is the transmit shift register (TSR). The shift register obtains its data from the read/write transmit buffer (TXREG). TXREG is loaded with data in software. The TSR is not loaded until the stop bit has been transmitted from the previous load. As soon as the stop bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once TXREG transfers the data to the TSR (occurs in one TCY at the end of the current BRG cycle), the TXREG is empty and an interrupt bit, TXIF (PIR<1>) is set. This interrupt can be enabled or disabled by the TXIE bit (PIE<1>). TXIF will be set regardless of TXIE and cannot be reset in software. It will reset only when new data is loaded into TXREG. While TXIF indicates the status of the TXREG, the TRMT (TXSTA<1>) bit shows the status of the TSR. TRMT is a read only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR is empty.

Note:	The TSR is not mapped in data memory,
	so it is not available to the user.

Transmission enabled setting is by the TXEN (TXSTA<5>) bit. The actual transmission will not occur until TXREG has been loaded with data and the baud rate generator (BRG) has produced a shift clock (Figure 13-5). The transmission can also be started by first loading TXREG and then setting TXEN. Normally when transmission is first started, the TSR is empty, so a transfer to TXREG will result in an immediate transfer to TSR resulting in an empty TXREG. A back-to-back transfer is thus possible (Figure 13-6). Clearing TXEN during a transmission will cause the transmission to be aborted. This will reset the transmitter and the RA5/TX/CK pin will revert to hi-impedance.

In order to select 9-bit transmission, the TX9 (TXSTA<6>) bit should be set and the ninth bit should be written to TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG. This is because a data write to TXREG can result in an immediate transfer of the data to the TSR (if the TSR is empty).

Steps to follow when setting up an Asynchronous Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate.
- 2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
- 3. If interrupts are desired, then set the TXIE bit.
- 4. If 9-bit transmission is desired, then set the TX9 bit.
- 5. Load data to the TXREG register.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in TX9D.
- 7. Enable the transmission by setting TXEN (starts transmission).

Writing the transmit data to the TXREG, then enabling the transmit (setting TXEN) allows transmission to start sooner then doing these two events in the opposite order.

Note: To terminate a transmission, either clear the SPEN bit, or the TXEN bit. This will reset the transmit logic, so that it will be in the proper state when transmit is re-enabled.

MOVFP	Move f to	р		MOVLB	Move Lite	eral to low n	ibble in BSR		
Syntax:	[ <i>label</i> ] N	IOVFP f,p		Syntax:	[ label ]	MOVLB k			
Operands:	$0 \le f \le 255$	5		Operands:	$0 \le k \le 15$	$0 \le k \le 15$			
	$0 \le p \le 31$			Operation:	$k \rightarrow (BSR)$	$k \rightarrow (BSR<3:0>)$			
Operation:	$(f) \to (p)$			Status Affected:	None				
Status Affected:	None			Encoding:	1011	1000 uu	uu kkkk		
Encoding:	011p	pppp ff:	ff ffff	Description:	The four bit	literal 'k' is lo	aded in the		
Description:	Move data from data memory location 'f' to data memory location 'p'. Location 'f' can be anywhere in the 256 word data space (00h to FFh) while 'p' can be 00h to 1Fh.				Bank Select low 4-bits of are affected is unchange encode the	t Register (BS f the Bank Se d. The upper h ed. The assen "u" fields as 'u	SR). Only the elect Register half of the BSR nbler will 0'.		
	Either 'p' or	'f' can be WR	EG (a useful	Words:	1				
special situation).		ful for transfer-	Cycles:	1					
	ring a data memory location to a periph-			Q Cycle Activity:					
	eral registe	r (such as the	transmit buffer	Q1	Q2	Q3	Q4		
	indirectly a	ddressed.	d p can be	Decode	Read	Execute	Write literal		
Words:	1				literal u:k		BSR<3:0>		
Cycles:	1			Example:	MOVLB	0x5	·		
Q Cycle Activity:				Before Instru	uction				
Q1	Q2	Q3	Q4	BSR regi	ister = 0x	22			
Decode	Read register 'f'	Execute	Write register 'p'	After Instruction BSR register = 0x25					
Example:	MOVFP	REG1, REG2		Note: For th	ne PIC17C42	, only the lo	w four bits of		
Before Instru	ction	22		the E mente	BSR registe ed. The uppe	r are phys r nibble is re	ad as '0'.		
REG2	= 0x = 0x	33, 11							
After Instruct REG1	ion = 0x	33,							

REG2

0x33

=

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# FIGURE 17-1: PARAMETER MEASUREMENT INFORMATION

All timings are measure between high and low measurement points as indicated in the figures below.



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# FIGURE 17-5: TIMER0 CLOCK TIMINGS



## TABLE 17-5: TIMER0 CLOCK REQUIREMENTS

Parameter								
No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20 §	—		ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5Tcy + 20 §	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		<u>Tcy + 40</u> §	—	_	ns	N = prescale value
				N				(1, 2, 4,, 256)

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

## FIGURE 17-6: TIMER1, TIMER2, AND TIMER3 CLOCK TIMINGS



# TABLE 17-6: TIMER1, TIMER2, AND TIMER3 CLOCK REQUIREMENTS

Parameter				Тур			
No.	Sym	Characteristic	Min	†	Max	Units	Conditions
45	Tt123H	TCLK12 and TCLK3 high time	0.5 TCY + 20 §	—	—	ns	
46	Tt123L	TCLK12 and TCLK3 low time	0.5 TCY + 20 §	—	_	ns	
47	Tt123P	TCLK12 and TCLK3 input period	<u>Tcy + 40</u> §	—	—	ns	N = prescale value
			N				(1, 2, 4, 8)
48	TckE2tmrl	Delay from selected External Clock Edge to	2Tosc §	—	6 Tosc §	_	
		Timer increment					

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

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FIGURE 18-6: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

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# FIGURE 18-9: TYPICAL IPD vs. VDD WATCHDOG DISABLED 25°C





FIGURE 18-10: MAXIMUM IPD vs. VDD WATCHDOG DISABLED

NOTES:

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# 19.0 PIC17CR42/42A/43/R43/44 ELECTRICAL CHARACTERISTICS

#### Absolute Maximum Ratings †

Ambient temperature under bias	55 to +125°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	0 to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0.6V to +14V
Voltage on RA2 and RA3 with respect to Vss	0.6V to +14V
Voltage on all other pins with respect to Vss	0.6V to VDD + 0.6V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin(s) - total	250 mA
Maximum current into VDD pin(s) - total	200 mA
Input clamp current, Iik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	±20 mA
Maximum output current sunk by any I/O pin (except RA2 and RA3)	35 mA
Maximum output current sunk by RA2 or RA3 pins	60 mA
Maximum output current sourced by any I/O pin	20 mA
Maximum current sunk by PORTA and PORTB (combined)	150 mA
Maximum current sourced by PORTA and PORTB (combined)	100 mA
Maximum current sunk by PORTC, PORTD and PORTE (combined)	150 mA
Maximum current sourced by PORTC, PORTD and PORTE (combined)	100 mA
<b>Note 1:</b> Power dissipation is calculated as follows: Pdis = VDD x {IDD - $\Sigma$ IOH} + $\Sigma$ {(VDD-VOH)	) x IOH} + $\Sigma$ (Vol x IOL)

**Note 2:** Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

**†** NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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#### 19.2 **DC CHARACTERISTICS:**

## PIC17LC42A/43/LC44 (Commercial, Industrial) PIC17LCR42/43 (Commercial, Industrial)

DC CHARA Parameter No.	Operating Min	g tempe	erature Max	-40°C 0°C Units	$\leq$ TA $\leq$ +85°C for industrial and $\leq$ TA $\leq$ +70°C for commercial <b>Conditions</b>		
D001	VDD	Supply Voltage	2.5	-	6.0	V	
D002	VDR	RAM Data Retention Voltage (Note 1)	1.5 *	-	_	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	_	Vss	_	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.060 *	_	_	mV/ms	See section on Power-on Reset for details
D010 D011 D014	IDD	Supply Current (Note 2)	_ _ _	3 6 95	6 12 * 150	mA mA μA	Fosc = 4 MHz (Note 4) Fosc = 8 MHz Fosc = 32 kHz, WDT disabled (EC osc configuration)
D020 D021	IPD	Power-down Current (Note 3)	_	10 < 1	40 5	μΑ μΑ	VDD = 5.5V, WDT enabled VDD = 5.5V, WDT disabled

These parameters are characterized but not tested.

+ Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD or VSS, TOCKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

Current consumed from the oscillator and I/O's driving external capacitive or resistive loads needs to be considered.

For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as: VbD / (2 • R). For capacitive loads, the current can be estimated (for an individual I/O pin) as (CL • VDD) • f

CL = Total capacitive load on the I/O pin; f = average frequency the I/O pin switches.

The capacitive currents are most significant when the device is configured for external execution (includes extended microcontroller mode).

- 3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

Standard Operating Conditions (unloss otherwise stated)

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#### FIGURE 19-3: CLKOUT AND I/O TIMING

TABLE 19-3:	<b>CLKOUT AND I/O TIMING REQUIREMENTS</b>

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
10	TosH2ckL	OSC1↓ to CLKOUT↓		_	15‡	30 ‡	ns	Note 1
11	TosH2ckH	OSC1↓ to CLKOUT	$\uparrow$	_	15‡	30 ‡	ns	Note 1
12	TckR	CLKOUT rise time		—	5‡	15 ‡	ns	Note 1
13	TckF	CLKOUT fall time		—	5‡	15 ‡	ns	Note 1
14	TckH2ioV	CLKOUT 1 to Port PIC17CR42/42A/43/ out valid R43/44		—	_	0.5TCY + 20 ‡	ns	Note 1
			PIC17LCR42/42A/43/ R43/44	_	—	0.5TCY + 50 ‡	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT↑	PIC17CR42/42A/43/ R43/44	0.25Tcy + 25 ‡	_		ns	Note 1
			PIC17LCR42/42A/43/ R43/44	0.25Tcy + 50 ‡	—	—	ns	Note 1
16	TckH2iol	Port in hold after CLKOUT1		0 ‡	—	_	ns	Note 1
17	TosH2ioV	OSC1↓ (Q1 cycle) t	o Port out valid	—	—	100 ‡	ns	
18	TosH2iol	OSC1↓ (Q2 cycle) to Port input invalid (I/O in hold time)		0 ‡	-	—	ns	
19	TioV2osH	Port input valid to OSC1↓ (I/O in setup time)		30 ‡	_	—	ns	
20	TioR	Port output rise time		—	10 ‡	35 ‡	ns	
21	TioF	Port output fall time		_	10 ‡	35 ‡	ns	
22	TinHL	INT pin high or low	time	25 *	—		ns	
23	TrbHL	RB7:RB0 change IN	IT high or low time	25 *	_		ns	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

t These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Measurements are taken in EC Mode where CLKOUT output is 4 x Tosc.

# Applicable Devices 42 R42 42A 43 R43 44





# TABLE 19-4:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP<br/>TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)		100 *	—	—	ns	VDD = 5V
31	Twdt	Watchdog Timer Time-out Period (Prescale = 1)		5*	12	25 *	ms	VDD = 5V
32	Tost	Oscillation Start-up Timer Period		—	1024Tosc§	—	ms	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period		40 *	96	200 *	ms	VDD = 5V
35	TmcL2adl	MCLR to System Inter- ace bus (AD15:AD0>)PIC17CR42/42A/ 43/R43/44		_	—	100 *	ns	
	invalid	PIC17LCR42/ 42A/43/R43/44	—	—	120 *	ns		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

t These parameters are for design guidance only and are not tested, nor characterized.

§ This specification ensured by design.

#### 21.6 **Package Marking Information** 40-Lead PDIP/CERDIP Example PIC17C43-25I/P L006 AABBCDE 9441CCA MICROCHIP MICROCHIP $\bigcirc$ 40 Lead CERDIP Windowed Example XXXXXXXXXXXX PIC17C44 XXXXXXXXXXXX /JW XXXXXXXXXXXX L184 AABBCDE 9444CCT 44-Lead PLCC Example $\mathcal{M}$ $\mathcal{M}$ MICROCHIP MICROCHIP PIC17C42 XXXXXXXXXX ○ <sub>XXXXXXXXX</sub> Ο -16I/L XXXXXXXXXX L013 AABBCDE 9445CCN 44-Lead MQFP Example $\mathcal{M}$ $\mathbf{w}$ XXXXXXXXXX PIC17C44 -25/PT XXXXXXXXXX XXXXXXXXXXX L247 AABBCDE 9450CAT $\cap$ $\cap$ 44-Lead TQFP Example \$ $\mathcal{Q}$ PIC17C44 XXXXXXXXXXX -25/TQ XXXXXXXXXX XXXXXXXXXXX L247 AABBCDE 9450CAT $\cap$ $\cap$ Microchip part number information Legend: MM...M XX...X Customer specific information\* AA Year code (last 2 digits of calendar year) BΒ Week code (week of January 1 is week '01') С Facility code of the plant at which wafer is manufactured C = Chandler, Arizona, U.S.A., S = Tempe, Arizona, U.S.A. D Mask revision number Е Assembly code of the plant or country of origin in which part was assembled Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information. Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond

code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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## PIC17C4X Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

<u>PART NO.</u> – <u>XX X /XX XXX</u>				Examples	
	Pattern:	QTP, SQTP, ROM Code (factory specified) or Special Requirements. Blank for OTP and Windowed devices		a)	PIC17C42 – 16/P Commercial Temp., PDIP package.
	Package:	P JW PQ PT L	<ul> <li>PDIP</li> <li>Windowed CERDIP</li> <li>PDIP (600 mil)</li> <li>MQFP</li> <li>TQFP</li> <li>PLCC</li> </ul>	b)	16 MHZ, normal VDD limits PIC17LC44 – 08/PT Commercial Temp., TQFP package,
	Temperature Range: Frequency Range:	– I 08 16 25 33	= 0°C to +70°C = -40°C to +85°C = 8 MHz = 16 MHz = 25 Mhz = 33 Mhz	c)	8MHz, extended VDD limits PIC17C43 – 25I/P Industrial Temp., PDIP package,
	Device:	PIC17C44 PIC17C44T PIC17LC44	: Standard Vdd range : (Tape and Reel) : Extended Vdd range		25 MHz, normal VDD limits

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Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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