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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	8MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	33
Program Memory Size	4KB (2K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	232 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17lc42at-08-l

FIGURE 6-5: PIC17C42 REGISTER FILE MAP

Addr	Unbanked			
00h	INDF0			
01h	FSR0			
02h	PCL			
03h	PCLATH			
04h	ALUSTA			
05h	T0STA			
06h	CPUSTA			
07h	INTSTA			
08h	INDF1			
09h	FSR1			
0Ah	WREG			
0Bh	TMR0L			
0Ch	TMR0H			
0Dh	TBLPTRL			
0Eh	TBLPTRH			
0Fh	BSR			
	Bank 0	Bank 1 ⁽¹⁾	Bank 2 ⁽¹⁾	Bank 3 ⁽¹⁾
10h	PORTA	DDRC	TMR1	PW1DCL
11h	DDRB	PORTC	TMR2	PW2DCL
12h	PORTB	DDRD	TMR3L	PW1DCH
13h	RCSTA	PORTD	TMR3H	PW2DCH
14h	RCREG	DDRE	PR1	CA2L
15h	TXSTA	PORTE	PR2	CA2H
16h	TXREG	PIR	PR3L/CA1L	TCON1
17h	SPBRG	PIE	PR3H/CA1H	TCON2
18h	General Purpose RAM			
1Fh				
20h				
FFh				

Note 1: SFR file locations 10h - 17h are banked. All other SFRs ignore the Bank Select Register (BSR) bits.

FIGURE 6-6: PIC17CR42/42A/43/R43/44 REGISTER FILE MAP

Addr	Unbanked				
00h	INDF0				
01h	FSR0				
02h	PCL				
03h	PCLATH				
04h	ALUSTA				
05h	T0STA				
06h	CPUSTA				
07h	INTSTA				
08h	INDF1				
09h	FSR1				
0Ah	WREG				
0Bh	TMR0L				
0Ch	TMR0H				
0Dh	TBLPTRL				
0Eh	TBLPTRH				
0Fh	BSR				
	Bank 0	Bank 1 ⁽¹⁾	Bank 2 ⁽¹⁾	Bank 3 ⁽¹⁾	
10h	PORTA	DDRC	TMR1	PW1DCL	
11h	DDRB	PORTC	TMR2	PW2DCL	
12h	PORTB	DDRD	TMR3L	PW1DCH	
13h	RCSTA	PORTD	TMR3H	PW2DCH	
14h	RCREG	DDRE	PR1	CA2L	
15h	TXSTA	PORTE	PR2	CA2H	
16h	TXREG	PIR	PR3L/CA1L	TCON1	
17h	SPBRG	PIE	PR3H/CA1H	TCON2	
18h	PRODL				
19h	PRODH				
1Ah	General Purpose RAM ⁽²⁾				General Purpose RAM ⁽²⁾
1Fh					
20h					
FFh					

Note 1: SFR file locations 10h - 17h are banked. All other SFRs ignore the Bank Select Register (BSR) bits.

2: General Purpose Registers (GPR) locations 20h - FFh and 120h - 1FFh are banked. All other GPRs ignore the Bank Select Register (BSR) bits.

6.2.2.1 ALU STATUS REGISTER (ALUSTA)

The ALUSTA register contains the status bits of the Arithmetic and Logic Unit and the mode control bits for the indirect addressing register.

As with all the other registers, the ALUSTA register can be the destination for any instruction. If the ALUSTA register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Therefore, the result of an instruction with the ALUSTA register as destination may be different than intended.

For example, `CLRF ALUSTA` will clear the upper four bits and set the Z bit. This leaves the ALUSTA register as 0000u1uu (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions be used to alter the ALUSTA register because these instructions do not affect any status bit. To see how other instructions affect the status bits, see the "Instruction Set Summary."

Note 1: The C and DC bits operate as a borrow out bit in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

Note 2: The overflow bit will be set if the 2's complement result exceeds +127 or is less than -128.

Arithmetic and Logic Unit (ALU) is capable of carrying out arithmetic or logical operations on two operands or a single operand. All single operand instructions operate either on the WREG register or a file register. For two operand instructions, one of the operands is the WREG register and the other one is either a file register or an 8-bit immediate constant.

FIGURE 6-7: ALUSTA REGISTER (ADDRESS: 04h, UNBANKED)

R/W - 1	R/W - 1	R/W - 1	R/W - 1	R/W - x	R/W - x	R/W - x	R/W - x
FS3	FS2	FS1	FS0	OV	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
-n = Value at POR reset
(x = unknown)

bit 7-6: **FS3:FS2:** FSR1 Mode Select bits
 00 = Post auto-decrement FSR1 value
 01 = Post auto-increment FSR1 value
 1x = FSR1 value does not change

bit 5-4: **FS1:FS0:** FSR0 Mode Select bits
 00 = Post auto-decrement FSR0 value
 01 = Post auto-increment FSR0 value
 1x = FSR0 value does not change

bit 3: **OV:** Overflow bit
 This bit is used for signed arithmetic (2's complement). It indicates an overflow of the 7-bit magnitude, which causes the sign bit (bit7) to change state.
 1 = Overflow occurred for signed arithmetic, (in this arithmetic operation)
 0 = No overflow occurred

bit 2: **Z:** Zero bit
 1 = The result of an arithmetic or logic operation is zero
 0 = The results of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/borrow bit
 For `ADDWF` and `ADDLW` instructions.
 1 = A carry-out from the 4th low order bit of the result occurred
 0 = No carry-out from the 4th low order bit of the result
 Note: For borrow the polarity is reversed.

bit 0: **C:** carry/borrow bit
 For `ADDWF` and `ADDLW` instructions.
 1 = A carry-out from the most significant bit of the result occurred
 Note that a subtraction is executed by adding the two's complement of the second operand. For rotate (`RRCF`, `RLCF`) instructions, this bit is loaded with either the high or low order bit of the source register.
 0 = No carry-out from the most significant bit of the result
 Note: For borrow the polarity is reversed.

11.3 Read/Write Consideration for TMR0

Although TMR0 is a 16-bit timer/counter, only 8-bits at a time can be read or written during a single instruction cycle. Care must be taken during any read or write.

11.3.1 READING 16-BIT VALUE

The problem in reading the entire 16-bit value is that after reading the low (or high) byte, its value may change from FFh to 00h.

Example 11-1 shows a 16-bit read. To ensure a proper read, interrupts must be disabled during this routine.

EXAMPLE 11-1: 16-BIT READ

```

MOVFP  TMR0L, TMPLO    ;read low tmr0
MOVFP  TMR0H, TMPHI    ;read high tmr0
MOVFP  TMPLO, WREG      ;tmplo -> wreg
CPFSLT TMR0L           ;tmr0l < wreg?
RETURN                ;no then return
MOVFP  TMR0L, TMPLO    ;read low tmr0
MOVFP  TMR0H, TMPHI    ;read high tmr0
RETURN                ;return
    
```

11.3.2 WRITING A 16-BIT VALUE TO TMR0

Since writing to either TMR0L or TMR0H will effectively inhibit increment of that half of the TMR0 in the next cycle (following write), but not inhibit increment of the other half, the user must write to TMR0L first and TMR0H next in two consecutive instructions, as shown in Example 11-2. The interrupt must be disabled. Any write to either TMR0L or TMR0H clears the prescaler.

EXAMPLE 11-2: 16-BIT WRITE

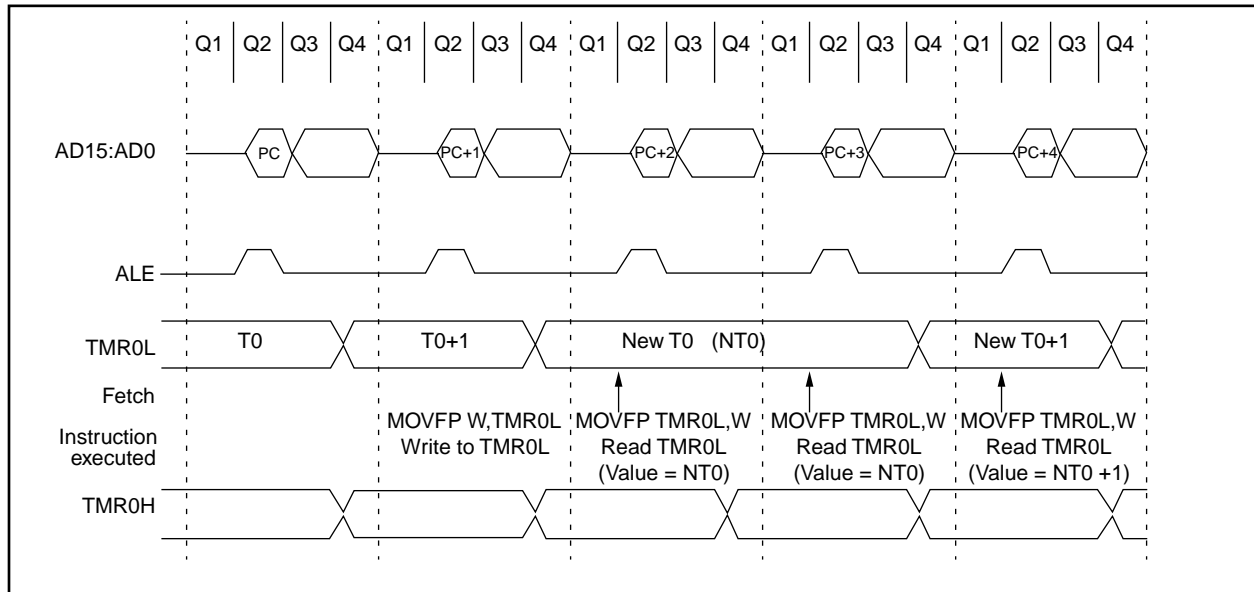
```

BSF    CPUSTA, GLINTD ; Disable interrupt
MOVFP  RAM_L, TMR0L   ;
MOVFP  RAM_H, TMR0H   ;
BCF    CPUSTA, GLINTD ; Done, enable interrupt
    
```

11.4 Prescaler Assignments

Timer0 has an 8-bit prescaler. The prescaler assignment is fully under software control; i.e., it can be changed “on the fly” during program execution. When changing the prescaler assignment, clearing the prescaler is recommended before changing assignment. The value of the prescaler is “unknown,” and assigning a value that is less than the present value makes it difficult to take this unknown time into account.

FIGURE 11-4: TMR0 TIMING: WRITE HIGH OR LOW BYTE



12.1.3 USING PULSE WIDTH MODULATION (PWM) OUTPUTS WITH TMR1 AND TMR2

Two high speed pulse width modulation (PWM) outputs are provided. The PWM1 output uses Timer1 as its time-base, while PWM2 may be software configured to use either Timer1 or Timer2 as the time-base. The PWM outputs are on the RB2/PWM1 and RB3/PWM2 pins.

Each PWM output has a maximum resolution of 10-bits. At 10-bit resolution, the PWM output frequency is 24.4 kHz (@ 25 MHz clock) and at 8-bit resolution the PWM output frequency is 97.7 kHz. The duty cycle of the output can vary from 0% to 100%.

Figure 12-5 shows a simplified block diagram of the PWM module. The duty cycle register is double buffered for glitch free operation. Figure 12-6 shows how a glitch could occur if the duty cycle registers were not double buffered.

The user needs to set the PWM1ON bit (TCON2<4>) to enable the PWM1 output. When the PWM1ON bit is set, the RB2/PWM1 pin is configured as PWM1 output and forced as an output irrespective of the data direction bit (DDRB<2>). When the PWM1ON bit is clear, the pin behaves as a port pin and its direction is controlled by its data direction bit (DDRB<2>). Similarly, the PWM2ON (TCON2<5>) bit controls the configuration of the RB3/PWM2 pin.

FIGURE 12-5: SIMPLIFIED PWM BLOCK DIAGRAM

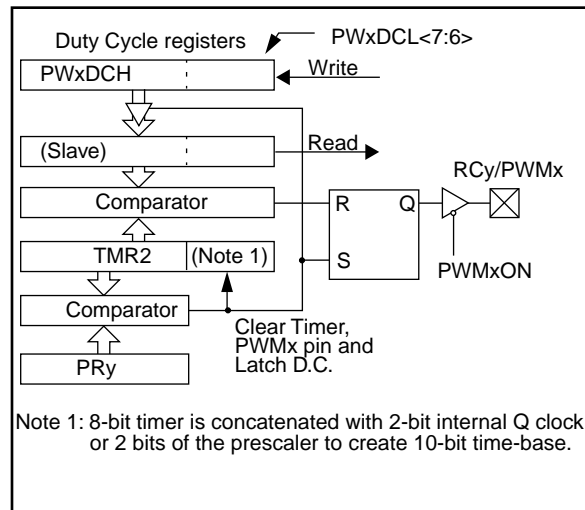
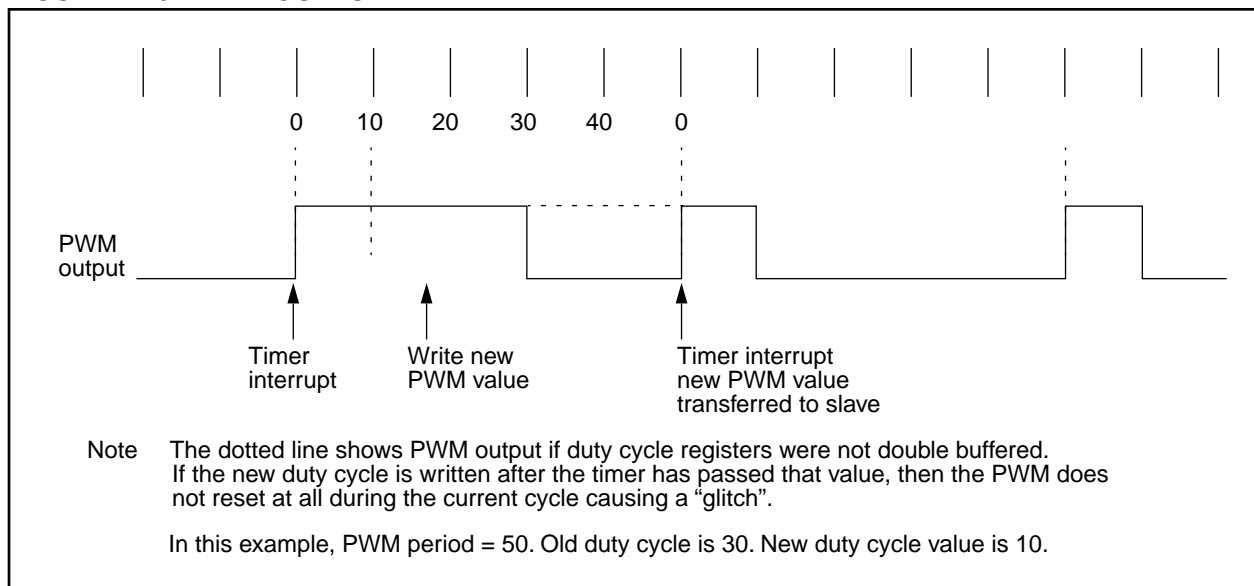


FIGURE 12-6: PWM OUTPUT



12.2.2 DUAL CAPTURE REGISTER MODE

This mode is selected by setting CA1/PR3. A block diagram is shown in Figure 12-8. In this mode, TMR3 runs without a period register and increments from 0000h to FFFFh and rolls over to 0000h. The TMR3 interrupt Flag (TMR3IF) is set on this roll over. The TMR3IF bit must be cleared in software.

Registers PR3H/CA1H and PR3L/CA1L make a 16-bit capture register (Capture1). It captures events on pin RB0/CAP1. Capture mode is configured by the CA1ED1 and CA1ED0 bits. Capture1 Interrupt Flag bit (CA1IF) is set on the capture event. The corresponding interrupt mask bit is CA1IE. The Capture1 Overflow Status bit is CA1OVF.

The Capture2 overflow status flag bit is double buffered. The master bit is set if one captured word is already residing in the Capture2 register and another "event" has occurred on the RB1/CA2 pin. The new event will not transfer the TMR3 value to the capture register which protects the previous unread capture value. When the user reads both the high and the low bytes (in any order) of the Capture2 register, the master overflow bit is transferred to the slave overflow bit (CA2OVF) and then the master bit is reset. The user can then read TCON2 to determine the value of CA2OVF.

The operation of the Capture1 feature is identical to Capture2 (as described in Section 12.2.1).

FIGURE 12-8: TIMER3 WITH TWO CAPTURE REGISTERS BLOCK DIAGRAM

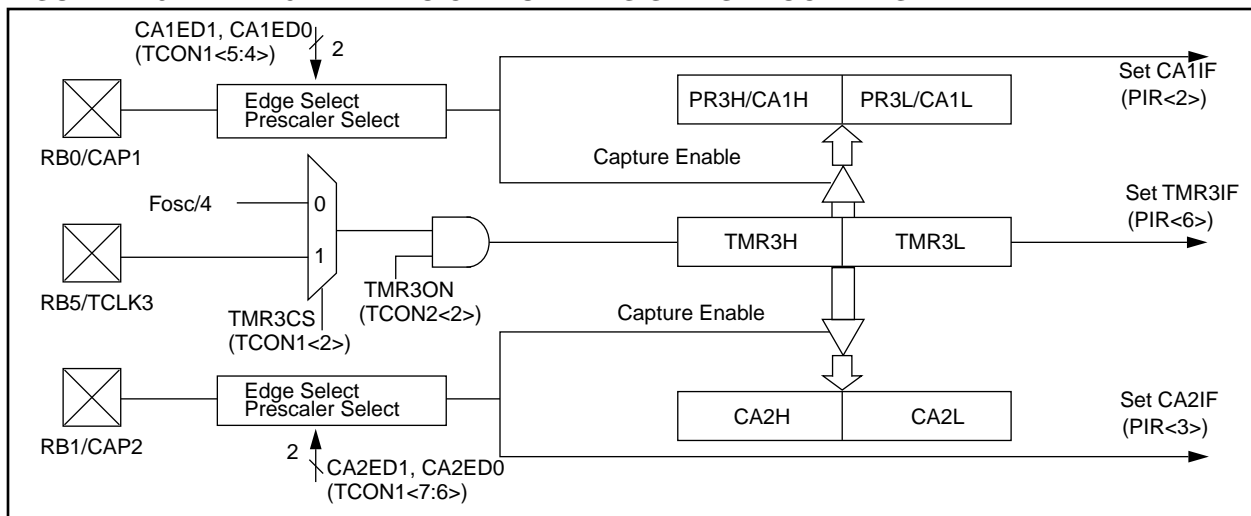


TABLE 12-5: REGISTERS ASSOCIATED WITH CAPTURE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/PR3	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000
12h, Bank 2	TMR3L	TMR3 register; low byte								xxxx xxxx	uuuu uuuu
13h, Bank 2	TMR3H	TMR3 register; high byte								xxxx xxxx	uuuu uuuu
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	T0	PD	—	—	--11 11--	--11 qq--
16h, Bank 2	PR3L/CA1L	Timer3 period register, low byte/capture1 register, low byte								xxxx xxxx	uuuu uuuu
17h, Bank 2	PR3H/CA1H	Timer3 period register, high byte/capture1 register, high byte								xxxx xxxx	uuuu uuuu
14h, Bank 3	CA2L	Capture2 low byte								xxxx xxxx	uuuu uuuu
15h, Bank 3	CA2H	Capture2 high byte								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, — = unimplemented read as '0', q - value depends on condition, shaded cells are not used by Capture.

Note 1: Other (non power-up) resets include: external reset through MCLR and WDT Timer Reset.

FIGURE 13-3: USART TRANSMIT

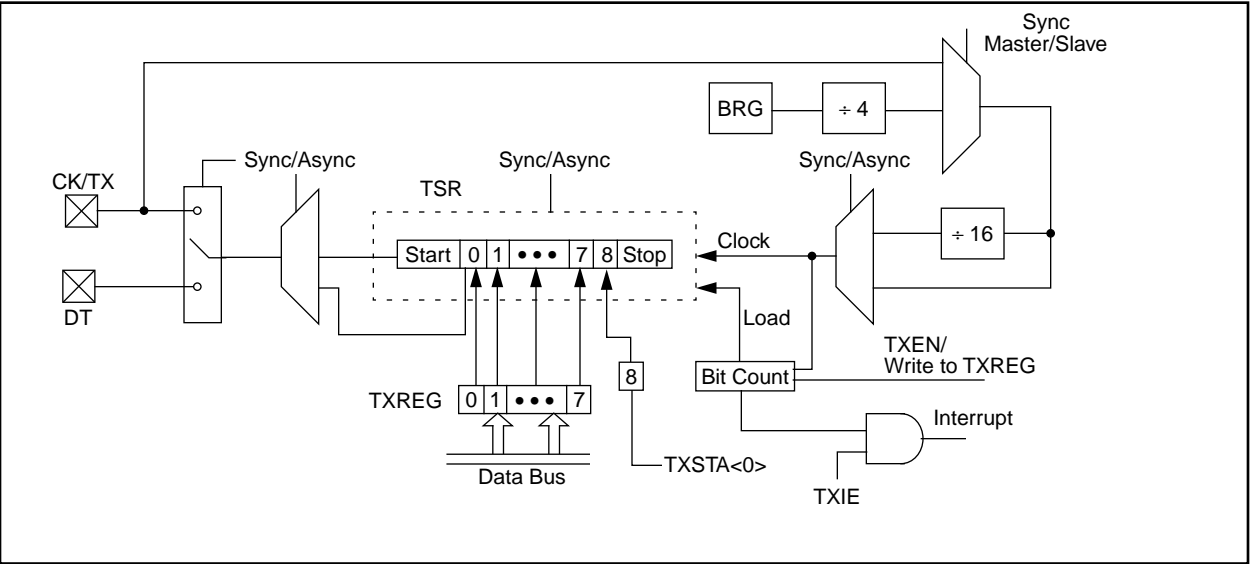
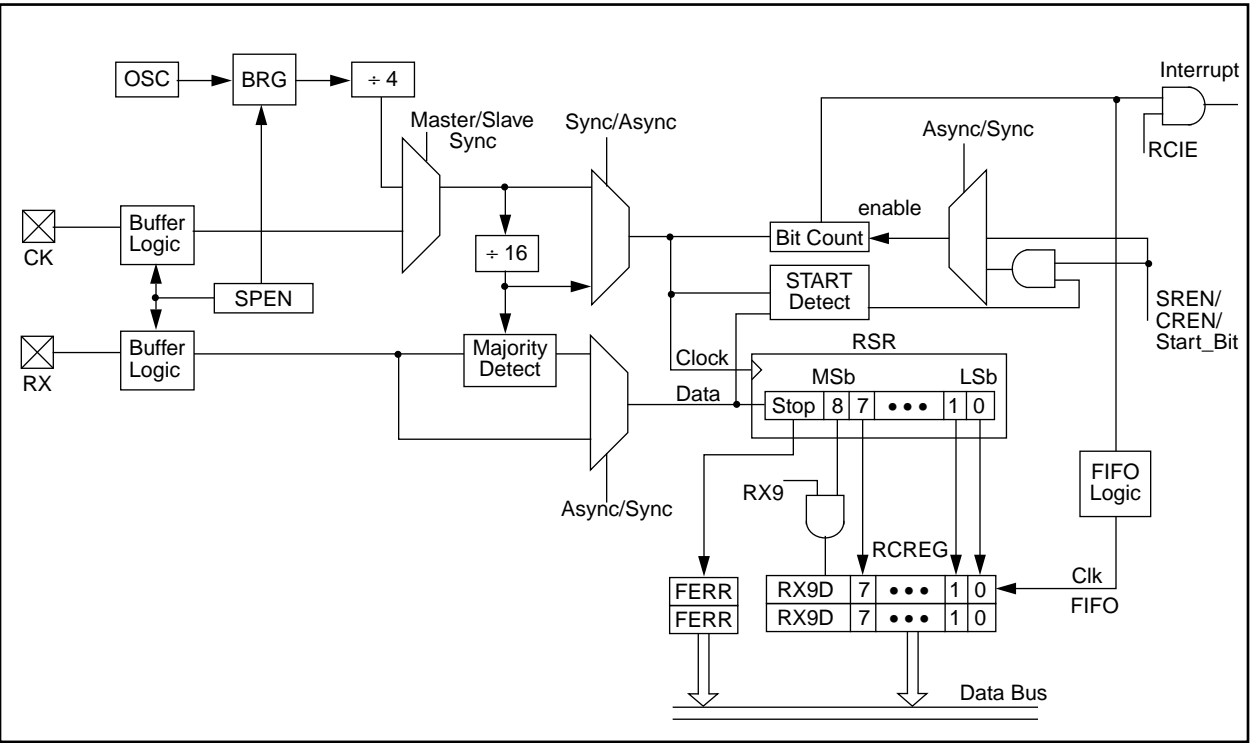


FIGURE 13-4: USART RECEIVE



PIC17C4X

TABLE 15-2: PIC17CXX INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	16-bit Opcode		Status Affected	Notes
			MSb	LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f,d	ADD WREG to f	1	0000 111d ffff ffff	OV,C,DC,Z	
ADDWFC	f,d	ADD WREG and Carry bit to f	1	0001 000d ffff ffff	OV,C,DC,Z	
ANDWF	f,d	AND WREG with f	1	0000 101d ffff ffff	Z	
CLRF	f,s	Clear f, or Clear f and Clear WREG	1	0010 100s ffff ffff	None	3
COMF	f,d	Complement f	1	0001 001d ffff ffff	Z	
CPFSEQ	f	Compare f with WREG, skip if f = WREG	1 (2)	0011 0001 ffff ffff	None	6,8
CPFSGT	f	Compare f with WREG, skip if f > WREG	1 (2)	0011 0010 ffff ffff	None	2,6,8
CPFSLT	f	Compare f with WREG, skip if f < WREG	1 (2)	0011 0000 ffff ffff	None	2,6,8
DAW	f,s	Decimal Adjust WREG Register	1	0010 111s ffff ffff	C	3
DECF	f,d	Decrement f	1	0000 011d ffff ffff	OV,C,DC,Z	
DECFSZ	f,d	Decrement f, skip if 0	1 (2)	0001 011d ffff ffff	None	6,8
DCFSNZ	f,d	Decrement f, skip if not 0	1 (2)	0010 011d ffff ffff	None	6,8
INCF	f,d	Increment f	1	0001 010d ffff ffff	OV,C,DC,Z	
INCFSZ	f,d	Increment f, skip if 0	1 (2)	0001 111d ffff ffff	None	6,8
INFSNZ	f,d	Increment f, skip if not 0	1 (2)	0010 010d ffff ffff	None	6,8
IORWF	f,d	Inclusive OR WREG with f	1	0000 100d ffff ffff	Z	
MOVFP	f,p	Move f to p	1	011p pppp ffff ffff	None	
MOVPF	p,f	Move p to f	1	010p pppp ffff ffff	Z	
MOVWF	f	Move WREG to f	1	0000 0001 ffff ffff	None	
MULWF	f	Multiply WREG with f	1	0011 0100 ffff ffff	None	9
NEGW	f,s	Negate WREG	1	0010 110s ffff ffff	OV,C,DC,Z	1,3
NOP	—	No Operation	1	0000 0000 0000 0000	None	
RLCF	f,d	Rotate left f through Carry	1	0001 101d ffff ffff	C	
RLNCF	f,d	Rotate left f (no carry)	1	0010 001d ffff ffff	None	
RRCF	f,d	Rotate right f through Carry	1	0001 100d ffff ffff	C	
RRNCF	f,d	Rotate right f (no carry)	1	0010 000d ffff ffff	None	
SETF	f,s	Set f	1	0010 101s ffff ffff	None	3
SUBWF	f,d	Subtract WREG from f	1	0000 010d ffff ffff	OV,C,DC,Z	1
SUBWFB	f,d	Subtract WREG from f with Borrow	1	0000 001d ffff ffff	OV,C,DC,Z	1
SWAPF	f,d	Swap f	1	0001 110d ffff ffff	None	
TABLRD	t,i,f	Table Read	2 (3)	1010 10ti ffff ffff	None	7

Legend: Refer to Table 15-1 for opcode field descriptions.

Note 1: 2's Complement method.

2: Unsigned arithmetic.

3: If s = '1', only the file is affected: If s = '0', both the WREG register and the file are affected; If only the Working register (WREG) is required to be affected, then f = WREG must be specified.

4: During an **LCALL**, the contents of PCLATH are loaded into the MSB of the PC and **kkkk** **kkkk** is loaded into the LSB of the PC (PCL)

5: Multiple cycle instruction for EPROM programming when table pointer selects internal EPROM. The instruction is terminated by an interrupt event. When writing to external program memory, it is a two-cycle instruction.

6: Two-cycle instruction when condition is true, else single cycle instruction.

7: Two-cycle instruction except for **TABLRD** to PCL (program counter low byte) in which case it takes 3 cycles.

8: A "skip" means that instruction fetched during execution of current instruction is not executed, instead an NOP is executed.

9: These instructions are not available on the PIC17C42.

ADDWFC		ADD WREG and Carry bit to f						
Syntax:	[<i>label</i>] ADDWFC f,d							
Operands:	0 ≤ f ≤ 255 d ∈ [0,1]							
Operation:	(WREG) + (f) + C → (dest)							
Status Affected:	OV, C, DC, Z							
Encoding:	<table border="1"><tr><td>0001</td><td>000d</td><td>ffff</td><td>ffff</td></tr></table>				0001	000d	ffff	ffff
0001	000d	ffff	ffff					
Description:	Add WREG, the Carry Flag and data memory location 'f'. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed in data memory location 'f'.							
Words:	1							
Cycles:	1							
Q Cycle Activity:								
	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Execute	Write to destination				

Example: ADDWFC REG 0

Before Instruction

Carry bit = 1
REG = 0x02
WREG = 0x4D

After Instruction

Carry bit = 0
REG = 0x02
WREG = 0x50

ANDLW		And Literal with WREG						
Syntax:	[<i>label</i>] ANDLW k							
Operands:	0 ≤ k ≤ 255							
Operation:	(WREG) .AND. (k) → (WREG)							
Status Affected:	Z							
Encoding:	<table border="1"><tr><td>1011</td><td>0101</td><td>kkkk</td><td>kkkk</td></tr></table>				1011	0101	kkkk	kkkk
1011	0101	kkkk	kkkk					
Description:	The contents of WREG are AND'd with the 8-bit literal 'k'. The result is placed in WREG.							
Words:	1							
Cycles:	1							
Q Cycle Activity:								
	Q1	Q2	Q3	Q4				
	Decode	Read literal 'k'	Execute	Write to WREG				

Example: ANDLW 0x5F

Before Instruction

WREG = 0xA3

After Instruction

WREG = 0x03

TABLWT Table Write

Example1: TABLWT 0, 1, REG

Before Instruction

REG = 0x53
TBLATH = 0xAA
TBLATL = 0x55
TBLPTR = 0xA356
MEMORY(TBLPTR) = 0xFFFF

After Instruction (table write completion)

REG = 0x53
TBLATH = 0x53
TBLATL = 0x55
TBLPTR = 0xA357
MEMORY(TBLPTR - 1) = 0x5355

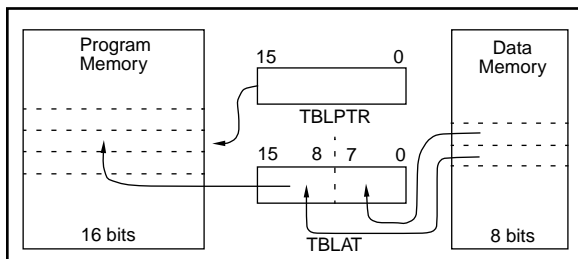
Example 2: TABLWT 1, 0, REG

Before Instruction

REG = 0x53
TBLATH = 0xAA
TBLATL = 0x55
TBLPTR = 0xA356
MEMORY(TBLPTR) = 0xFFFF

After Instruction (table write completion)

REG = 0x53
TBLATH = 0xAA
TBLATL = 0x53
TBLPTR = 0xA356
MEMORY(TBLPTR) = 0xAA53



TLRD Table Latch Read

Syntax: [label] TLRD t,f

Operands: $0 \leq f \leq 255$
 $t \in [0,1]$

Operation: If $t = 0$,
TBLATL \rightarrow f;
If $t = 1$,
TBLATH \rightarrow f

Status Affected: None

Encoding:

1010	00tx	ffff	ffff
------	------	------	------

Description: Read data from 16-bit table latch (TBLAT) into file register 'f'. Table Latch is unaffected.

If $t = 1$; high byte is read

If $t = 0$; low byte is read

This instruction is used in conjunction with TABLWD to transfer data from program memory to data memory.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register TBLATH or TBLATL	Execute	Write register 'f'

Example: TLRD t, RAM

Before Instruction

t = 0
RAM = ?
TBLAT = 0x00AF (TBLATH = 0x00)
(TBLATL = 0xAF)

After Instruction

RAM = 0xAF
TBLAT = 0x00AF (TBLATH = 0x00)
(TBLATL = 0xAF)

Before Instruction

t = 1
RAM = ?
TBLAT = 0x00AF (TBLATH = 0x00)
(TBLATL = 0xAF)

After Instruction

RAM = 0x00
TBLAT = 0x00AF (TBLATH = 0x00)
(TBLATL = 0xAF)

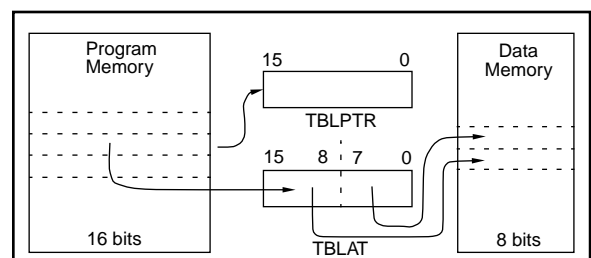


FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

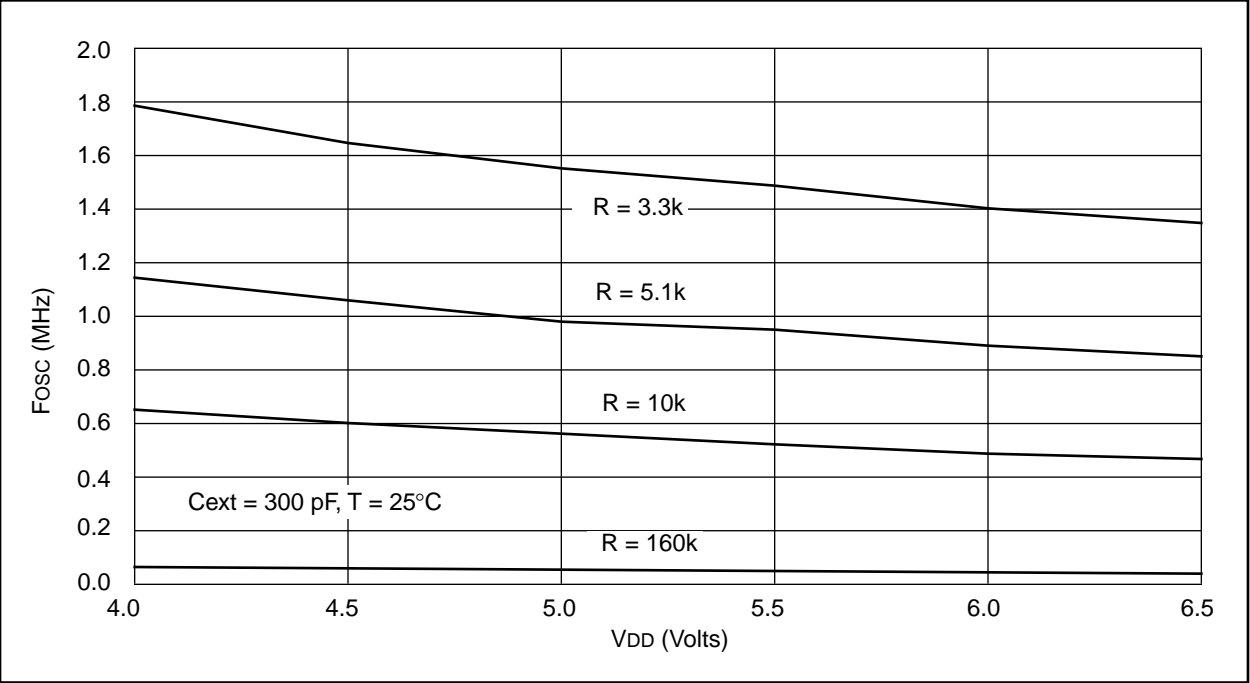


TABLE 18-2: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
22 pF	10k	3.33 MHz	± 12%
	100k	353 kHz	± 13%
100 pF	3.3k	3.54 MHz	± 10%
	5.1k	2.43 MHz	± 14%
	10k	1.30 MHz	± 17%
	100k	129 kHz	± 10%
300 pF	3.3k	1.54 MHz	± 14%
	5.1k	980 kHz	± 12%
	10k	564 kHz	± 16%
	160k	35 kHz	± 18%

FIGURE 18-7: TYPICAL I_{DD} vs. FREQUENCY (EXTERNAL CLOCK 25°C)

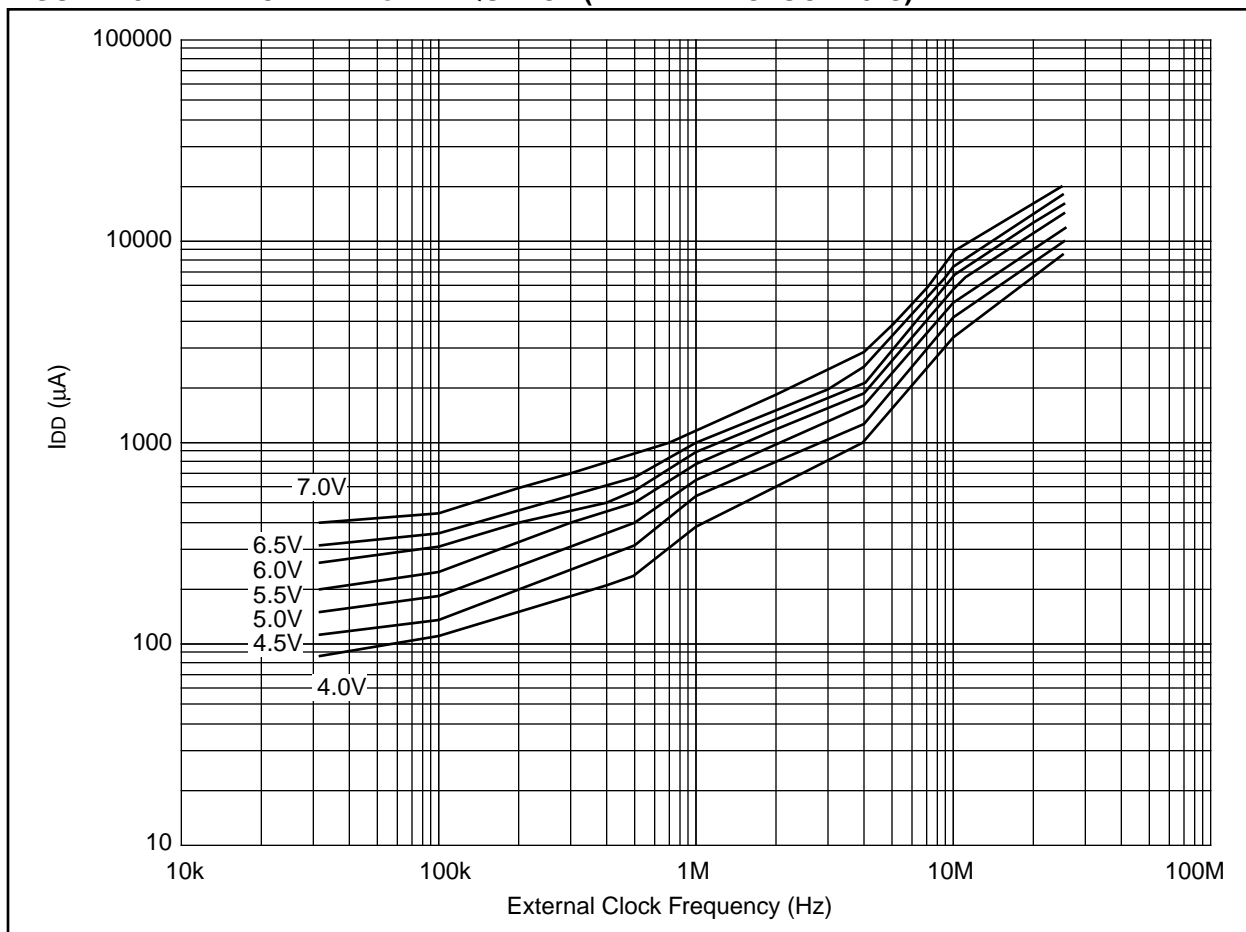
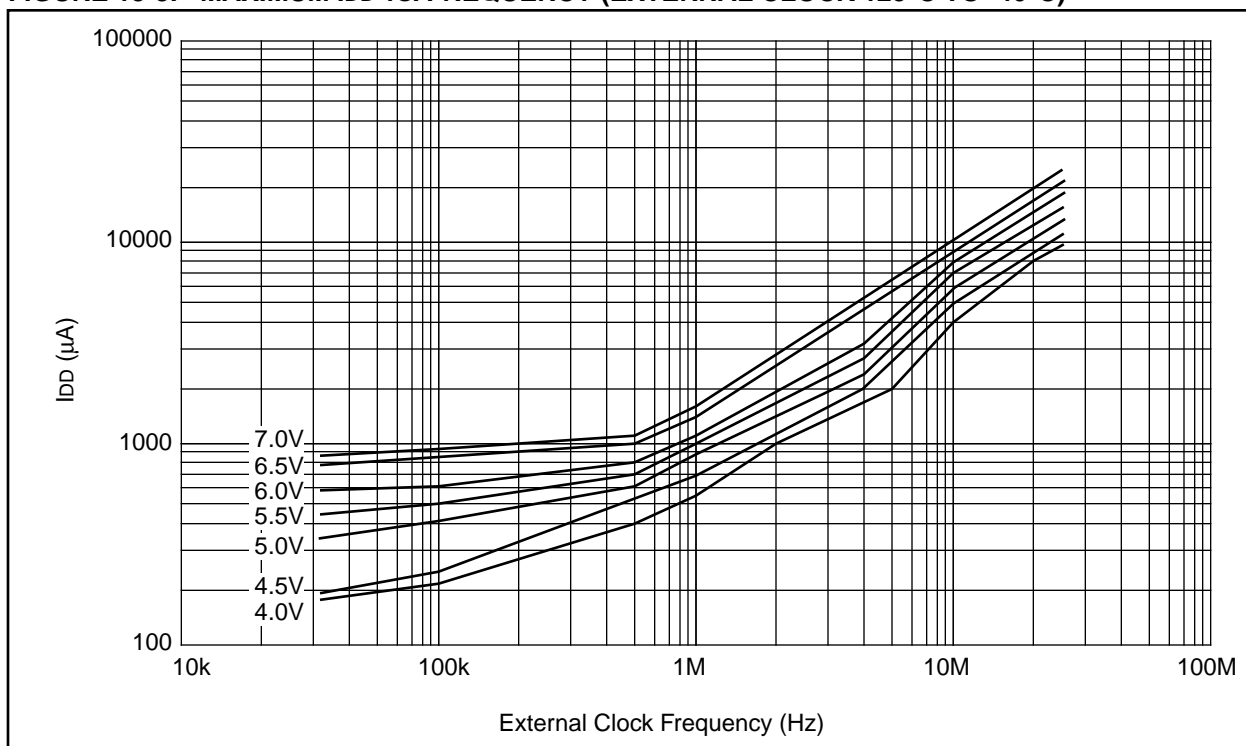


FIGURE 18-8: MAXIMUM I_{DD} vs. FREQUENCY (EXTERNAL CLOCK 125°C TO -40°C)



20.0 PIC17CR42/42A/43/R43/44 DC AND AC CHARACTERISTICS

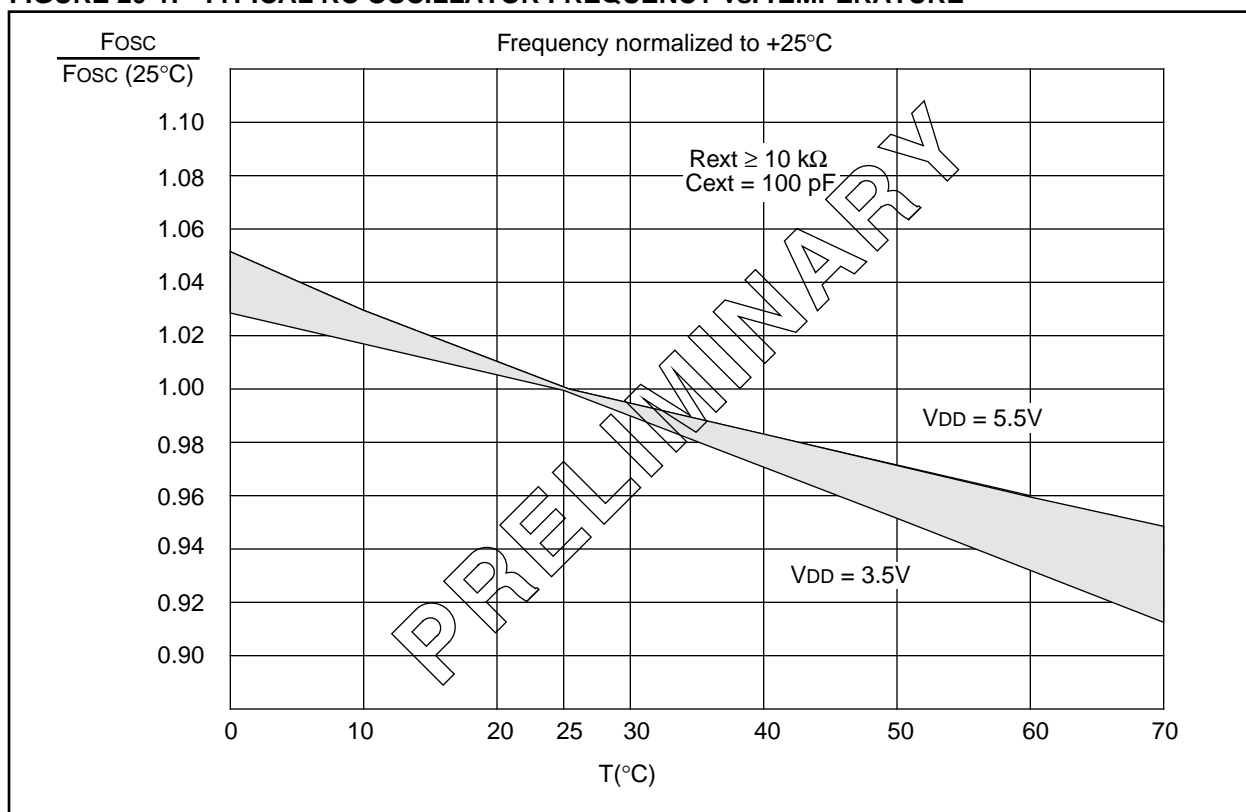
The graphs and tables provided in this section are for design guidance and are not tested nor guaranteed. In some graphs or tables the data presented is outside specified operating range (e.g. outside specified V_{DD} range). This is for information only and devices are ensured to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents $(\text{mean} + 3\sigma)$ and $(\text{mean} - 3\sigma)$ respectively where σ is standard deviation.

TABLE 20-1: PIN CAPACITANCE PER PACKAGE TYPE

Pin Name	Typical Capacitance (pF)			
	40-pin DIP	44-pin PLCC	44-pin MQFP	44-pin TQFP
All pins, except $\overline{\text{MCLR}}$, V_{DD} , and V_{SS}	10	10	10	10
$\overline{\text{MCLR}}$ pin	20	20	20	20

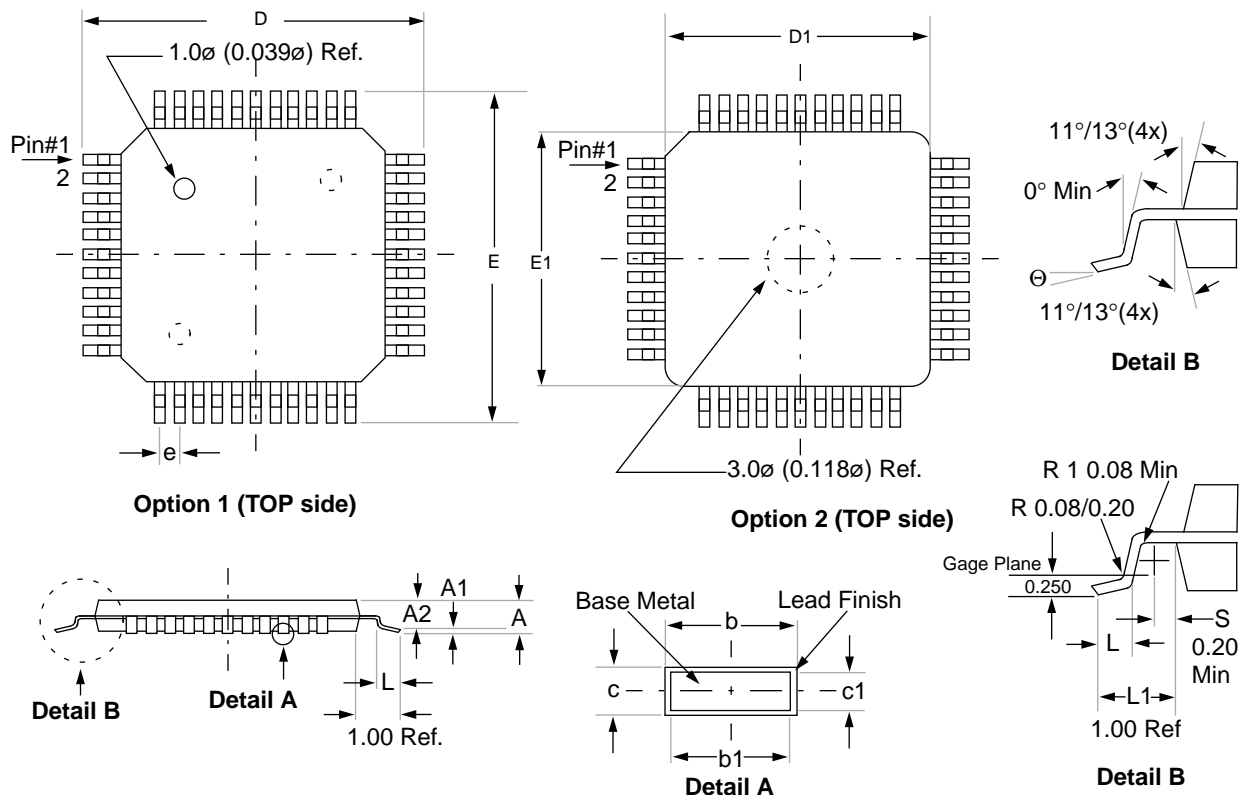
FIGURE 20-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE



PIC17C4X

NOTES:

21.5 44-Lead Plastic Surface Mount (TQFP 10x10 mm Body 1.0/0.10 mm Lead Form)



Package Group: Plastic TQFP						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.00	1.20		0.039	0.047	
A1	0.05	0.15		0.002	0.006	
A2	0.95	1.05		0.037	0.041	
D	11.75	12.25		0.463	0.482	
D1	9.90	10.10		0.390	0.398	
E	11.75	12.25		0.463	0.482	
E1	9.90	10.10		0.390	0.398	
L	0.45	0.75		0.018	0.030	
e	0.80 BSC			0.031 BSC		
b	0.30	0.45		0.012	0.018	
b1	0.30	0.40		0.012	0.016	
c	0.09	0.20		0.004	0.008	
c1	0.09	0.16		0.004	0.006	
N	44	44		44	44	
Θ	0°	7°		0°	7°	

Note 1: Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25mm (0.010") per side. D1 and E1 dimensions including mold mismatch.

2: Dimension "b" does not include Dambar protrusion, allowable Dambar protrusion shall be 0.08mm (0.003") max.

3: This outline conforms to JEDEC MS-026.

APPENDIX A: MODIFICATIONS

The following is the list of modifications over the PIC16CXX microcontroller family:

1. Instruction word length is increased to 16-bit. This allows larger page sizes both in program memory (8 Kwords versus 2 Kwords) and register file (256 bytes versus 128 bytes).
2. Four modes of operation: microcontroller, protected microcontroller, extended microcontroller, and microprocessor.
3. 22 new instructions. The `MOVF`, `TRIS` and `OPTION` instructions have been removed.
4. 4 new instructions for transferring data between data memory and program memory. This can be used to "self program" the EPROM program memory.
5. Single cycle data memory to data memory transfers possible (`MOVFP` and `MOVFP` instructions). These instructions do not affect the Working register (WREG).
6. W register (WREG) is now directly addressable.
7. A PC high latch register (PCLATH) is extended to 8-bits. The PCLATCH register is now both readable and writable.
8. Data memory paging is redefined slightly.
9. DDR registers replaces function of TRIS registers.
10. Multiple Interrupt vectors added. This can decrease the latency for servicing the interrupt.
11. Stack size is increased to 16 deep.
12. BSR register for data memory paging.
13. Wake up from SLEEP operates slightly differently.
14. The Oscillator Start-Up Timer (OST) and Power-Up Timer (PWRT) operate in parallel and not in series.
15. PORTB interrupt on change feature works on all eight port pins.
16. TMR0 is 16-bit plus 8-bit prescaler.
17. Second indirect addressing register added (FSR1 and FSR2). Configuration bits can select the FSR registers to auto-increment, auto-decrement, remain unchanged after an indirect address.
18. Hardware multiplier added (8 x 8 → 16-bit) (PIC17C43 and PIC17C44 only).
19. Peripheral modules operate slightly differently.
20. Oscillator modes slightly redefined.
21. Control/Status bits and registers have been placed in different registers and the control bit for globally enabling interrupts has inverse polarity.
22. Addition of a test mode pin.
23. In-circuit serial programming is not implemented.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16CXX to PIC17CXX, the user should take the following steps:

1. Remove any `TRIS` and `OPTION` instructions, and implement the equivalent code.
2. Separate the interrupt service routine into its four vectors.
3. Replace:

```
MOVF    REG1, W
```

 with:

```
MOVFP   REG1, WREG
```
4. Replace:

```
MOVF    REG1, W
```

```
MOVWF   REG2
```

 with:

```
MOVFP   REG1, REG2 ; Addr(REG1)<20h
```

 or

```
MOVFP   REG1, REG2 ; Addr(REG2)<20h
```

Note: If REG1 and REG2 are both at addresses greater than 20h, two instructions are required.

```
MOVFP   REG1, WREG ;
MOVFP   WREG, REG2 ;
```

5. Ensure that all bit names and register names are updated to new data memory map location.
6. Verify data memory banking.
7. Verify mode of operation for indirect addressing.
8. Verify peripheral routines for compatibility.
9. Weak pull-ups are enabled on reset.

To convert code from the PIC17C42 to all the other PIC17C4X devices, the user should take the following steps.

1. If the hardware multiply is to be used, ensure that any variables at address 18h and 19h are moved to another address.
2. Ensure that the upper nibble of the BSR was not written with a non-zero value. This may cause unexpected operation since the RAM bank is no longer 0.
3. The disabling of global interrupts has been enhanced so there is no additional testing of the GLINTD bit after a `BSF CPUSTA, GLINTD` instruction.

INDEX

A

ADDLW	112
ADDWF	112
ADDWFC	113
ALU	9
ALU STATUS Register (ALUSTA)	36
ALUSTA	34, 36, 108
ALUSTA Register	36
ANDLW	113
ANDWF	114
Application Notes	
AN552	55
Assembler	144
Asynchronous Master Transmission	90
Asynchronous Transmitter	89

B

Bank Select Register (BSR)	42
Banking	42
Baud Rate Formula	86
Baud Rate Generator (BRG)	86
Baud Rates	
Asynchronous Mode	88
Synchronous Mode	87
BCF	114
Bit Manipulation	108
Block Diagrams	
On-chip Reset Circuit	15
PIC17C42	10
PORTD	60
PORTE	62
PWM	75
RA0 and RA1	53
RA2 and RA3	54
RA4 and RA5	54
RB3:RB2 Port Pins	56
RB7:RB4 and RB1:RB0 Port Pins	55
RC7:RC0 Port Pins	58
Timer3 with One Capture and One Period Register ..	78
TMR1 and TMR2 in 16-bit Timer/Counter Mode	74
TMR1 and TMR2 in Two 8-bit Timer/Counter Mode ..	73
TMR3 with Two Capture Registers	79
WDT	104
BORROW	9
BRG	86
Brown-out Protection	18
BSF	115
BSR	34, 42
BSR Operation	42
BTFSC	115
BTFSS	116
BTG	116

C

C	9, 36
C Compiler (MP-C)	145
CA1/PR3	72
CA1ED0	71
CA1ED1	71

CA1IE	23
CA1IF	24
CA1OVF	72
CA2ED0	71
CA2ED1	71
CA2H	20, 35
CA2IE	23, 78
CA2IF	24, 78
CA2L	20, 35
CA2OVF	72
Calculating Baud Rate Error	86
CALL	39, 117
Capacitor Selection	
Ceramic Resonators	101
Crystal Oscillator	101
Capture	71, 78
Capture Sequence to Read Example	78
Capture1	
Mode	71
Overflow	72
Capture2	
Mode	71
Overflow	72
Carry (C)	9
Ceramic Resonators	100
Circular Buffer	39
Clearing the Prescaler	103
Clock/Instruction Cycle (Figure)	14
Clocking Scheme/Instruction Cycle (Section)	14
CLRF	117
CLRWDT	118
Code Protection	99, 106
COMF	118
Configuration	
Bits	100
Locations	100
Oscillator	100
Word	99
CPFSEQ	119
CPFSGT	119
CPFSLT	120
CPU STATUS Register (CPUTA)	37
CPUTA	34, 37, 105
CREN	84
Crystal Operation, Overtone Crystals	101
Crystal or Ceramic Resonator Operation	100
Crystal Oscillator	100
CSRC	83

D

Data Memory	
GPR	29, 32
Indirect Addressing	39
Organization	32
SFR	29, 32
Transfer to Program Memory	43
DAW	120
DC	9, 36
DDRB	19, 34, 55
DDRC	19, 34, 58
DDRD	19, 34, 60
DDRE	19, 34, 62
DECF	121
DECFSNZ	122
DECFSZ	121

PIC17C4X

Figure 6-12:	Program Counter using The CALL and GOTO Instructions.....	41
Figure 6-13:	BSR Operation (PIC17C43/R43/44).....	42
Figure 7-1:	TLWT Instruction Operation.....	43
Figure 7-2:	TABLWT Instruction Operation.....	43
Figure 7-3:	TLRD Instruction Operation.....	44
Figure 7-4:	TABLRD Instruction Operation.....	44
Figure 7-5:	TABLWT Write Timing (External Memory).....	46
Figure 7-6:	Consecutive TABLWT Write Timing (External Memory).....	47
Figure 7-7:	TABLRD Timing.....	48
Figure 7-8:	TABLRD Timing (Consecutive TABLRD Instructions).....	48
Figure 9-1:	RA0 and RA1 Block Diagram.....	53
Figure 9-2:	RA2 and RA3 Block Diagram.....	54
Figure 9-3:	RA4 and RA5 Block Diagram.....	54
Figure 9-4:	Block Diagram of RB<7:4> and RB<1:0> Port Pins.....	55
Figure 9-5:	Block Diagram of RB3 and RB2 Port Pins..	56
Figure 9-6:	Block Diagram of RC<7:0> Port Pins.....	58
Figure 9-7:	PORTD Block Diagram (in I/O Port Mode).....	60
Figure 9-8:	PORTE Block Diagram (in I/O Port Mode).....	62
Figure 9-9:	Successive I/O Operation.....	64
Figure 11-1:	T0STA Register (Address: 05h, Unbanked).....	67
Figure 11-2:	Timer0 Module Block Diagram.....	68
Figure 11-3:	TMR0 Timing with External Clock (Increment on Falling Edge).....	68
Figure 11-4:	TMR0 Timing: Write High or Low Byte.....	69
Figure 11-5:	TMR0 Read/Write in Timer Mode.....	70
Figure 12-1:	TCON1 Register (Address: 16h, Bank 3) ...	71
Figure 12-2:	TCON2 Register (Address: 17h, Bank 3) ...	72
Figure 12-3:	Timer1 and Timer2 in Two 8-bit Timer/Counter Mode.....	73
Figure 12-4:	TMR1 and TMR2 in 16-bit Timer/Counter Mode.....	74
Figure 12-5:	Simplified PWM Block Diagram.....	75
Figure 12-6:	PWM Output.....	75
Figure 12-7:	Timer3 with One Capture and One Period Register Block Diagram.....	78
Figure 12-8:	Timer3 with Two Capture Registers Block Diagram.....	79
Figure 12-9:	TMR1, TMR2, and TMR3 Operation in External Clock Mode.....	80
Figure 12-10:	TMR1, TMR2, and TMR3 Operation in Timer Mode.....	81
Figure 13-1:	TXSTA Register (Address: 15h, Bank 0)	83
Figure 13-2:	RCSTA Register (Address: 13h, Bank 0) ...	84
Figure 13-3:	USART Transmit.....	85
Figure 13-4:	USART Receive.....	85
Figure 13-5:	Asynchronous Master Transmission.....	90
Figure 13-6:	Asynchronous Master Transmission (Back to Back).....	90
Figure 13-7:	RX Pin Sampling Scheme.....	91
Figure 13-8:	Asynchronous Reception.....	92
Figure 13-9:	Synchronous Transmission.....	94
Figure 13-10:	Synchronous Transmission (Through TXEN).....	94
Figure 13-11:	Synchronous Reception (Master Mode, SREN).....	95
Figure 14-1:	Configuration Word.....	99
Figure 14-2:	Crystal or Ceramic Resonator Operation (XT or LF OSC Configuration).....	100
Figure 14-3:	Crystal Operation, Overtone Crystals (XT OSC Configuration).....	101
Figure 14-4:	External Clock Input Operation (EC OSC Configuration).....	101
Figure 14-5:	External Parallel Resonant Crystal Oscillator Circuit.....	102
Figure 14-6:	External Series Resonant Crystal Oscillator Circuit.....	102
Figure 14-7:	RC Oscillator Mode.....	102
Figure 14-8:	Watchdog Timer Block Diagram.....	104
Figure 14-9:	Wake-up From Sleep Through Interrupt... ..	105
Figure 15-1:	General Format for Instructions.....	108
Figure 15-2:	Q Cycle Activity.....	109
Figure 17-1:	Parameter Measurement Information.....	154
Figure 17-2:	External Clock Timing.....	155
Figure 17-3:	CLKOUT and I/O Timing.....	156
Figure 17-4:	Reset, Watchdog Timer, Oscillator Start-Up Timer and Power-Up Timer Timing.....	157
Figure 17-5:	Timer0 Clock Timings.....	158
Figure 17-6:	Timer1, Timer2, And Timer3 Clock Timings.....	158
Figure 17-7:	Capture Timings.....	159
Figure 17-8:	PWM Timings.....	159
Figure 17-9:	USART Module: Synchronous Transmission (Master/Slave) Timing.....	160
Figure 17-10:	USART Module: Synchronous Receive (Master/Slave) Timing.....	160
Figure 17-11:	Memory Interface Write Timing.....	161
Figure 17-12:	Memory Interface Read Timing.....	162
Figure 18-1:	Typical RC Oscillator Frequency vs. Temperature.....	163
Figure 18-2:	Typical RC Oscillator Frequency vs. VDD.....	164
Figure 18-3:	Typical RC Oscillator Frequency vs. VDD.....	164
Figure 18-4:	Typical RC Oscillator Frequency vs. VDD.....	165
Figure 18-5:	Transconductance (gm) of LF Oscillator vs. VDD.....	166
Figure 18-6:	Transconductance (gm) of XT Oscillator vs. VDD.....	166
Figure 18-7:	Typical IDD vs. Frequency (External Clock 25°C).....	167
Figure 18-8:	Maximum IDD vs. Frequency (External Clock 125°C to -40°C).....	167
Figure 18-9:	Typical IPD vs. VDD Watchdog Disabled 25°C.....	168
Figure 18-10:	Maximum IPD vs. VDD Watchdog Disabled.....	168
Figure 18-11:	Typical IPD vs. VDD Watchdog Enabled 25°C.....	169
Figure 18-12:	Maximum IPD vs. VDD Watchdog Enabled.....	169
Figure 18-13:	WDT Timer Time-Out Period vs. VDD.....	170
Figure 18-14:	IOH vs. VOH, VDD = 3V.....	170
Figure 18-15:	IOH vs. VOH, VDD = 5V.....	171
Figure 18-16:	IOL vs. VOL, VDD = 3V.....	171
Figure 18-17:	IOL vs. VOL, VDD = 5V.....	172
Figure 18-18:	VTH (Input Threshold Voltage) of I/O Pins (TTL) vs. VDD.....	172
Figure 18-19:	VTH, VIL of I/O Pins (Schmitt Trigger) vs. VDD.....	173
Figure 18-20:	VTH (Input Threshold Voltage) of OSC1 Input (In XT and LF Modes) vs. VDD.....	173
Figure 19-1:	Parameter Measurement Information.....	183

PIC17C4X

Table 17-9:	Serial Port Synchronous Transmission Requirements	160
Table 17-10:	Serial Port Synchronous Receive Requirements	160
Table 17-11:	Memory Interface Write Requirements	161
Table 17-12:	Memory Interface Read Requirements	162
Table 18-1:	Pin Capacitance per Package Type	163
Table 18-2:	RC Oscillator Frequencies	165
Table 19-1:	Cross Reference of Device Specs for Oscillator Configurations and Frequencies of Operation (Commercial Devices)	176
Table 19-2:	External Clock Timing Requirements	184
Table 19-3:	CLKOUT and I/O Timing Requirements ...	185
Table 19-4:	Reset, Watchdog Timer, Oscillator Start-Up Timer and Power-Up Timer Requirements	186
Table 19-5:	Timer0 Clock Requirements	187
Table 19-6:	Timer1, Timer2, and Timer3 Clock Requirements	187
Table 19-7:	Capture Requirements	188
Table 19-8:	PWM Requirements	188
Table 19-9:	Synchronous Transmission Requirements	189
Table 19-10:	Synchronous Receive Requirements	189
Table 19-11:	Memory Interface Write Requirements (Not Supported in PIC17LC4X Devices) ...	190
Table 19-12:	Memory Interface read Requirements (Not Supported in PIC17LC4X Devices) ...	191
Table 20-1:	Pin Capacitance per Package Type	193
Table 20-2:	RC Oscillator Frequencies	195
Table E-1:	Pin Compatible Devices	221

LIST OF EQUATIONS

Equation 8-1:	16 x 16 Unsigned Multiplication Algorithm	50
Equation 8-2:	16 x 16 Signed Multiplication Algorithm	51

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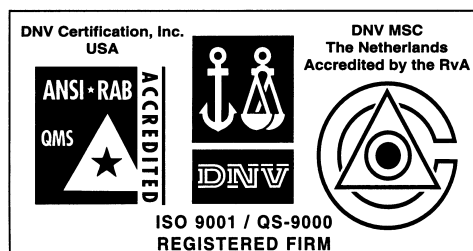
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