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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	8MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	33
Program Memory Size	16KB (8K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	454 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17lc44-08i-pt

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC17C4X can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC17C4X uses a modified Harvard architecture. This architecture has the program and data accessed from separate memories. So the device has a program memory bus and a data memory bus. This improves bandwidth over traditional von Neumann architecture, where program and data are fetched from the same memory (accesses over the same bus). Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. PIC17C4X opcodes are 16-bits wide, enabling single word instructions. The full 16-bit wide program memory bus fetches a 16-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions. Consequently, all instructions execute in a single cycle (121 ns @ 33 MHz), except for program branches and two special instructions that transfer data between program and data memory.

The PIC17C4X can address up to 64K x 16 of program memory space.

The **PIC17C42** and **PIC17C42A** integrate 2K x 16 of EPROM program memory on-chip, while the **PIC17CR42** has 2K x 16 of ROM program memory on-chip.

The **PIC17C43** integrates 4K x 16 of EPROM program memory, while the **PIC17CR43** has 4K x 16 of ROM program memory.

The **PIC17C44** integrates 8K x 16 EPROM program memory.

Program execution can be internal only (microcontroller or protected microcontroller mode), external only (microprocessor mode) or both (extended microcontroller mode). Extended microcontroller mode does not allow code protection.

The PIC17CXX can directly or indirectly address its register files or data memory. All special function registers, including the Program Counter (PC) and Working Register (WREG), are mapped in the data memory. The PIC17CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC17CXX simple yet efficient. In addition, the learning curve is reduced significantly.

One of the PIC17CXX family architectural enhancements from the PIC16CXX family allows two file registers to be used in some two operand instructions. This allows data to be moved directly between two registers without going through the WREG register. This increases performance and decreases program memory usage. The PIC17CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift, and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature.

The WREG register is an 8-bit working register used for ALU operations.

All PIC17C4X devices (except the PIC17C42) have an 8 x 8 hardware multiplier. This multiplier generates a 16-bit result in a single cycle.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

Although the ALU does not perform signed arithmetic, the Overflow bit (OV) can be used to implement signed math. Signed arithmetic is comprised of a magnitude and a sign bit. The overflow bit indicates if the magnitude overflows and causes the sign bit to change state. Signed math can have greater than 7-bit values (magnitude), if more than one byte is used. The use of the overflow bit only operates on bit6 (MSb of magnitude) and bit7 (sign bit) of the value in the ALU. That is, the overflow bit is not useful if trying to implement signed math where the magnitude, for example, is 11-bits. If the signed math values are greater than 7-bits (15-, 24or 31-bit), the algorithm must ensure that the low order bytes ignore the overflow status bit.

Care should be taken when adding and subtracting signed numbers to ensure that the correct operation is executed. Example 3-1 shows an item that must be taken into account when doing signed arithmetic on an ALU which operates as an unsigned machine.

EXAMPLE 3-1: SIGNED MATH

Hex Value	Signed Value Math	Unsigned Value Math
FFh	-127	255
<u>+ 01h</u>	<u>+ 1</u>	<u>+ 1</u>
= ?	= -126 (FEh)	= 0 (00h); Carry bit = 1
		curry pro - r

Signed math requires the result in REG to be FEh (-126). This would be accomplished by subtracting one as opposed to adding one.

Simplified block diagrams are shown in Figure 3-1 and Figure 3-2. The descriptions of the device pins are listed in Table 3-1.

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4.0 RESET

The PIC17CXX differentiates between various kinds of reset:

- Power-on Reset (POR)
- MCLR reset during normal operation
- WDT Reset (normal operation)

Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are forced to a "reset state" on Power-on Reset (POR), on $\overline{\text{MCLR}}$ or WDT Reset and on $\overline{\text{MCLR}}$ reset during SLEEP. They are not affected by a WDT Reset during SLEEP, since this reset is viewed as the resumption of normal operation. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different reset situations as indicated in Table 4-3. These bits are used in software to determine the nature of reset. See Table 4-4 for a full description of reset states of all registers.

Note: While the device is in a reset state, the internal phase clock is held in the Q1 state. Any processor mode that allows external execution will force the RE0/ALE pin as a low output and the RE1/OE and RE2/WR pins as high outputs.

A simplified block diagram of the on-chip reset circuit is shown in Figure 4-1.

4.1 <u>Power-on Reset (POR), Power-up</u> <u>Timer (PWRT), and Oscillator Start-up</u> <u>Timer (OST)</u>

4.1.1 POWER-ON RESET (POR)

The Power-on Reset circuit holds the device in reset until VDD is above the trip point (in the range of 1.4V -2.3V). The PIC17C42 does not produce an internal reset when VDD declines. All other devices will produce an internal reset for both rising and falling VDD. To take advantage of the POR, just tie the MCLR/VPP pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for VDD is required. See Electrical Specifications for details.

4.1.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 96 ms time-out (nominal) on power-up. This occurs from rising edge of the POR signal and after the first rising edge of $\overline{\text{MCLR}}$ (detected high). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. In most cases the PWRT delay allows the VDD to rise to an acceptable level.

The power-up time delay will vary from chip to chip and to VDD and temperature. See DC parameters for details.

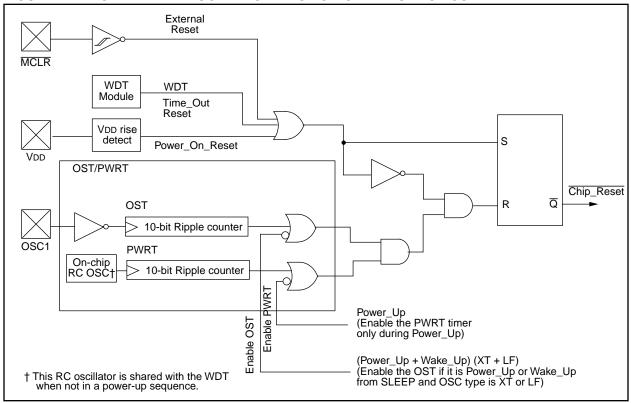


FIGURE 4-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

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5.2 <u>Peripheral Interrupt Enable Register</u> (PIE)

This register contains the individual flag bits for the Peripheral interrupts.

FIGURE 5-3: PIE REGISTER (ADDRESS: 17h, BANK 1)

RBIE	0 R/W - 0 R/W TMR3IE TMR2IE TMR1IE CA2IE CA1IE TXIE R0	CIE R = Readable bit
bit7		bit0 W = Writable bit -n = Value at POR reset
bit 7:	RBIE : PORTB Interrupt on Change Enable bit 1 = Enable PORTB interrupt on change 0 = Disable PORTB interrupt on change	
bit 6:	TMR3IE : Timer3 Interrupt Enable bit 1 = Enable Timer3 interrupt 0 = Disable Timer3 interrupt	
bit 5:	TMR2IE : Timer2 Interrupt Enable bit 1 = Enable Timer2 interrupt 0 = Disable Timer2 interrupt	
bit 4:	TMR1IE : Timer1 Interrupt Enable bit 1 = Enable Timer1 interrupt 0 = Disable Timer1 interrupt	
bit 3:	CA2IE : Capture2 Interrupt Enable bit 1 = Enable Capture interrupt on RB1/CAP2 pin 0 = Disable Capture interrupt on RB1/CAP2 pin	
bit 2:	CA1IE : Capture1 Interrupt Enable bit 1 = Enable Capture interrupt on RB2/CAP1 pin 0 = Disable Capture interrupt on RB2/CAP1 pin	
bit 1:	TXIE : USART Transmit Interrupt Enable bit 1 = Enable Transmit buffer empty interrupt 0 = Disable Transmit buffer empty interrupt	
bit 0:	RCIE : USART Receive Interrupt Enable bit 1 = Enable Receive buffer full interrupt 0 = Disable Receive buffer full interrupt	

6.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC17C4X; program memory and data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle.

The data memory can further be broken down into General Purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

6.1 Program Memory Organization

PIC17C4X devices have a 16-bit program counter capable of addressing a 64K x 16 program memory space. The reset vector is at 0000h and the interrupt vectors are at 0008h, 0010h, 0018h, and 0020h (Figure 6-1).

6.1.1 PROGRAM MEMORY OPERATION

The PIC17C4X can operate in one of four possible program memory configurations. The configuration is selected by two configuration bits. The possible modes are:

- Microprocessor
- Microcontroller
- Extended Microcontroller
- Protected Microcontroller

The microcontroller and protected microcontroller modes only allow internal execution. Any access beyond the program memory reads unknown data. The protected microcontroller mode also enables the code protection feature.

The extended microcontroller mode accesses both the internal program memory as well as external program memory. Execution automatically switches between internal and external memory. The 16-bits of address allow a program memory range of 64K-words.

The microprocessor mode only accesses the external program memory. The on-chip program memory is ignored. The 16-bits of address allow a program memory range of 64K-words. Microprocessor mode is the default mode of an unprogrammed device.

The different modes allow different access to the configuration bits, test memory, and boot ROM. Table 6-1 lists which modes can access which areas in memory. Test Memory and Boot Memory are not required for normal operation of the device. Care should be taken to ensure that no unintended branches occur to these areas.

FIGURE 6-1: PROGRAM MEMORY MAP AND STACK

	AND STACK	
	PC<15:0>]
CALL,	RETURN 1 16	1
RETFI		
	Stack Level 1	1
	:	1
	• Stack Level 16	-
	Stack Level 10]
T T	Reset Vector] 0000h
	INT Pin Interrupt Vector	0008h
	Timer0 Interrupt Vector	0010h
	T0CKI Pin Interrupt Vector	0018h
	Peripheral Interrupt Vector	0020h
		0021h
		7FFh (PIC17C42,
<u>></u>		PIC17CR42,
User Memory Space (1)		PIC17C42A)
ace		FFFh
Spe		(PIC17C43
n ∣		PIC17CR43)
		1FFFh (PIC17C44)
		(FIC17C44)
		l
<u>+</u>	FOSC0	FDFFh
> [FOSC0	FE00h FE01h
Jor	WDTPS0	FE02h
len	WDTPS1	FE03h
≥ e	PM0	FE04h
pac	Reserved	FE05h
S IB	PM1	FE06h
figu	Reserved	FE07h
Configuration Memory Space	Reserved	FE08h
		FE0Eh
📕	PM2 ⁽²⁾	FE0Fh
	Test EPROM	FE10h FF5Fh
		FF60h
	Boot ROM	
		FFFFh
Note 1: U	ser memory space may be inter	nal, external, or
	oth. The memory configuration of	
	rocessor mode.	,
	his location is reserved on the F	PIC17C42.
1		

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (3)
Bank 2											
10h	TMR1	Timer1								xxxx xxxx	uuuu uuuu
11h	TMR2	Timer2								xxxx xxxx	uuuu uuuu
12h	TMR3L	TMR3 reg	ister; low b	yte						xxxx xxxx	uuuu uuuu
13h	TMR3H	TMR3 reg	ister; high l	oyte						xxxx xxxx	uuuu uuuu
14h	PR1	Timer1 pe	eriod registe	er						xxxx xxxx	uuuu uuuu
15h	PR2	Timer2 pe	eriod registe	er						xxxx xxxx	uuuu uuuu
16h	PR3L/CA1L	Timer3 pe	eriod registe	er, low byte/c	apture1 regi	ster; low by	te			xxxx xxxx	uuuu uuuu
17h	PR3H/CA1H	Timer3 pe	eriod registe	er, high byte/	capture1 reg	jister; high b	oyte			xxxx xxxx	uuuu uuuu
Bank 3											
10h	PW1DCL	DC1	DC0	—	—	—	—	—	—	xx	uu
11h	PW2DCL	DC1	DC0	TM2PW2	_	—	—	_	_	xx0	uu0
12h	PW1DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
13h	PW2DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
14h	CA2L	Capture2	low byte							xxxx xxxx	uuuu uuuu
15h	CA2H	Capture2	high byte							xxxx xxxx	uuuu uuuu
16h	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h	TCON2	CA2OVF	CA10VF	PWM2ON	PWM10N	CA1/PR3	TMR3ON	TMR2ON	TMR10N	0000 0000	0000 0000
Unbanke	ed										
18h ⁽⁵⁾	PRODL	Low Byte	of 16-bit Pr	oduct (8 x 8	Hardware M	lultiply)				XXXX XXXX	uuuu uuuu
19h ⁽⁵⁾	PRODH	High Byte	of 16-bit P	roduct (8 x 8	B Hardware N	/lultiply)				xxxx xxxx	uuuu uuuu
Legend:	x = unknown,	u = unchar	nged, - = ur	implemente	d read as '0'	, q - value d	epends on o	condition. Sha	ded cells ar	e unimplemente	ed, read as '0'.

TABLE 6-3: SPECIAL FUNCTION REGISTERS (Cont.'d)

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<15:8> whose contents are updated from or transferred to the upper byte of the program counter. The TO and PD status bits in CPUSTA are not affected by a MCLR reset. Other (non power-up) resets include: external reset through MCLR and the Watchdog Timer Reset. The following values are for both TBLPTRL and TBLPTRH:

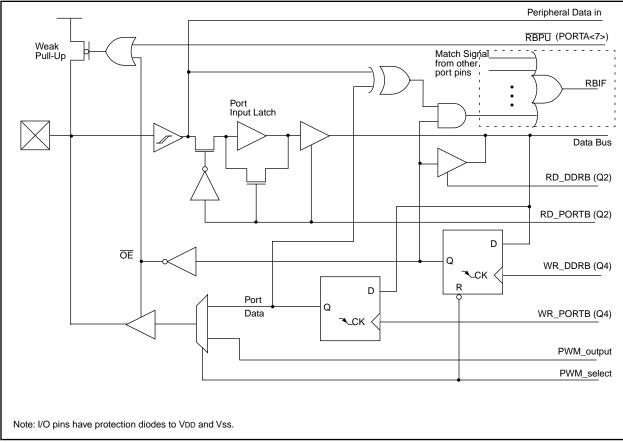
2:

3: 4:

All PIC17C4X devices (Power-on Reset 0000 0000) and (All other resets 0000 0000) except the PIC17C42 (Power-on Reset xxxx xxxx) and (All other resets uuuu uuuu) The PRODL and PRODH registers are not implemented on the PIC17C42.

5:

FIGURE 9-5: BLOCK DIAGRAM OF RB3 AND RB2 PORT PINS



9.5 I/O Programming Considerations

9.5.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. For example, the BCF and BSF instructions read the register into the CPU, execute the bit operation, and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g. bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Reading a port reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (BCF, BSF, BTG, etc.) on a port, the value of the port pins is read, the desired operation is performed with this value, and the value is then written to the port latch.

Example 9-5 shows the effect of two sequential read-modify-write instructions on an I/O port.

EXAMPLE 9-5: READ MODIFY WRITE INSTRUCTIONS ON AN I/O PORT

; Initial PORT settings: PORTB<7:4> Inputs PORTB<3:0> Outputs ; ; PORTB<7:6> have pull-ups and are ; not connected to other circuitry ; PORT latch PORT pins ; ; _____ _____ ; PORTB, 7 BCF 01pp pppp 11pp pppp BCF PORTB, 6 10pp pppp 11pp pppp ; BCF DDRB, 7 10pp pppp 11pp pppp BCF DDRB, 6 10pp pppp 10pp pppp ; ; Note that the user may have expected the ; pin values to be 00pp pppp. The 2nd BCF ; caused RB7 to be latched as the pin value ; (High).

Note: A pin actively outputting a Low or High should not be driven from external devices in order to change the level on this pin (i.e. "wired-or", "wired-and"). The resulting high output currents may damage the device.

9.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 9-9). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before executing the instruction that reads the values on that I/O port. Otherwise, the previous state of that pin may be read into the CPU rather than the "new" state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 9-9: SUCCESSIVE I/O OPERATION

Instruction fetched	Q1 Q2 Q3 Q4 PC MOVWF PORTB write to PORTB	PC + 1	Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 <u>PC+2</u> <u>PC+3</u> NOP NOP	Note: This example shows a write to PORTB followed by a read from PORTB. Note that: data setup time = (0.25 Tcy - TPD) where TcY = instruction cycle. TPD = propagation delay
RB7:RB0			X	Therefore, at higher clock frequencies, a write followed by a
			Port pin sampled here	read may be problematic.
Instruction executed		MOVWF PORTB write to PORTB	MOVF PORTB,W NOP	
			· · · · ·	

12.1 <u>Timer1 and Timer2</u>

12.1.1 TIMER1, TIMER2 IN 8-BIT MODE

Both Timer1 and Timer2 will operate in 8-bit mode when the T16 bit is clear. These two timers can be independently configured to increment from the internal instruction cycle clock or from an external clock source on the RB4/TCLK12 pin. The timer clock source is configured by the TMRxCS bit (x = 1 for Timer1 or = 2 for Timer2). When TMRxCS is clear, the clock source is internal and increments once every instruction cycle (Fosc/4). When TMRxCS is set, the clock source is the RB4/TCLK12 pin, and the timer will increment on every falling edge of the RB4/TCLK12 pin.

The timer increments from 00h until it equals the Period register (PRx). It then resets to 00h at the next increment cycle. The timer interrupt flag is set when the timer is reset. TMR1 and TMR2 have individual interrupt flag bits. The TMR1 interrupt flag bit is latched into TMR1IF, and the TMR2 interrupt flag bit is latched into TMR2IF.

Each timer also has a corresponding interrupt enable bit (TMRxIE). The timer interrupt can be enabled by setting this bit and disabled by clearing this bit. For peripheral interrupts to be enabled, the Peripheral Interrupt Enable bit must be enabled (PEIE is set) and global interrupts must be enabled (GLINTD is cleared).

The timers can be turned on and off under software control. When the Timerx On control bit (TMRxON) is set, the timer increments from the clock source. When TMRxON is cleared, the timer is turned off and cannot cause the timer interrupt flag to be set.

12.1.1.1 EXTERNAL CLOCK INPUT FOR TIMER1 OR TIMER2

When TMRxCS is set, the clock source is the RB4/TCLK12 pin, and the timer will increment on every falling edge on the RB4/TCLK12 pin. The TCLK12 input is synchronized with internal phase clocks. This causes a delay from the time a falling edge appears on TCLK12 to the time TMR1 or TMR2 is actually incremented. For the external clock input timing requirements, see the Electrical Specification section.

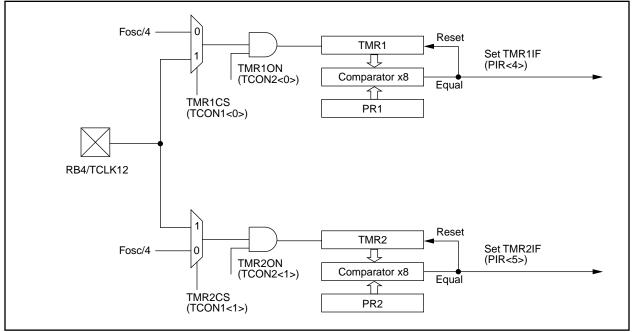


FIGURE 12-3: TIMER1 AND TIMER2 IN TWO 8-BIT TIMER/COUNTER MODE

BAUD RATE	Fosc = 3	3 MHz	SPBRG value	Fosc = 2	5 MHz	SPBRG value	Fosc = 2	0 MHz	SPBRG value	Fosc = 1	6 MHz	SPBRG value
(K)	KBAUD	%ERROR	(decimal)									
0.3	NA	_	_	NA	_	_	NA	_	_	NA		_
1.2	NA	_	_									
2.4	NA	_	_	NA	_	_	NA	_	_	NA	—	_
9.6	NA	—	—									
19.2	NA	_	—	NA	—	—	19.53	+1.73	255	19.23	+0.16	207
76.8	77.10	+0.39	106	77.16	+0.47	80	76.92	+0.16	64	76.92	+0.16	51
96	95.93	-0.07	85	96.15	+0.16	64	96.15	+0.16	51	95.24	-0.79	41
300	294.64	-1.79	27	297.62	-0.79	20	294.1	-1.96	16	307.69	+2.56	12
500	485.29	-2.94	16	480.77	-3.85	12	500	0	9	500	0	7
HIGH	8250	_	0	6250	_	0	5000	_	0	4000	_	0
LOW	32.22	_	255	24.41	_	255	19.53	_	255	15.625	_	255

BAUD	Fosc = 10 M	Hz	SPBRG	Fosc = 7.159	MHz	SPBRG	Fosc = 5.068	SPBRG	
RATE (K)	KBAUD	%ERROR	value (decimal)	KBAUD	%ERROR	value (decimal)	KBAUD	%ERROR	value (decimal)
0.3	NA	_	_	NA	_	_	NA	_	_
1.2	NA	_	_	NA	_	_	NA	_	_
2.4	NA	_	_	NA	_	_	NA	_	_
9.6	9.766	+1.73	255	9.622	+0.23	185	9.6	0	131
19.2	19.23	+0.16	129	19.24	+0.23	92	19.2	0	65
76.8	75.76	-1.36	32	77.82	+1.32	22	79.2	+3.13	15
96	96.15	+0.16	25	94.20	-1.88	18	97.48	+1.54	12
300	312.5	+4.17	7	298.3	-0.57	5	316.8	+5.60	3
500	500	0	4	NA	_	_	NA	_	_
HIGH	2500	_	0	1789.8	_	0	1267	_	0
LOW	9.766	—	255	6.991	—	255	4.950	—	255
	F000 0 570	OSC = 3.579 MHz SPBRG		FOSC = 1 MHz SPBRG			Fosc = 32.76		
BAUD	FOSC = 3.579	MHZ			Z		030 = 32.70		SPBRG
BAUD RATE (K)	KBAUD	MHZ %ERROR	SPBRG value (decimal)	KBAUD	2 %ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)
RATE			value			value			value
RATE (K)	KBAUD		value	KBAUD		value	KBAUD	%ERROR	value (decimal)
RATE (K) 0.3	KBAUD		value	KBAUD NA	%ERROR	value (decimal)	KBAUD 0.303	%ERROR +1.14	value (decimal) 26
RATE (K) 0.3 1.2	KBAUD NA NA		value	KBAUD NA 1.202	%ERROR 	value (decimal) — 207	KBAUD 0.303 1.170	%ERROR +1.14	value (decimal) 26
RATE (K) 0.3 1.2 2.4	KBAUD NA NA NA	%ERROR 	value (decimal) — — —	KBAUD NA 1.202 2.404	%ERROR +0.16 +0.16	value (decimal) 207 103	KBAUD 0.303 1.170 NA	%ERROR +1.14	value (decimal) 26
RATE (K) 0.3 1.2 2.4 9.6	KBAUD NA NA NA 9.622	%ERROR — — +0.23	value (decimal) — — — 92	KBAUD NA 1.202 2.404 9.615	%ERROR +0.16 +0.16 +0.16	value (decimal) — 207 103 25	KBAUD 0.303 1.170 NA NA	%ERROR +1.14	value (decimal) 26
RATE (K) 0.3 1.2 2.4 9.6 19.2	KBAUD NA NA 9.622 19.04	%ERROR — — +0.23 -0.83	value (decimal) — — 92 46	KBAUD NA 1.202 2.404 9.615 19.24	%ERROR +0.16 +0.16 +0.16 +0.16	value (decimal) — 207 103 25 12	KBAUD 0.303 1.170 NA NA NA	%ERROR +1.14	value (decimal) 26
RATE (K) 0.3 1.2 2.4 9.6 19.2 76.8	KBAUD NA NA 9.622 19.04 74.57	%ERROR — — +0.23 -0.83 -2.90	value (decimal) — — — 92 46 11	KBAUD NA 1.202 2.404 9.615 19.24 83.34	%ERROR +0.16 +0.16 +0.16 +0.16	value (decimal) — 207 103 25 12	KBAUD 0.303 1.170 NA NA NA NA	%ERROR +1.14	value (decimal) 26
RATE (K) 0.3 1.2 2.4 9.6 19.2 76.8 96	KBAUD NA NA 9.622 19.04 74.57 99.43	%ERROR — +0.23 -0.83 -2.90 _3.57	value (decimal) — — 92 46 11 8	KBAUD NA 1.202 2.404 9.615 19.24 83.34 NA	%ERROR +0.16 +0.16 +0.16 +0.16	value (decimal) — 207 103 25 12	KBAUD 0.303 1.170 NA NA NA NA NA	%ERROR +1.14	value (decimal) 26
RATE (K) 0.3 1.2 2.4 9.6 19.2 76.8 96 300	KBAUD NA NA 9.622 19.04 74.57 99.43 298.3	%ERROR — +0.23 -0.83 -2.90 _3.57	value (decimal) — — 92 46 11 8	KBAUD NA 1.202 2.404 9.615 19.24 83.34 NA NA	%ERROR +0.16 +0.16 +0.16 +0.16	value (decimal) — 207 103 25 12	KBAUD 0.303 1.170 NA NA NA NA NA NA	%ERROR +1.14	value (decimal) 26

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
13h, Bank 0	RCSTA	SPEN	RX9	SREN	CREN	-	FERR	OERR	RX9D	0000 -00x	0000 -00u
16h, Bank 0	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	xxxx xxxx	uuuu uuuu
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	-	_	TRMT	TX9D	00001x	00001u
17h, Bank 0	SPBRG	Baud rate	generator	register						xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used for synchronous slave transmission.

Note 1: Other (non power-up) resets include: external reset through MCLR and Watchdog Timer Reset.

TABLE 13-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
13h, Bank0	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00u
14h, Bank0	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	xxxx xxxx	uuuu uuuu
17h, Bank1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	_	-	TRMT	TX9D	00001x	00001u
17h, Bank0	SPBRG	Baud rate	generator	register						xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used for synchronous slave reception.

Note 1: Other (non power-up) resets include: external reset through MCLR and Watchdog Timer Reset.

CPFS	SLT	Compare f with WREG, skip if f < WREG							
Synta	ax:	[label]	CPFSLT f						
Opera	ands:	$0 \le f \le 25$	$0 \le f \le 255$						
Operation:		skip if (f) <	(f) – (WREG), skip if (f) < (WREG) (unsigned comparison)						
Statu	s Affected:	None							
Enco	ding:	0011	0000 ffi	ff ffff					
Description:		location 'f' performing If the conte WREG, the discarded	Compares the contents of data memory location 'f' to the contents of WREG by performing an unsigned subtraction. If the contents of 'f' < the contents of WREG, then the fetched instruction is discarded and an NOP is executed instead making this a two-cycle instruc- tion.						
Word	s:	1							
Cycle	es:	1 (2)							
Q Cy	cle Activity:								
	Q1	Q2	Q3	Q4					
	Decode	Read register 'f'	Execute	NOP					
lf skip	o:								
-	Q1	Q2	Q3	Q4					
	Forced NOP	NOP	Execute	NOP					
<u>Exarr</u>	nple:	HERE NLESS LESS	CPFSLT REG : :						
E	Before Instru PC W		ddress (HERE)						
W = ? After Instruction If REG < WREG; PC = Address (LESS) If REG ≥ WREG; PC = Address (NLESS)									

DAW		Decimal	Decimal Adjust WREG Register						
Syntax	K:	[<i>label</i>] D	AW f,s						
Opera	nds:	$0 \le f \le 25$ s $\in [0,1]$	5						
Opera	tion:	⁻ WREG else	If [WREG<3:0> >9] .OR. [DC = 1] then WREG<3:0> + 6 \rightarrow f<3:0>, s<3:0>; else WREG<3:0> \rightarrow f<3:0>, s<3:0>;						
		If [WREG<7:4> >9] .OR. [C = 1] then WREG<7:4> + 6 → f<7:4>, s<7:4 else							
Status	Affected:	C	$<7:4> \rightarrow f<7:$	4>, S<7:4>					
Encod		0010	111s ff	ff ffff					
Descri	U		ts the eight bi						
		tion of two BCD forma packed BC s = 0: Ro m W	WREG resulting from the earlier addi- tion of two variables (each in packed BCD format) and produces a correct packed BCD result. s = 0: Result is placed in Data memory location 'f' and WREG.						
			s = 1: Result is placed in Data memory location 'f'.						
Words	:	1							
Cycles	8:	1							
Q Cyc	le Activity:			•					
	Q1 Decode	Q2 Read	Q3 Execute	Q4 Write					
	Decode	register 'f'	Execute	register 'f' and other specified register					
Exam	ole1:	DAW RE	G1, 0						
B	 efore Instru	iction							
	WREG REG1 C DC	= 0xA5 = ?? = 0 = 0							
REG1 = C =		ion = 0x05 = 0x05 = 1 = 0							
В	efore Instru								
	WREG REG1 C	= 0xCE = ?? = 0							

U	-	0
DC	=	0
After Instruc		
WREG	=	0x24
REG1	=	0x24
С	=	1
DC	=	0

Applicable Devices 42 R42 42A 43 R43 44

19.1 DC CHARACTERISTICS:

PIC17CR42/42A/43/R43/44-16 (Commercial, Industrial) PIC17CR42/42A/43/R43/44-25 (Commercial, Industrial) PIC17CR42/42A/43/R43/44-33 (Commercial, Industrial)

DC CHARACT		Standard Operating Conditions (unless otherwise stated) Operating temperature					
	ERISTI	63				-40°C	
		i				0°C	\leq TA \leq +70°C for commercial
Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
D001	Vdd	Supply Voltage	4.5	_	6.0	V	
D002	Vdr	RAM Data Retention Voltage (Note 1)	1.5 *	_	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	_	Vss	-	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.060 *	_	_	mV/ms	See section on Power-on Reset for details
D010	IDD	Supply Current	-	3	6	mA	Fosc = 4 MHz (Note 4)
D011		(Note 2)	-	6	12 *	mA	Fosc = 8 MHz
D012			-	11	24 *	mA	Fosc = 16 MHz
D013			-	19	38	mA	Fosc = 25 MHz
D015			-	25	50	mA	Fosc = 33 MHz
D014			-	95	150	μA	Fosc = 32 kHz,
							WDT enabled (EC osc configuration)
D020	IPD	Power-down	_	10	40	μA	VDD = 5.5V, WDT enabled
D021		Current (Note 3)	-	< 1	5	μA	VDD = 5.5V, WDT disabled

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD or VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

Current consumed from the oscillator and I/O's driving external capacitive or resistive loads needs to be considered.

For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as: $VDD / (2 \bullet R)$. For capacitive loads, the current can be estimated (for an individual I/O pin) as (CL • VDD) • f

CL = Total capacitive load on the I/O pin; f = average frequency the I/O pin switches.

The capacitive currents are most significant when the device is configured for external execution (includes extended microcontroller mode).

- 3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VbD and Vss.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

Applicable Devices 42 R42 42A 43 R43 44

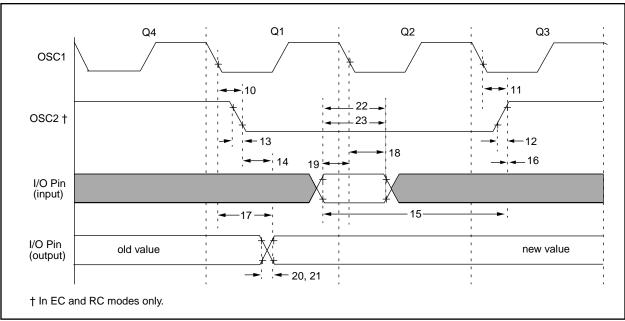


FIGURE 19-3: CLKOUT AND I/O TIMING

TABLE 19-3:	CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
10	TosH2ckL	OSC1↓ to CLKOUT↓		—	15‡	30 ‡	ns	Note 1
11	TosH2ckH	OSC1↓ to CLKOUT	\uparrow	—	15‡	30 ‡	ns	Note 1
12	TckR	CLKOUT rise time		—	5‡	15 ‡	ns	Note 1
13	TckF	CLKOUT fall time		—	5‡	15 ‡	ns	Note 1
14	TckH2ioV	CLKOUT [↑] to Port PIC17CR42/42A/43/ out valid R43/44		—	—	0.5TCY + 20 ‡	ns	Note 1
			PIC17LCR42/42A/43/ R43/44	—	—	0.5TCY + 50 ‡	ns	Note 1
15	TioV2ckH	Port in valid before PIC17CR42/42A/43/ CLKOUT [↑] R43/44		0.25Tcy + 25 ‡	_	—	ns	Note 1
			PIC17LCR42/42A/43/ R43/44	0.25Tcy + 50 ‡	—		ns	Note 1
16	TckH2iol	Port in hold after CL	KOUT	0 ‡	—	—	ns	Note 1
17	TosH2ioV	OSC1↓ (Q1 cycle) t	o Port out valid	—	—	100 ‡	ns	
18	TosH2iol	OSC1↓ (Q2 cycle) t (I/O in hold time)	o Port input invalid	0‡	—		ns	
19	TioV2osH	Port input valid to OSC1↓ (I/O in setup time)		30 ‡	—		ns	
20	TioR	Port output rise time		—	10 ‡	35 ‡	ns	
21	TioF	Port output fall time		—	10 ‡	35 ‡	ns	
22	TinHL	INT pin high or low	time	25 *	—	—	ns	
23	TrbHL	RB7:RB0 change IN	NT high or low time	25 *	—	—	ns	

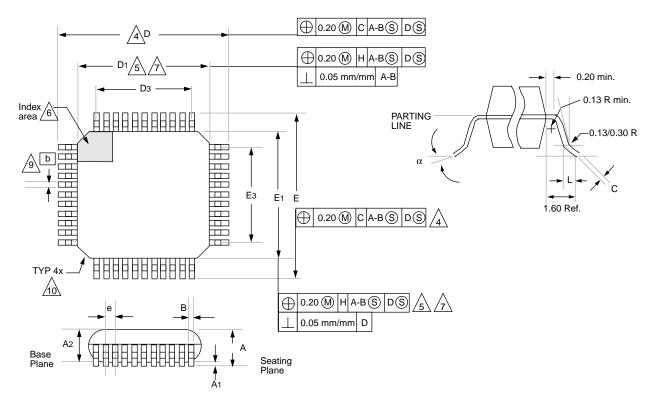
These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

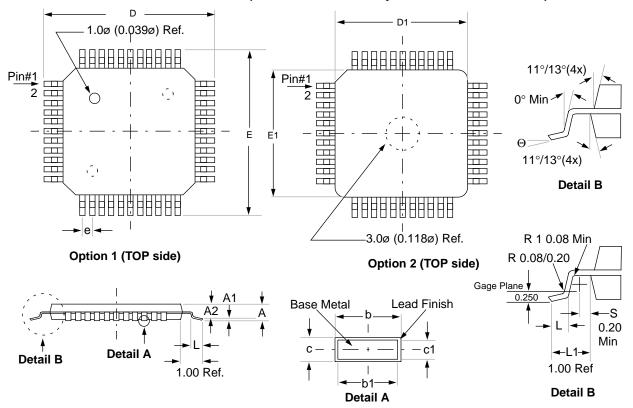
t These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Measurements are taken in EC Mode where CLKOUT output is 4 x Tosc.





Package Group: Plastic MQFP							
		Millimeters		Inches			
Symbol	Min	Max	Notes	Min	Мах	Notes	
α	0°	7 °		0°	7 °		
А	2.000	2.350		0.078	0.093		
A1	0.050	0.250		0.002	0.010		
A2	1.950	2.100		0.768	0.083		
b	0.300	0.450	Typical	0.011	0.018	Typical	
С	0.150	0.180		0.006	0.007		
D	12.950	13.450		0.510	0.530		
D1	9.900	10.100		0.390	0.398		
D3	8.000	8.000	Reference	0.315	0.315	Reference	
E	12.950	13.450		0.510	0.530		
E1	9.900	10.100		0.390	0.398		
E3	8.000	8.000	Reference	0.315	0.315	Reference	
е	0.800	0.800		0.031	0.032		
L	0.730	1.030		0.028	0.041		
Ν	44	44		44	44		
CP	0.102	_		0.004	_		



21.5	44-Lead Plastic Surface Mount (TOFP 10x10 mm Body	v 1.0/0.10 mm Lead Form)
21.0			

Package Group: Plastic TQFP							
	Millimeters		Inches				
Symbol	Min	Max	Notes	Min	Max	Notes	
A	1.00	1.20		0.039	0.047		
A1	0.05	0.15		0.002	0.006		
A2	0.95	1.05		0.037	0.041		
D	11.75	12.25		0.463	0.482		
D1	9.90	10.10		0.390	0.398		
E	11.75	12.25		0.463	0.482		
E1	9.90	10.10		0.390	0.398		
L	0.45	0.75		0.018	0.030		
е	0.80	BSC		0.031			
b	0.30	0.45		0.012	0.018		
b1	0.30	0.40		0.012	0.016		
С	0.09	0.20		0.004	0.008		
c1	0.09	0.16		0.004	0.006		
Ν	44	44		44	44		
Θ	0°	7°		0°	7 °		

Note 1: Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25m/m (0.010") per side. D1 and E1 dimensions including mold mismatch.

2: Dimension "b" does not include Dambar protrusion, allowable Dambar protrusion shall be 0.08m/m (0.003")max.

3: This outline conforms to JEDEC MS-026.

PIC16C7X Family of Devices

E.5

Clock Memory Peripherals Features Clock Memory Peripherals Features Clock Memory Peripherals Features Features Clock Memory Clock Memor	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	TMR0 — — — 4 4 13 3.0-6.0 Yes — 18-pin DIP, SOIC	IMR0 4 4 13 3.0-6.0 Yes 18-pin DIP, SOIC; 20-pin SSOP 20-pin SSOP 20-pin SSOP 20-pin SSOP 20-pin SSOP	TMR0, 1 SPI/I ² C - 5 8 22 2.5-6.0 Yes 28-pin SDIP, SOIC, SSOP TMR1, TMR2 - 5 8 22 2.5-6.0 Yes 28-pin SDIP, SOIC, SSOP	TMR0, 2 SPI/I ² C, - 5 11 22 3.0-6.0 Yes - 28-pin SDIP, SOIC TMR1, TMR2 USART	TMR0, 2 SPI/I ² C, 5 11 22 2.5-6.0 Yes Yes 28-pin SDIP, SOIC TMR1, TMR2 USART	TMR0, 2 SPI/I ² C, Yes 8 12 33 3.0-6.0 Yes - 40-pin DIP; TMR1, TMR2 USART 12 33 3.0-6.0 Yes - 40-pin DIP;	TMR0, 2 SPI/I ² C, Yes 8 12 33 2.5-6.0 Yes 40-pin DIP; TMR1, TMR2 USART 12 33 2.5-6.0 Yes 44-pin PLCC, MQFP, TQFP	All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.
C C C C C C C C C C C C C C C C C C C	TMR0	TMR0	TMR0	TMR0, TMR1, TM	TMR0, TMR1, TM	TMR0, TMR1, TM	TMR0, TMR1, TM	TMR0, TMR1, TM	All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable c capability.
-10 TOLISTO	36 044	36	89	128	192	192	192	192	y device
	512 512	ź	Ϋ́	2K	44 A	4 K	4K	4 K	⁷ Family
	20 10	20	20	20	20	20	20	20	C16/17 vility.
	PIC16C710	PIC16C71	PIC16C711	PIC16C72	PIC16C73	PIC16C73A ⁽¹⁾	PIC16C74	PIC16C74A ⁽¹⁾	All PIC16/ capability.

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