Infineon Technologies - MB95F378EPMC1-G-SNE2 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

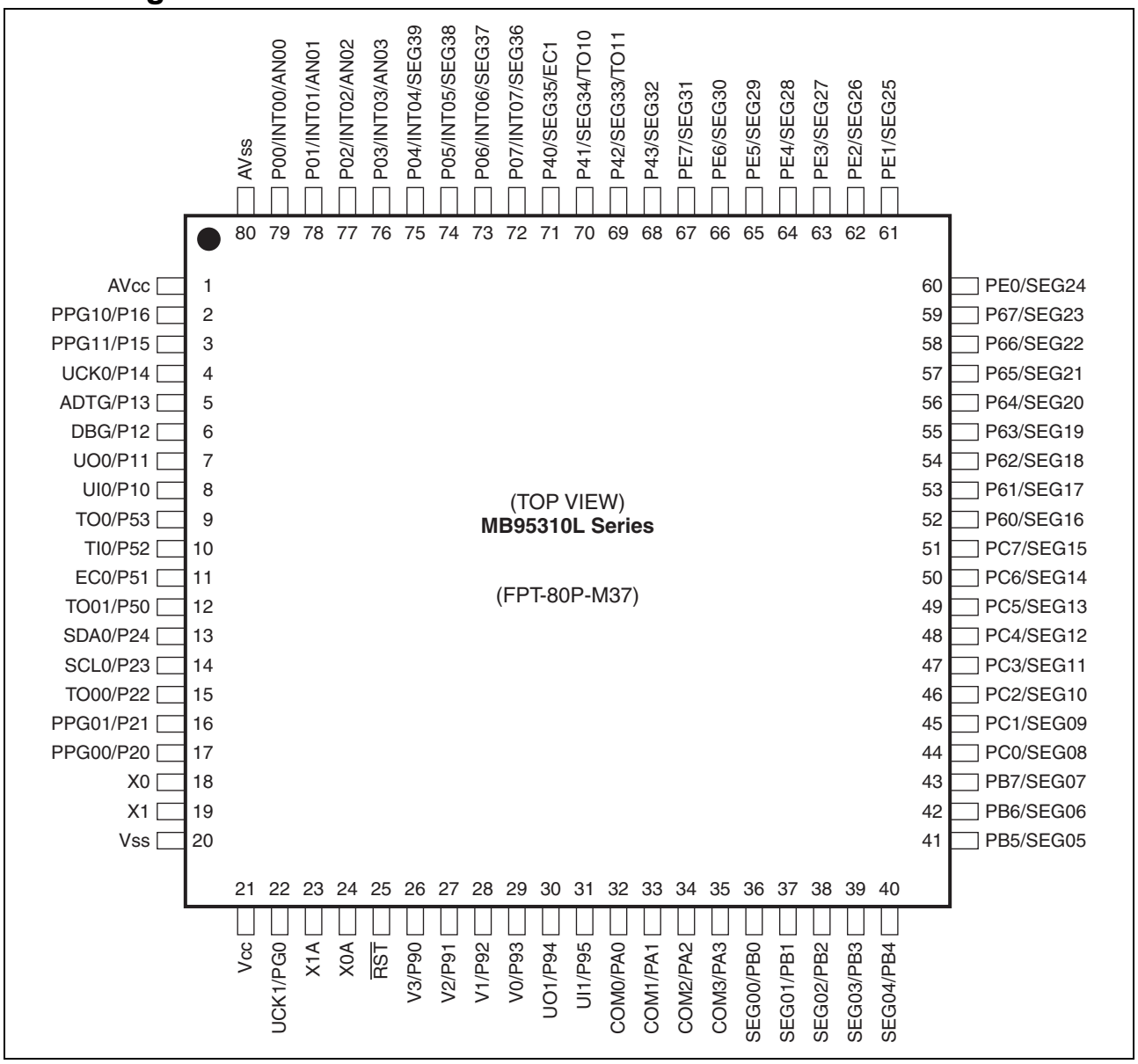
Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.98K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f378epmc1-g-sne2

■ MB95370L Series

Part number / Parameter	MB95F374E	MB95F376E	MB95F378E	MB95F374L	MB95F376L	MB95F378L
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	496 bytes	1008 bytes	2032 bytes	496 bytes	1008 bytes	2032 bytes
Low-voltage detection reset	Yes			No		
Reset input	Dedicated					
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max): 55 • CMOS I/O: 52 • N-ch open drain: 3					
Time-base timer	Interval time: 0.256 ms - 8.3 s (external clock frequency = 4 MHz)					
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
I^2C	1 channel					
	• Master/Slave sending and receiving • Bus error function and arbitration function • Detecting transmitting direction function • Start condition repeated generation and detection functions • Built-in wake-up function					
UART/SIO	2 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
8/10-bit A/D converter	4 channels					
	8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	2 channels					
	• Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					

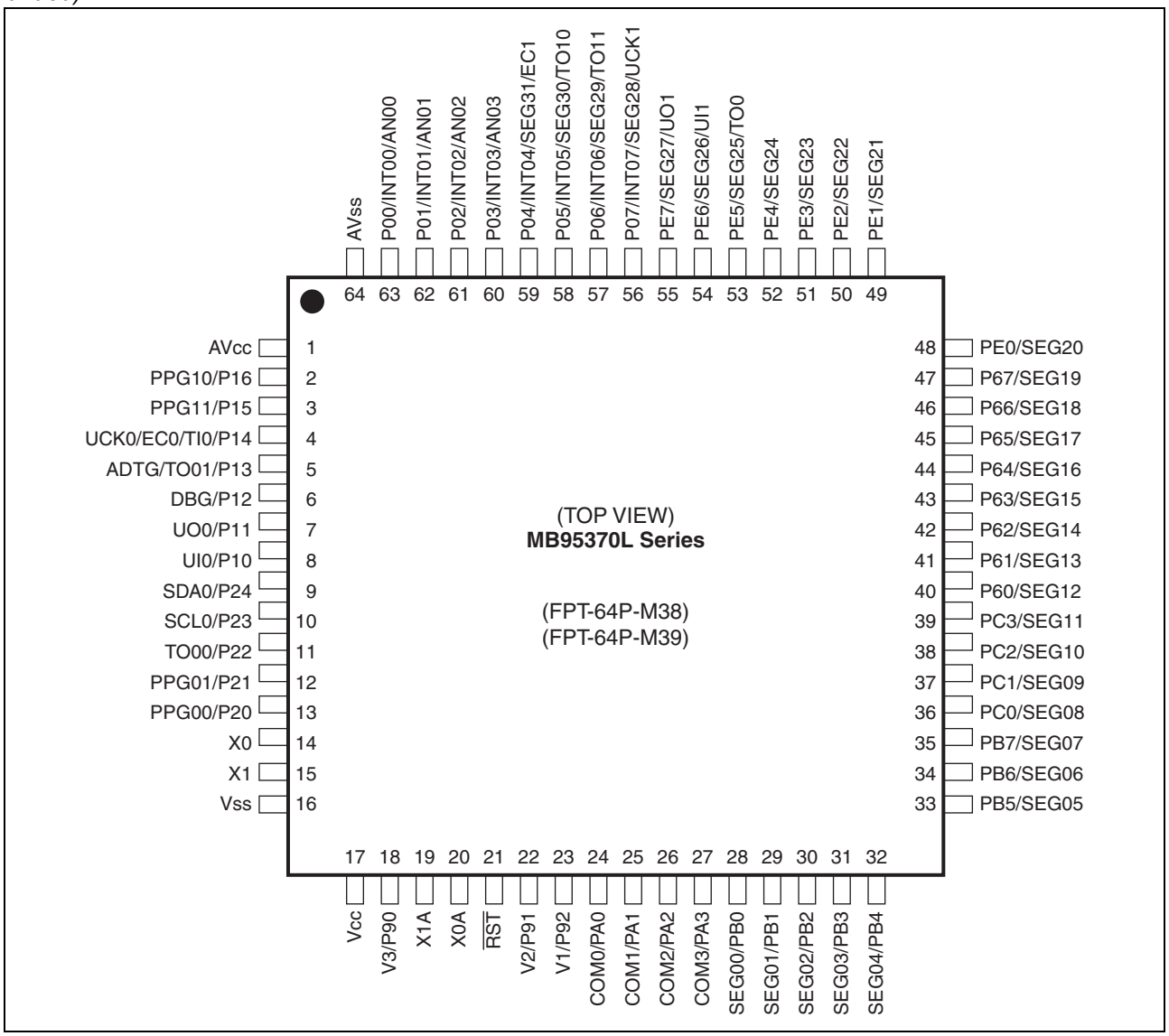
(Continued)

5. Pin Assignment



(Continued)

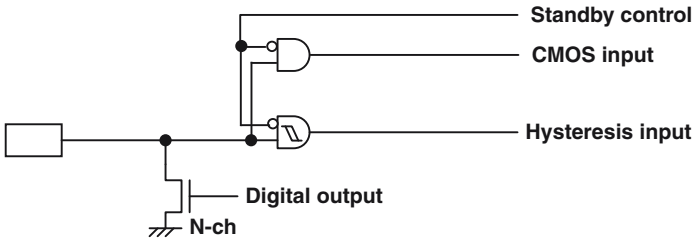
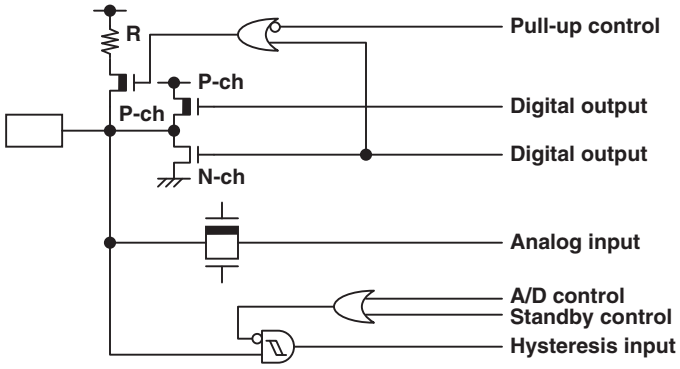
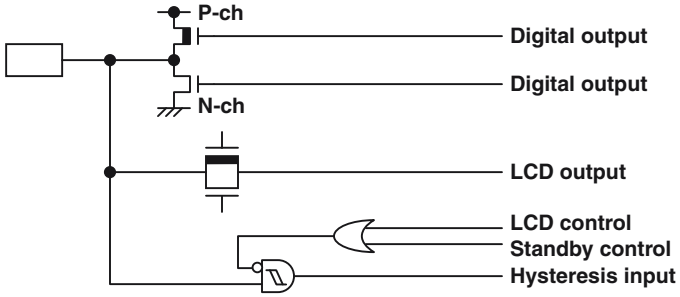
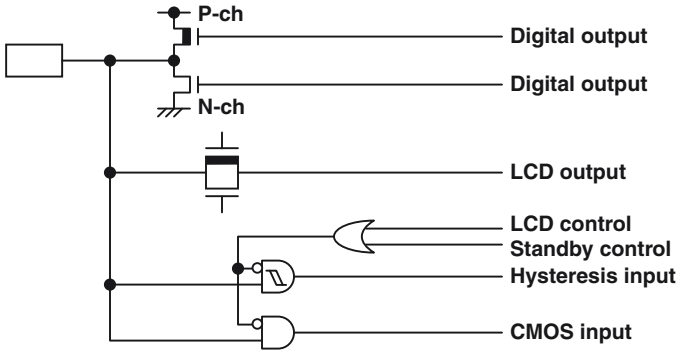
(Continued)


AVss
P00/INT00/AN00
P01/INT01/AN01
P02/INT02/AN02
P03/INT03/AN03
P04/INT04/SEG31/EC1
P05/INT05/SEG30/TO10
P06/INT06/SEG29/TO11
P07/INT07/SEG28/UCK1
PE7/SEG27/UO1
PE6/SEG26/UI1
PE5/SEG25/TO0
PE4/SEG24
PE3/SEG23
PE2/SEG22
PE1/SEG21
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
AVcc 1
PPG10/P16 2
PPG11/P15 3
UCK0/EC0/TI0/P14 4
ADTG/TO01/P13 5
DBG/P12 6
UO0/P11 7
UI0/P10 8
SDA0/P24 9
SCL0/P23 10
TO00/P22 11
PPG01/P21 12
PPG00/P20 13
X0 14
X1 15
Vss 16
48 PE0/SEG20
47 P67/SEG19
46 P66/SEG18
45 P65/SEG17
44 P64/SEG16
43 P63/SEG15
42 P62/SEG14
41 P61/SEG13
40 P60/SEG12
39 PC3/SEG11
38 PC2/SEG10
37 PC1/SEG09
36 PC0/SEG08
35 PB7/SEG07
34 PB6/SEG06
33 PB5/SEG05
(TOP VIEW)
MB95370L Series
(FPT-64P-M38)
(FPT-64P-M39)
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
Vcc
V3/P90
X1A
X0A
RST
V2/P91
V1/P92
COM0/PA0
COM1/PA1
COM2/PA2
COM3/PA3
SEG00/PB0
SEG01/PB1
SEG02/PB2
SEG03/PB3
SEG04/PB4

7. Pin Description (MB95370L Series)

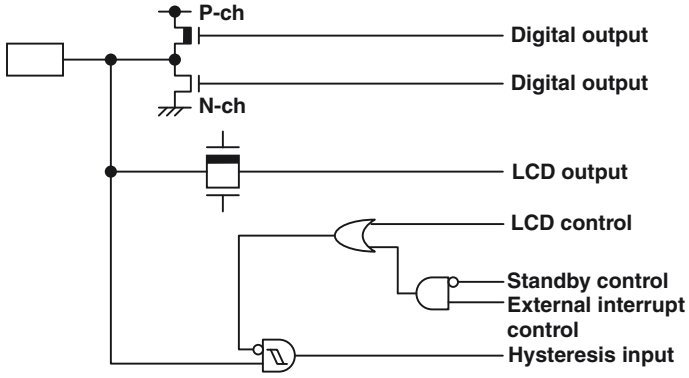
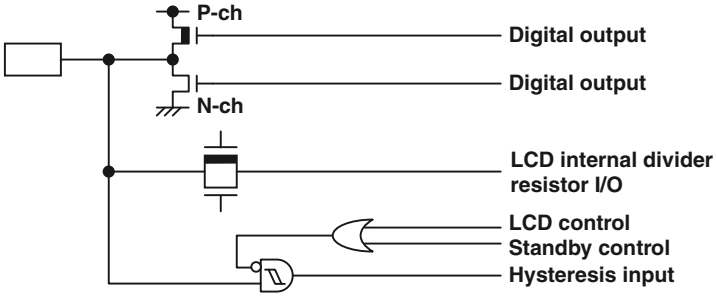
Pin no.	Pin name	I/O circuit type*	Function
1	AV_{CC}	—	A/D converter power supply pin
2	P16	H	General-purpose I/O port
	PPG10		8/16-bit PPG ch. 1 output pin
3	P15	H	General-purpose I/O port
	PPG11		8/16-bit PPG ch. 1 output pin
4	P14	H	General-purpose I/O port
	UCK0		UART/SIO ch. 0 clock I/O pin
	EC0		8/16-bit composite timer ch. 0 clock input pin The pin can also be used as the event counter input pin when the event counter function is used.
	TI0		16-bit reload timer ch. 0 input pin
5	P13	H	General-purpose I/O port
	ADTG		A/D trigger input (ADTG) pin
	TO01		8/16-bit composite timer ch. 0 output pin
6	P12	C	General-purpose I/O port
	DBG		DBG input pin
7	P11	H	General-purpose I/O port
	UO0		UART/SIO ch. 0 data output pin
8	P10	G	General-purpose I/O port
	UI0		UART/SIO ch. 0 data input pin
9	P24	I	General-purpose I/O port
	SDA0		I^2C data I/O pin
10	P23	I	General-purpose I/O port
	SCL0		I^2C clock I/O pin
11	P22	H	General-purpose I/O port
	TO00		8/16-bit composite timer ch. 0 output pin
12	P21	H	General-purpose I/O port
	PPG01		8/16-bit PPG ch. 0 output pin
13	P20	H	General-purpose I/O port
	PPG00		8/16-bit PPG ch. 0 output pin
14	X0	A	Main clock oscillation pin
15	X1	A	Main clock oscillation pin
16	V_{SS}	—	Power supply pin (GND)
17	V_{CC}	—	Power supply pin
18	P90	R	General-purpose I/O port
	V3		LCDC drive power supply pin

(Continued)

Type	Circuit	Remarks
I		■ N-ch open drain output ■ CMOS input ■ Hysteresis input
J		■ CMOS output ■ Hysteresis input ■ Analog input ■ Pull-up control available
M		■ CMOS output ■ LCD output ■ Hysteresis input
N		■ CMOS output ■ LCD output ■ Hysteresis input ■ CMOS input

(Continued)

(Continued)

Type	Circuit	Remarks
Q		■ CMOS output ■ LCD output ■ Hysteresis input
R		■ CMOS output ■ LCD power supply ■ Hysteresis input

9. Notes On Device Handling

■ Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “18.1 Absolute Maximum Ratings” of “Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

■ Stabilizing supply voltage

Supply voltage must be stabilized.

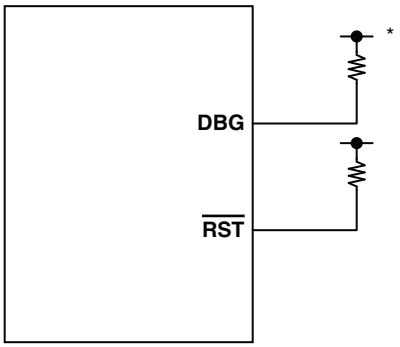
A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

■ Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

• DBG/$\overline{\text{RST}}$ pins connection diagram

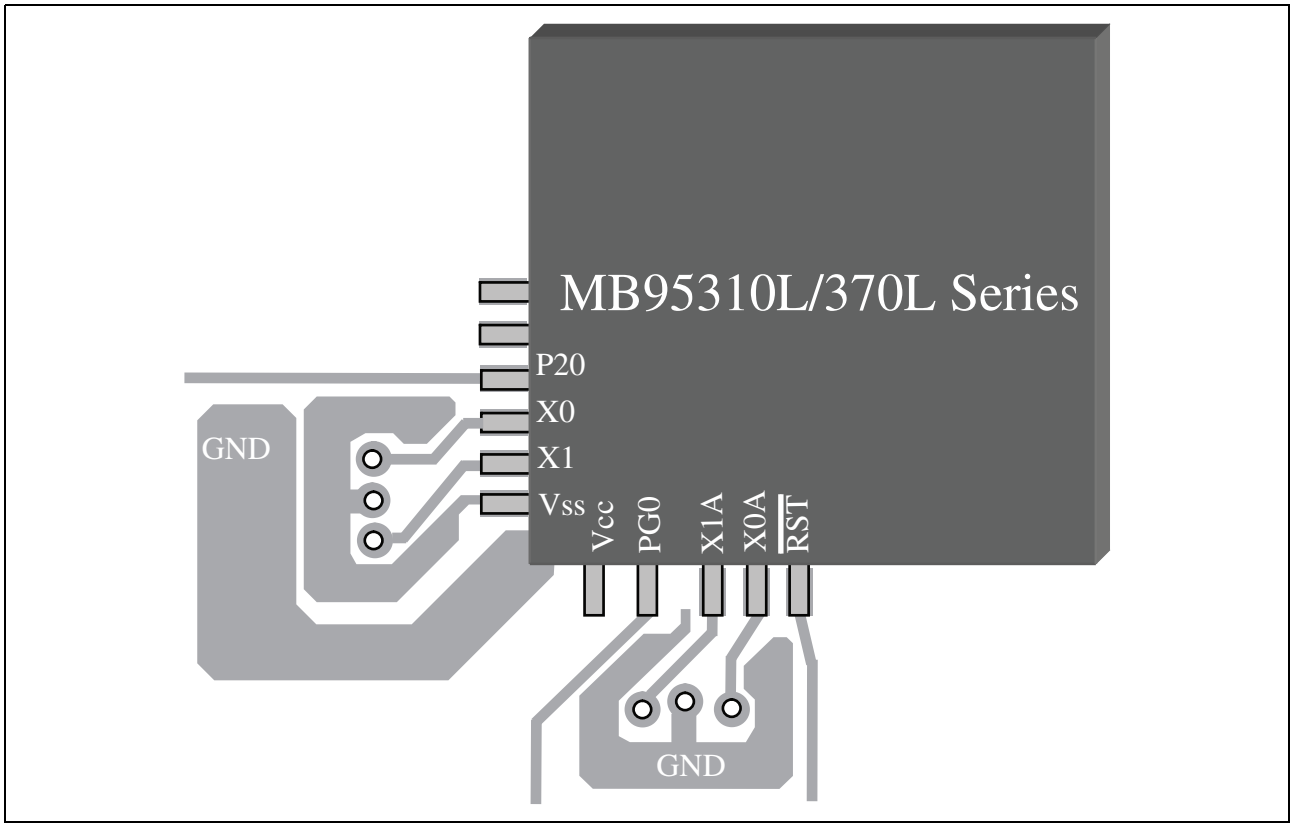


*: Since the DBG input pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.

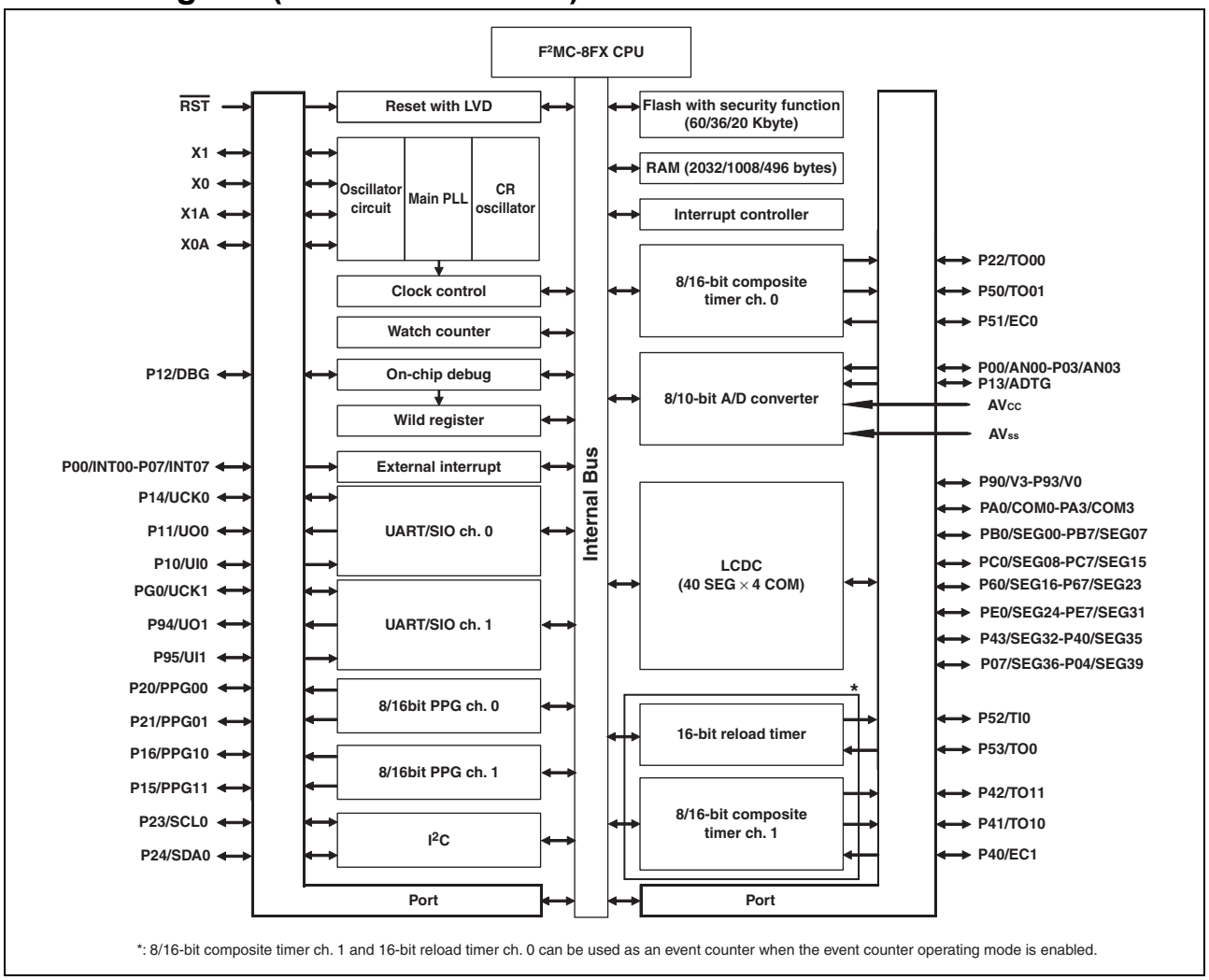
11. Recommended Layout

■ GND wire should be placed around X0, X1, X0A and X1A

The recommended layout method illustrated in following diagram aims to avoid noise coupled between the oscillator pins and GPIO, which may cause the main oscillator or the sub oscillator to malfunction.

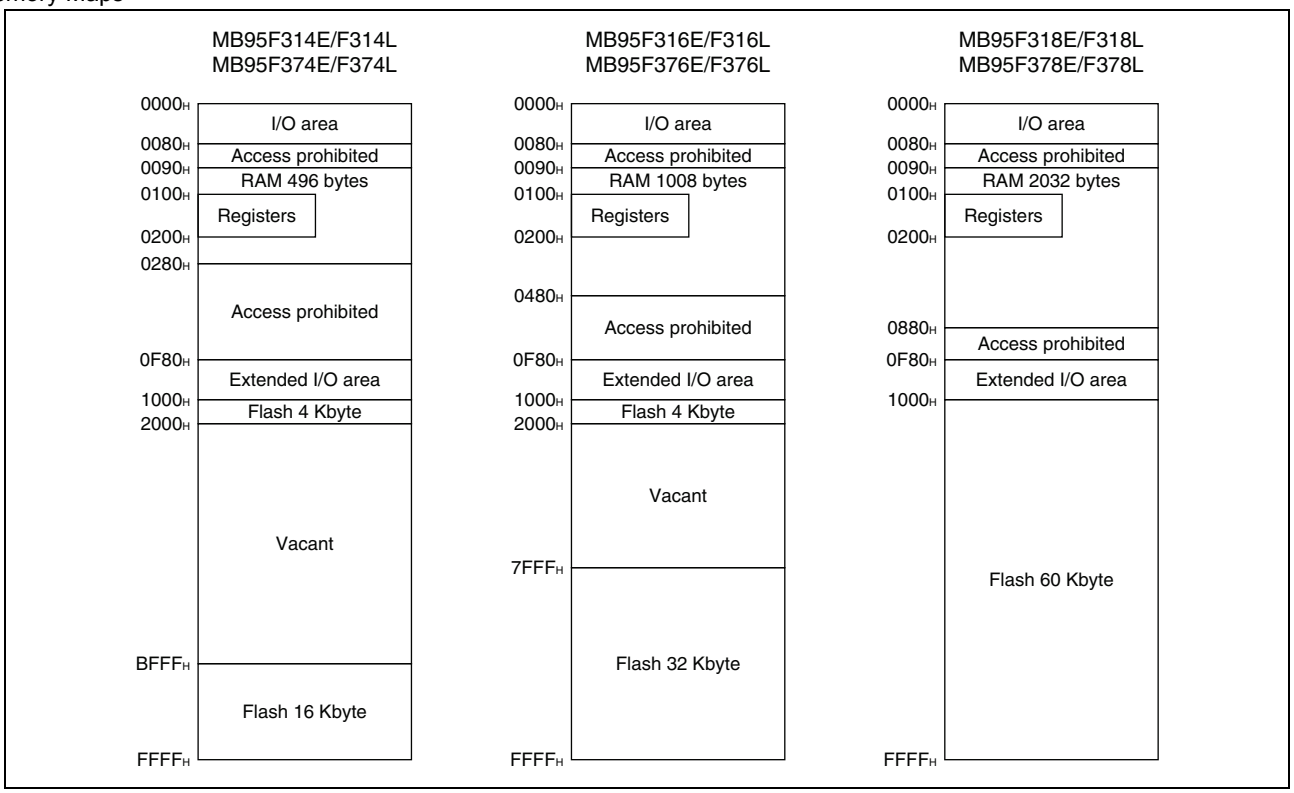


12. Block Diagram (MB95310L Series)



*: 8/16-bit composite timer ch. 1 and 16-bit reload timer ch. 0 can be used as an event counter when the event counter operating mode is enabled.

■ Memory Maps


MB95F314E/F314L
MB95F374E/F374L
0000H
I/O area
0080H
Access prohibited
0090H
RAM 496 bytes
0100H
Registers
0200H
0280H
Access prohibited
0F80H
Extended I/O area
1000H
Flash 4 Kbyte
2000H
Vacant
BFFFH
Flash 16 Kbyte
FFFFH
MB95F316E/F316L
MB95F376E/F376L
0000H
I/O area
0080H
Access prohibited
0090H
RAM 1008 bytes
0100H
Registers
0200H
0480H
Access prohibited
0F80H
Extended I/O area
1000H
Flash 4 Kbyte
2000H
Vacant
7FFFH
Flash 32 Kbyte
FFFFH
MB95F318E/F318L
MB95F378E/F378L
0000H
I/O area
0080H
Access prohibited
0090H
RAM 2032 bytes
0100H
Registers
0200H
0880H
Access prohibited
0F80H
Extended I/O area
1000H
Flash 60 Kbyte
FFFFH

15. I/O Map (MB95310L Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	PLLC	PLL control register	R/W	00000000_B
0007_H	SYCC	System clock control register	R/W	$XXXXXX11_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	$000XXXXX_B$
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	00000000_B
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$	PDR2	Port 2 data register	R/W	00000000_B
$000F_H$	DDR2	Port 2 direction register	R/W	00000000_B
0010_H, 0011_H	—	(Disabled)	—	—
0012_H	PDR4	Port 4 data register	R/W	00000000_B
0013_H	DDR4	Port 4 direction register	R/W	00000000_B
0014_H	PDR5	Port 5 data register	R/W	00000000_B
0015_H	DDR5	Port 5 direction register	R/W	00000000_B
0016_H	PDR6	Port 6 data register	R/W	00000000_B
0017_H	DDR6	Port 6 direction register	R/W	00000000_B
0018_H to $001B_H$	—	(Disabled)	—	—
$001C_H$	PDR9	Port 9 data register	R/W	00000000_B
$001D_H$	DDR9	Port 9 direction register	R/W	00000000_B
$001E_H$	PDRA	Port A data register	R/W	00000000_B
$001F_H$	DDRA	Port A direction register	R/W	00000000_B
0020_H	PDRB	Port B data register	R/W	00000000_B
0021_H	DDRB	Port B direction register	R/W	00000000_B
0022_H	PDRC	Port C data register	R/W	00000000_B
0023_H	DDRC	Port C direction register	R/W	00000000_B
0024_H, 0025_H	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0026_H	PDRE	Port E data register	R/W	00000000_B
0027_H	DDRE	Port E direction register	R/W	00000000_B
0028_H, 0029_H	—	(Disabled)	—	—
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$	PUL1	Port 1 pull-up register	R/W	00000000_B
$002E_H$	PUL2	Port 2 pull-up register	R/W	00000000_B
$002F_H$, 0030_H	—	(Disabled)	—	—
0031_H	PUL5	Port 5 pull-up register	R/W	00000000_B
0032_H, 0033_H	—	(Disabled)	—	—
0034_H	PUL9	Port 9 pull-up register	R/W	00000000_B
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	T11CR1	8/16-bit composite timer 11 status control register 1 ch. 1	R/W	00000000_B
0039_H	T10CR1	8/16-bit composite timer 10 status control register 1 ch. 1	R/W	00000000_B
$003A_H$	PC01	8/16-bit PPG01 control register ch. 0	R/W	00000000_B
$003B_H$	PC00	8/16-bit PPG00 control register ch. 0	R/W	00000000_B
$003C_H$	PC11	8/16-bit PPG11 control register ch. 1	R/W	00000000_B
$003D_H$	PC10	8/16-bit PPG10 control register ch. 1	R/W	00000000_B
$003E_H$	TMCSRH	16-bit reload timer control status register upper ch. 0	R/W	00000000_B
$003F_H$	TMCSRL	16-bit reload timer control status register lower ch. 0	R/W	00000000_B
0040_H to 0047_H	—	(Disabled)	—	—
0048_H	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000_B
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$, $004D_H$	—	(Disabled)	—	—
$004E_H$	LVDR	LVD reset voltage selection ID register	R/W	00000000_B
$004F_H$	LVDC	LVD control register	R/W	$X000000X_B$
0050_H to 0055_H	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000_B
$0F98_H$	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000_B
$0F99_H$	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000_B
$0F9A_H$	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000_B
$0F9B_H$	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000_B
$0F9C_H$	PPS01	8/16-bit PPG01 cycle setting buffer register ch. 0	R/W	11111111_B
$0F9D_H$	PPS00	8/16-bit PPG00 cycle setting buffer register ch. 0	R/W	11111111_B
$0F9E_H$	PDS01	8/16-bit PPG01 duty setting buffer register ch. 0	R/W	11111111_B
$0F9F_H$	PDS00	8/16-bit PPG00 duty setting buffer register ch. 0	R/W	11111111_B
$0FA0_H$	PPS11	8/16-bit PPG11 cycle setting buffer register ch. 1	R/W	11111111_B
$0FA1_H$	PPS10	8/16-bit PPG10 cycle setting buffer register ch. 1	R/W	11111111_B
$0FA2_H$	PDS11	8/16-bit PPG11 duty setting buffer register ch. 1	R/W	11111111_B
$0FA3_H$	PDS10	8/16-bit PPG10 duty setting buffer register ch. 1	R/W	11111111_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0060_H	IBCR00	I^2C bus control register 0	R/W	00000001_B
0061_H	IBCR10	I^2C bus control register 1	R/W	00000000_B
0062_H	IBCR0	I^2C bus status register	R	00000000_B
0063_H	IDDR0	I^2C data register	R/W	00000000_B
0064_H	IAAR0	I^2C address register	R/W	00000000_B
0065_H	ICCR0	I^2C clock control register	R/W	00000000_B
0066_H to $006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register upper	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register lower	R/W	00000000_B
0070_H	WCSR	Watch counter status register	R/W	00000000_B
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	00000000_B
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B

(Continued)

18.4 AC Characteristics

18.4.1 Clock Timing

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1.00	—	16.25	MHz	When the main oscillation circuit is used
				1.00	—	32.50	MHz	When the main external clock is used
				3.00	—	8.13	MHz	Main PLL multiplied by 2
				3.00	—	6.5	MHz	Main PLL multiplied by 2.5
				3.00	—	4.06	MHz	Main PLL multiplied by 4
	F_{CRH}	—		12.25	12.5	12.75	MHz	Operating conditions: • The main CR clock is used. • T_A = −10°C to +85°C
				9.8	10	10.2	MHz	
				7.84	8	8.16	MHz	
				0.98	1	1.02	MHz	
		—		12.1875	12.5	12.8125	MHz	Operating conditions: • The main CR clock is used. • T_A = −40°C to −10°C
				9.75	10	10.25	MHz	
				7.8	8	8.2	MHz	
				0.975	1	1.025	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	When the sub-oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—		50	100	200	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
				30.8	—	1000	ns	When the external clock is used
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1} t_{WL1}	X0	—	61.5	—	—	ns	When using external clock and the duty ratio is about 30% to 70%
	t_{WH2} t_{WL2}	X0A		—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0, X0A	X1: open	—	—	5	ns	When the external clock is used
CR oscillation start time	t_{CRHWK}	—	—	—	—	150	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	10	µs	When the sub-CR clock is used

18.4.2 Source Clock/Machine Clock

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main oscillation clock is used Min: F_{CH} = 8.125 MHz, multiplied by the PLL multiplier of 2 Max: F_{CH} = 1 MHz, divided by 2
			80	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 12.5 MHz Max: F_{CRH} = 1 MHz
			—	61	—	µs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.50	—	16.25	MHz	When the main oscillation clock is used
			1	—	12.5	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			80	—	16000	ns	When the main CR clock is used Min: F_{SP} = 12.5 MHz Max: F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.393 kHz, no division Max: F_{SPL} = 16.393 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	12.5	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

*1: This is the clock before it is divided according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1 and DIV0). This source clock is divided to become a machine clock according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1 and DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- PLL multiplication of main clock (select from 2, 2.5, 4 multiplication)
- Main CR clock divided by 2
- Subclock divided by 2
- Sub-CR clock divided by 2

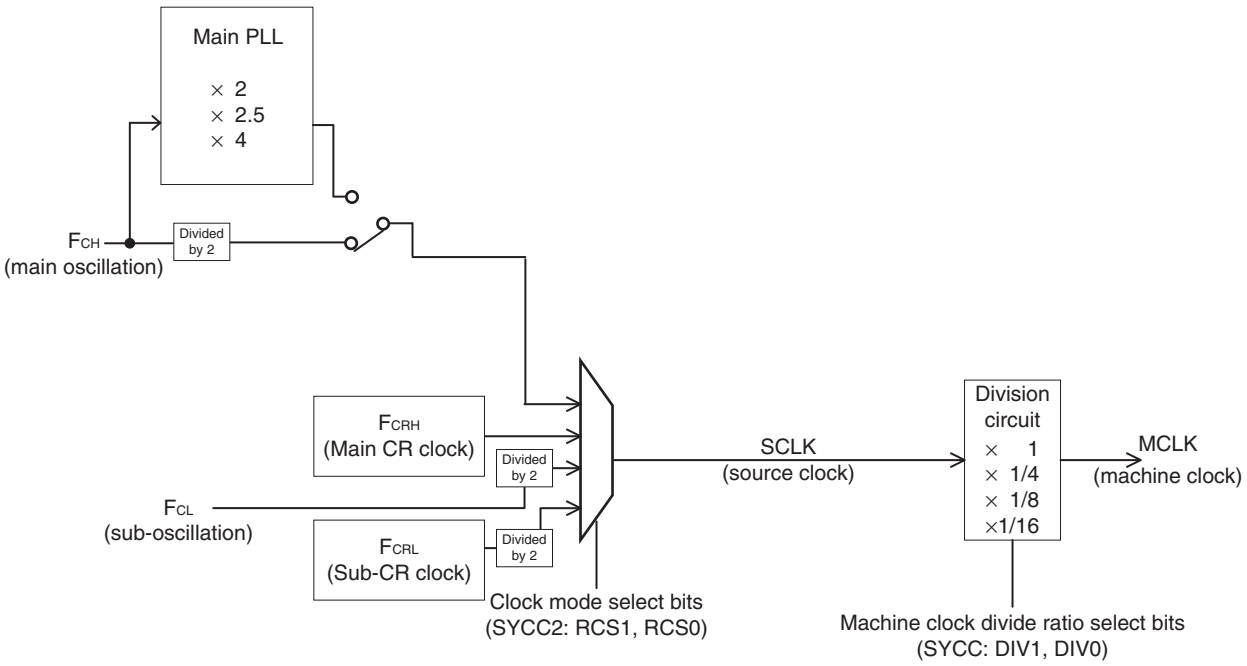
(Continued)

(Continued)

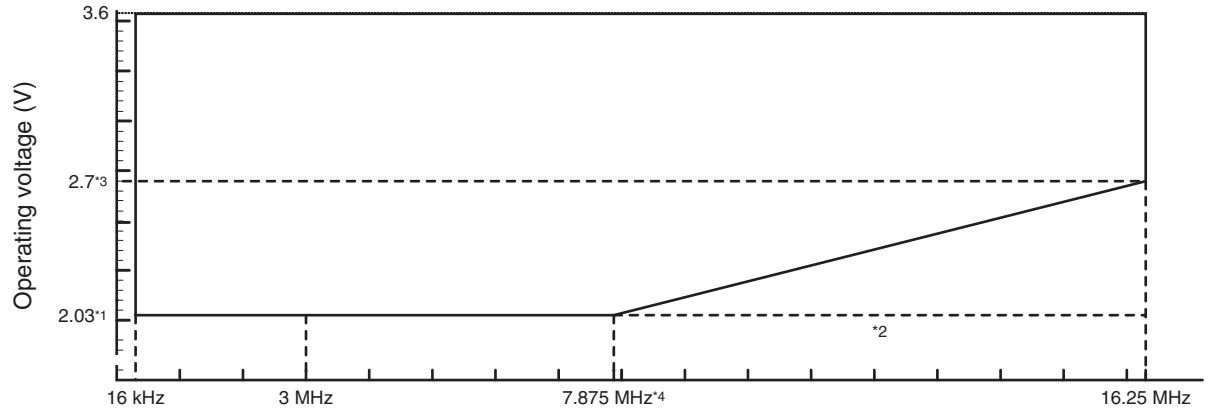
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

• Schematic diagram of the clock generation block



• Operating voltage - Operating frequency (When T_A = +5°C to +35°C)
With the on-chip debug function



*1: This is the default LVD reset clear threshold: 1.93 V ± 0.10 V. It can also be set to 2.40 V ± 0.15 V or 2.95 V ± 0.15 V.

*2: If the LVD reset clear threshold is set to 2.95 V ± 0.15 V, the slope from 10 MHz to 16.25 MHz should be a horizontal line.

*3: The operating voltage becomes 3.1 V if the LVD reset clear threshold is set to 2.95 V ± 0.15 V.

*4: The source clock frequency becomes 14.375 MHz if the LVD reset clear threshold is set to 2.40 V ± 0.15 V.

18.4.3 External Reset

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation
		Oscillation time of the oscillator*2 + 100	—	µs	In stop mode, subclock mode, subsleep mode, watch mode, and power-on
		100	—	µs	In time-base timer mode

*1: See "(2) Source Clock/Machine Clock" for t_{MCLK}.

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

18.4.8 I²C Timing

(V_{CC} = 3.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL0	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) Start condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL0, SDA0		4.0	—	0.6	—	µs
SCL clock "L" width	t_{LOW}	SCL0		4.7	—	1.3	—	µs
SCL clock "H" width	t_{HIGH}	SCL0		4.0	—	0.6	—	µs
(Repeat) Start condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL0, SDA0		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HD;DAT}$	SCL0, SDA0		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SU;DAT}$	SCL0, SDA0		0.25	—	0.1	—	µs
Stop condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL0, SDA0		4.0	—	0.6	—	µs
Bus free time between stop condition and start condition	t_{BUF}	SCL0, SDA0		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL0 and SDA0 lines, and C the load capacitor of the SCL0 and SDA0 lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at "L" (t_{LOW}) does not extend.

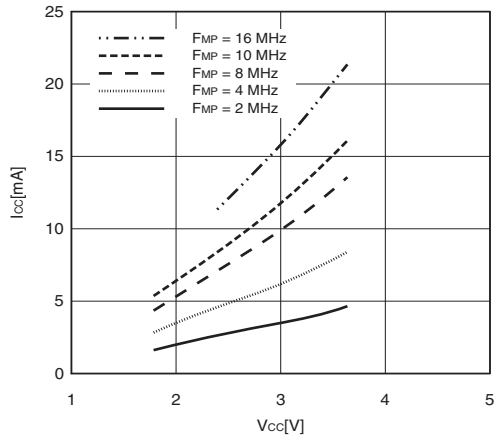
*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of $t_{SU;DAT} \geq 250$ ns is fulfilled.

(Continued)

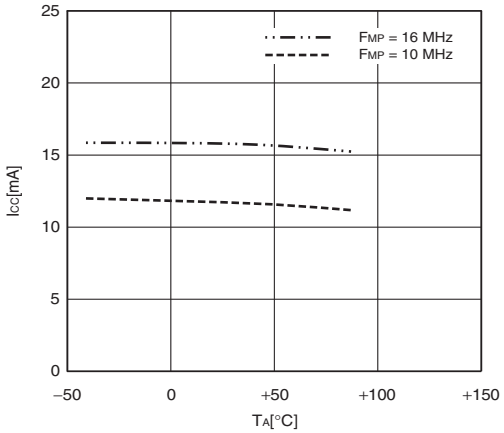
19. Sample Characteristics

- Power supply current temperature characteristics

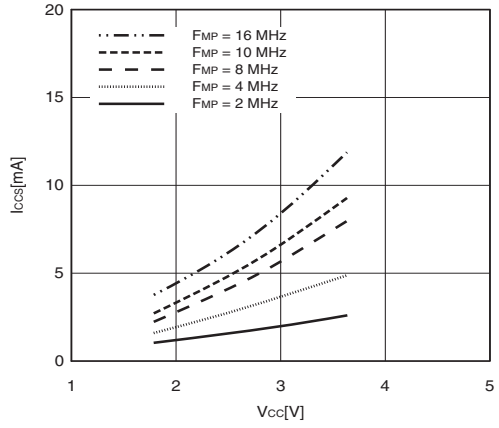
$I_{CC} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



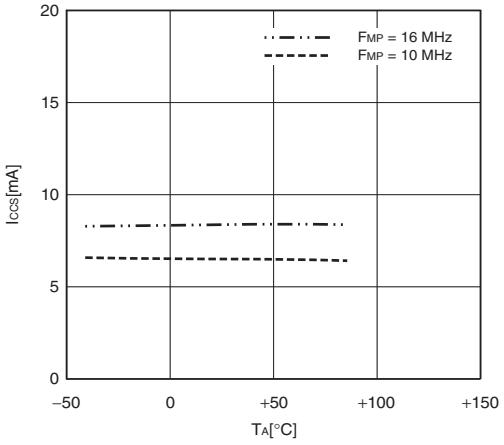
$I_{CC} - T_A$
V_{CC} = 3.0 V, F_{MP} = 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



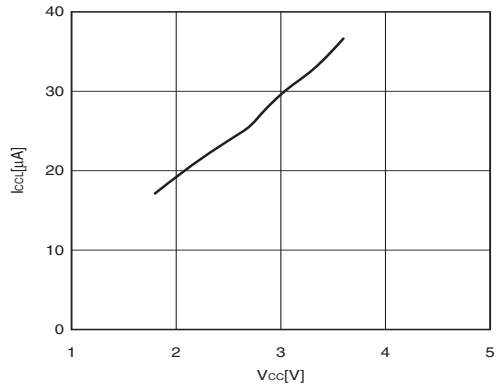
$I_{CCS} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



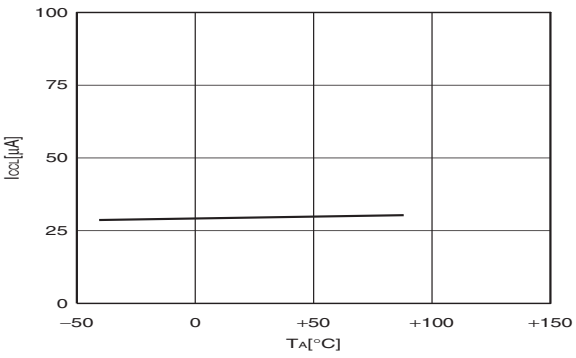
$I_{CCS} - T_A$
V_{CC} = 3.0 V, F_{MP} = 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



$I_{CCL} - V_{CC}$
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



ICCL —TA
VCC = 3.0 V, FMPL = 16 kHz (divided by 2)
Subclock mode with the external clock operating



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

cypress.com/psoc

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/support