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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D - 16bit; D/A - 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl26z32vft4

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{IH}	Input high voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	— —	V V	
V_{IL}	Input low voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	— —	$0.35 \times V_{DD}$ $0.3 \times V_{DD}$	V V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin <ul style="list-style-type: none"> $V_{IN} < V_{SS}-0.3\text{V}$ 	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins <ul style="list-style-type: none"> Negative current injection 	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

- All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} ($= V_{SS}-0.3\text{ V}$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|$.
- Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements

Table 6. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—

Table continues on the next page...

Table 7. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V _{OL}	Output low voltage — Normal drive pad <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA 	—	0.5	V	1
		—	0.5	V	
V _{OL}	Output low voltage — High drive pad <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA 	—	0.5	V	1
		—	0.5	V	
I _{OLT}	Output low current total for all ports	—	100	mA	
I _{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	3
I _{IN}	Input leakage current (per pin) at 25 °C	—	0.025	μA	3
I _{IN}	Input leakage current (total all pins) for full temperature range	—	65	μA	3
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R _{PU}	Internal pullup resistors	20	50	kΩ	4

1. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at V_{DD} = 3.6 V
4. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx→RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V _{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	1

Table continues on the next page...

Table 8. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• VLLS0 → RUN	—	106	120	μs	
	• VLLS1 → RUN	—	105	117	μs	
	• VLLS3 → RUN	—	47	54	μs	
	• LLS → RUN	—	4.5	5.0	μs	
	• VLPS → RUN	—	4.5	5.0	μs	
	• STOP → RUN	—	4.5	5.0	μs	

1. Normal boot (FTFA_FOFT[LPBOOT]=11).

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 9. Power consumption operating behaviors

Symbol	Description	Temp.	Typ.	Max	Unit	Note
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUNCO_CM}	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus disabled, LPTMR running using 4 MHz internal reference clock, CoreMark® benchmark code executing from flash, at 3.0 V	—	6.1	—	mA	2
I _{DD_RUNCO}	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash, at 3.0 V	—	3.8	4.4	mA	3
I _{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code executing from flash, at 3.0 V	—	4.6	5.2	mA	3

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Temp.	Typ.	Max	Unit	Note
I _{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 3.0 V	at 25 °C	6.0	6.2	mA	3, 4
		at 70 °C	6.2	6.4	mA	
		at 125 °C	6.2	6.5	mA	
I _{DD_WAIT}	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled, at 3.0 V	—	2.7	3.2	mA	3
I _{DD_WAIT}	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled, at 3.0 V	—	2.1	2.6	mA	3
I _{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus, at 3.0 V	—	1.5	2.0	mA	3
I _{DD_VLPRCO_CM}	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, LPTMR running with 4 MHz internal reference clock, CoreMark benchmark code executing from flash, at 3.0 V	—	732	—	μA	5
I _{DD_VLPRCO}	Very low power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code executing from flash, at 3.0 V	—	161	329	μA	6
I _{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code executing from flash, at 3.0 V	—	185	352	μA	6
I _{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 3.0 V	—	255	421	μA	4, 6
I _{DD_VLPW}	Very low power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled, at 3.0 V	—	110	281	μA	6
I _{DD_STOP}	Stop mode current at 3.0 V	at 25 °C	305	326	μA	—
		at 50 °C	317	344	μA	
		at 70 °C	337	380	μA	
		at 85 °C	364	428	μA	
		at 105 °C	429	553	μA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V	at 25 °C	2.69	4.14	μA	—
		at 50 °C	5.54	9.80	μA	
		at 70 °C	11.80	21.94	μA	

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit	
		-40	25	50	70	85	105		
I _{IREFSTEN4MHz}	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA	
I _{IREFSTEN32KHz}	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA	
I _{EREFSTEN4MHz}	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	μA	
I _{EREFSTEN32KHz}	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	VLLS1	440	490	540	560	570	580	nA
		VLLS3	440	490	540	560	570	580	
		LLS	490	490	540	560	570	680	
		VLPS	510	560	560	560	610	680	
		STOP	510	560	560	560	610	680	
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA	
I _{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA	
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
		OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I _{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	86	μA
		OSCERCLK (4 MHz external crystal)	235	256	265	274	280	287	

Table continues on the next page...

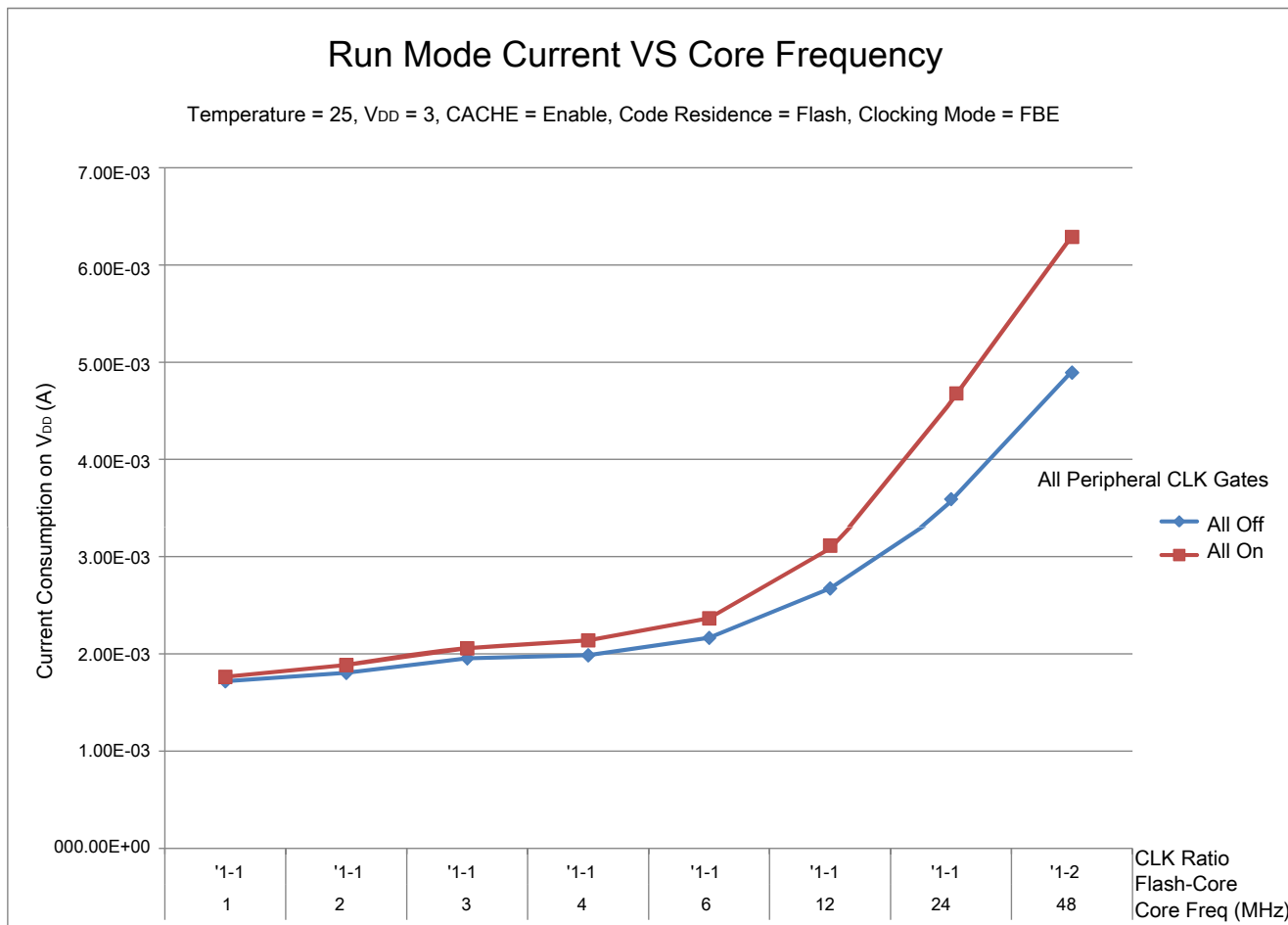


Figure 2. Run mode supply current vs. core frequency

General

application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $f_{OSC} = 8\text{ MHz}$ (crystal), $f_{SYS} = 48\text{ MHz}$, $f_{BUS} = 24\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 12. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes ¹				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock ²	—	24	MHz

Table continues on the next page...

Table 13. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit
f _{ERCLK}	External reference clock	—	16	MHz
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz
f _{TPM}	TPM asynchronous clock	—	8	MHz
f _{UART0}	UART0 asynchronous clock	—	8	MHz

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 14. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T _J	Die junction temperature	−40	125	°C
T _A	Ambient temperature	−40	105	°C

3.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
$t_{nmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nmcyccp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 25](#) and [Table 26](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.6.1.1 16-bit ADC operating conditions

Table 25. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	3

Table continues on the next page...

Table 25. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{ADIN}	Input voltage	<ul style="list-style-type: none"> 16-bit differential mode All other modes 	VREFL	—	31/32 * VREFH	V	—
C _{ADIN}	Input capacitance	<ul style="list-style-type: none"> 16-bit mode 8-bit / 10-bit / 12-bit modes 	—	8	10	pF	—
R _{ADIN}	Input series resistance		—	2	5	kΩ	—
R _{AS}	Analog source resistance (external)	13-bit / 12-bit modes f _{ADCK} < 4 MHz	—	—	5	kΩ	4
f _{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	5
f _{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	5
C _{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	6
C _{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	6

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated VREFH and VREFL pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SSA}.
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
5. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
6. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

Peripheral operating requirements and behaviors

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0\text{ V}$, $\text{Temp} = 25\text{ }^{\circ}\text{C}$, $f_{ADCK} = 2.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. $1\text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

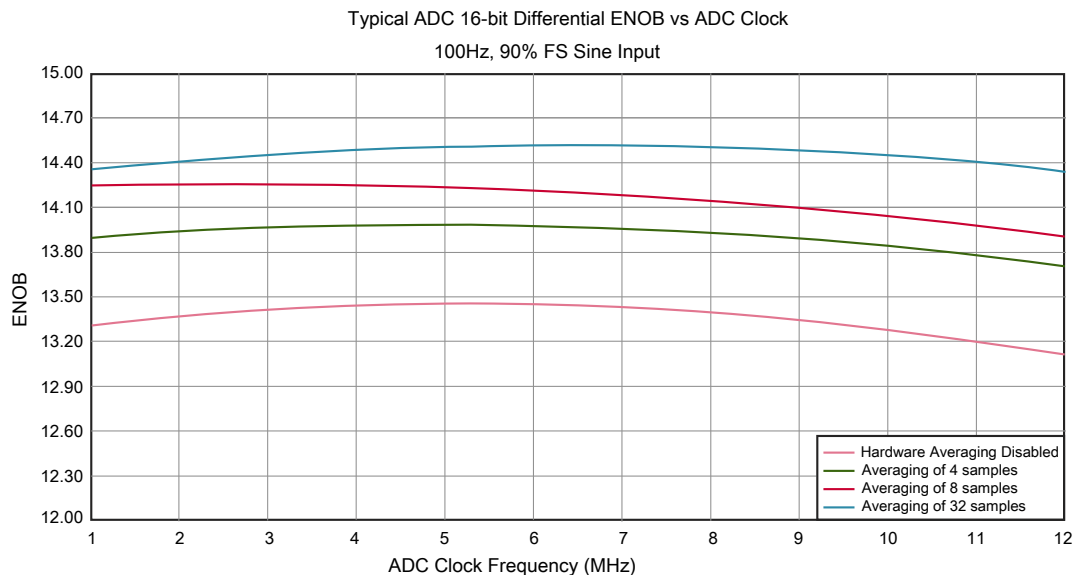


Figure 7. Typical ENOB vs. ADC_CLK for 16-bit differential mode

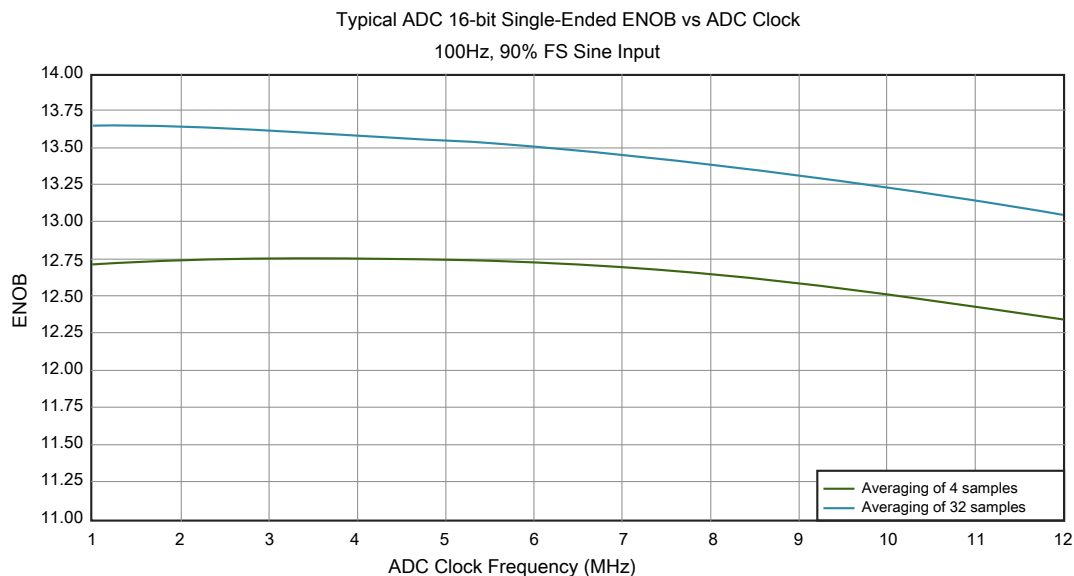


Figure 8. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

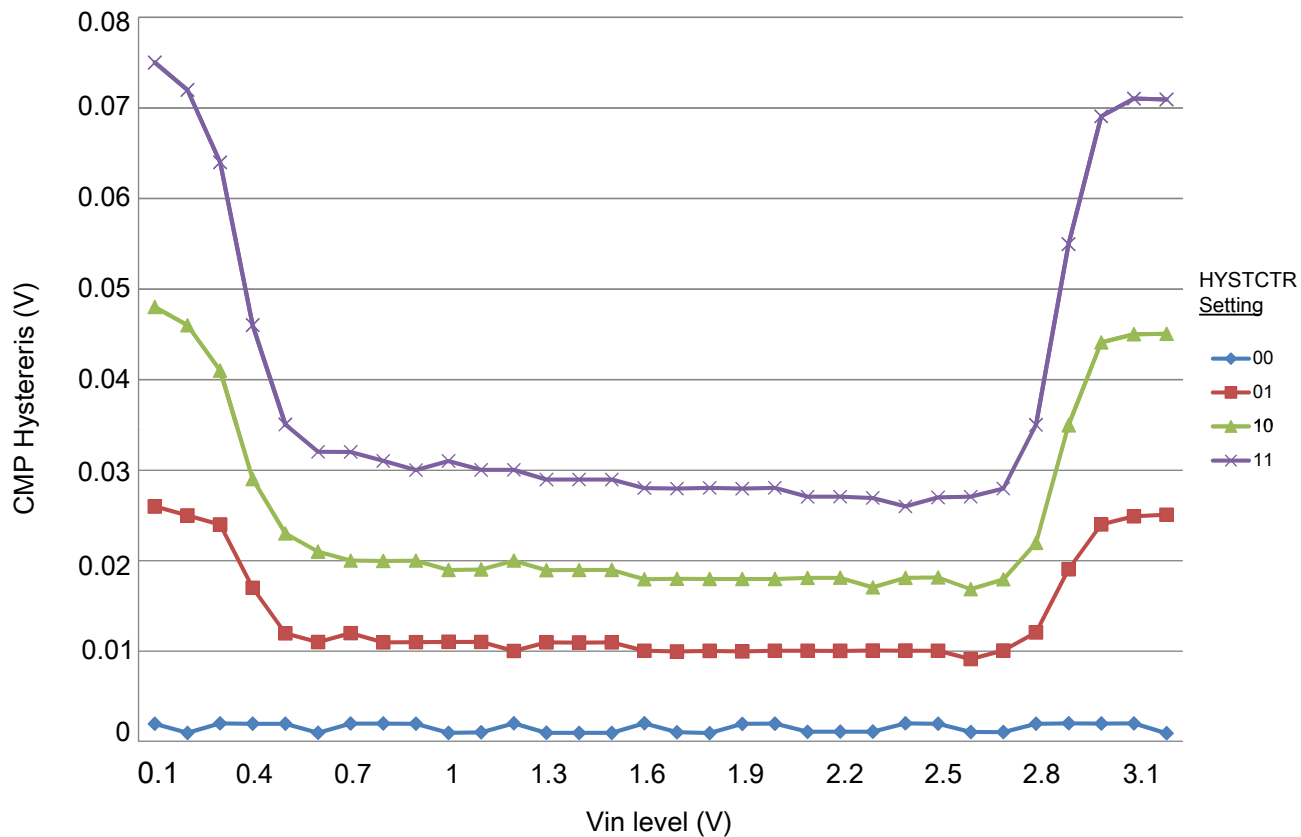


Figure 9. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

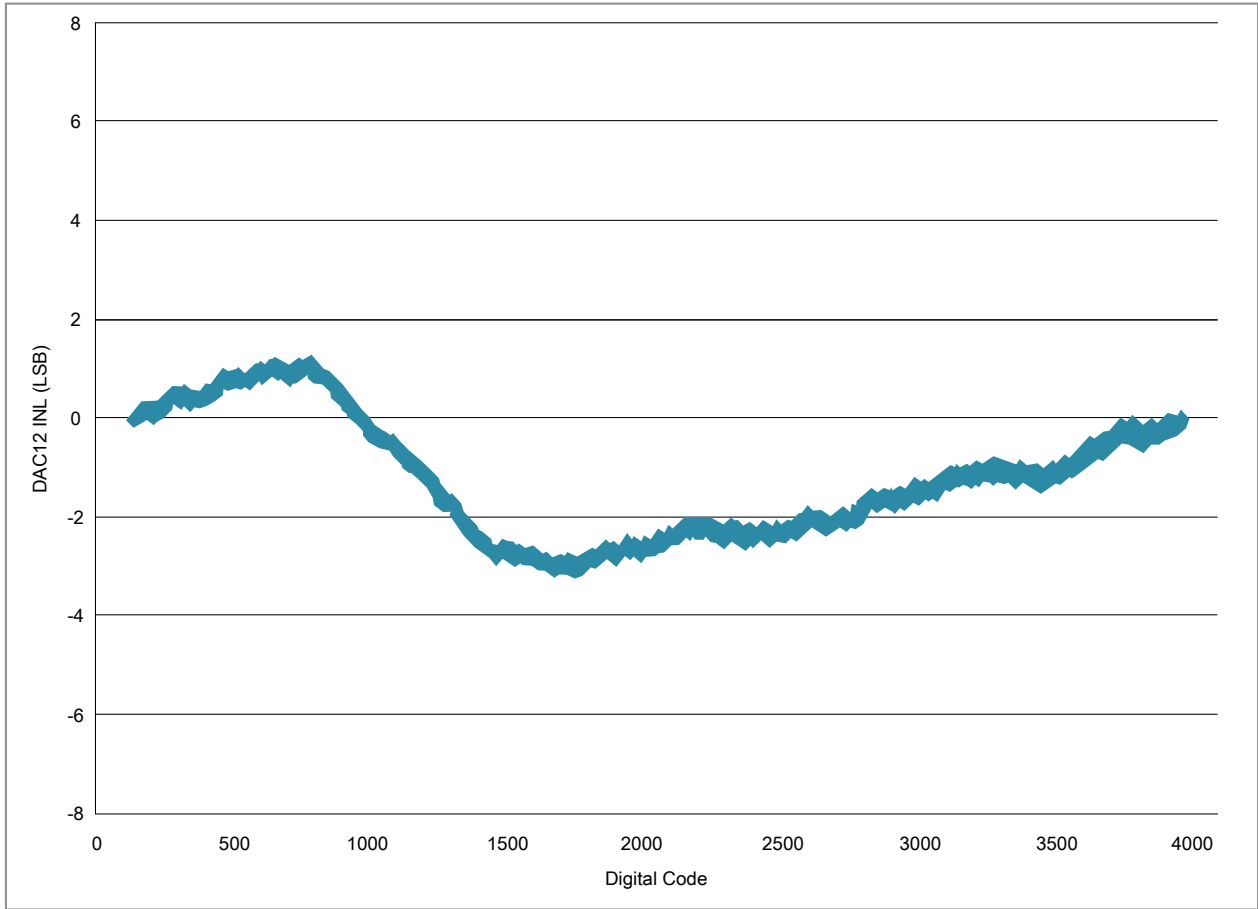


Figure 11. Typical INL error vs. digital code

2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t_{HD; DAT} must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU; DAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

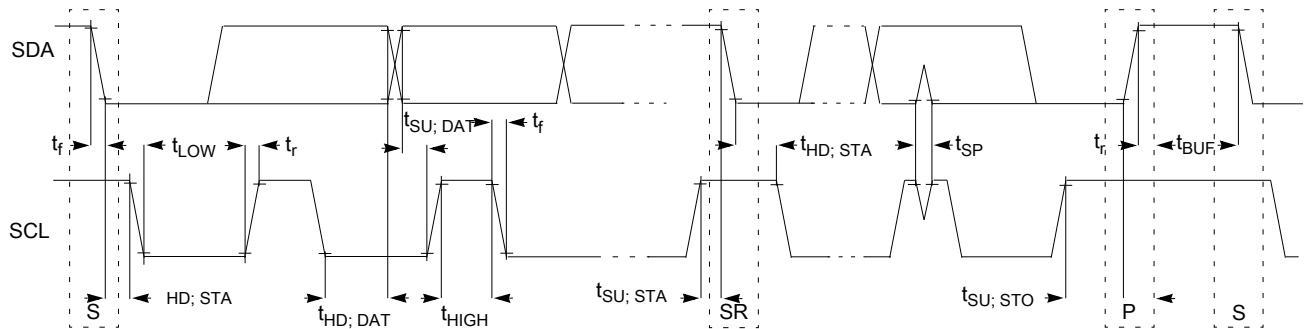


Figure 17. Timing definition for fast and standard mode devices on the I²C bus

3.8.5 UART

See [General switching specifications](#).

3.8.6 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
62	46	30	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5			
63	47	31	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	UART0_RX		SPI1_MISO		
64	48	32	PTD7	DISABLED		PTD7	SPI1_MISO	UART0_TX		SPI1_MOSI		

5.2 KL26 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see [KL26 Signal Multiplexing and Pin Assignments](#).

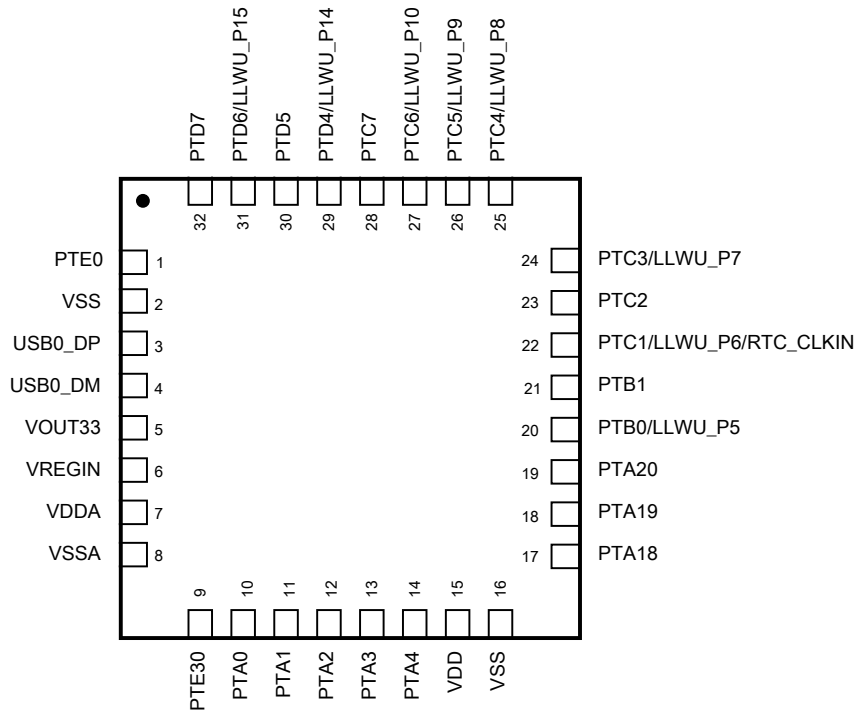


Figure 24. KL26 32-pin QFN pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PKL26 and MKL26

7 Part identification

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

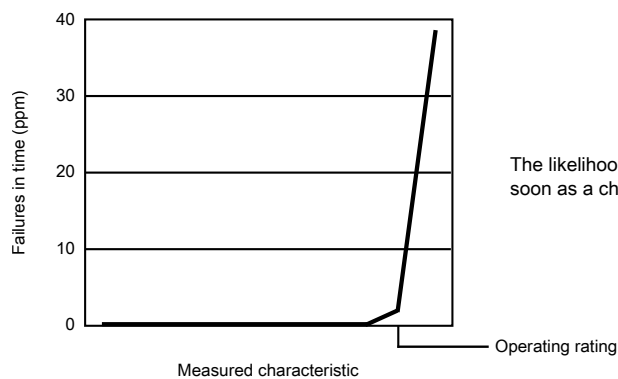
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

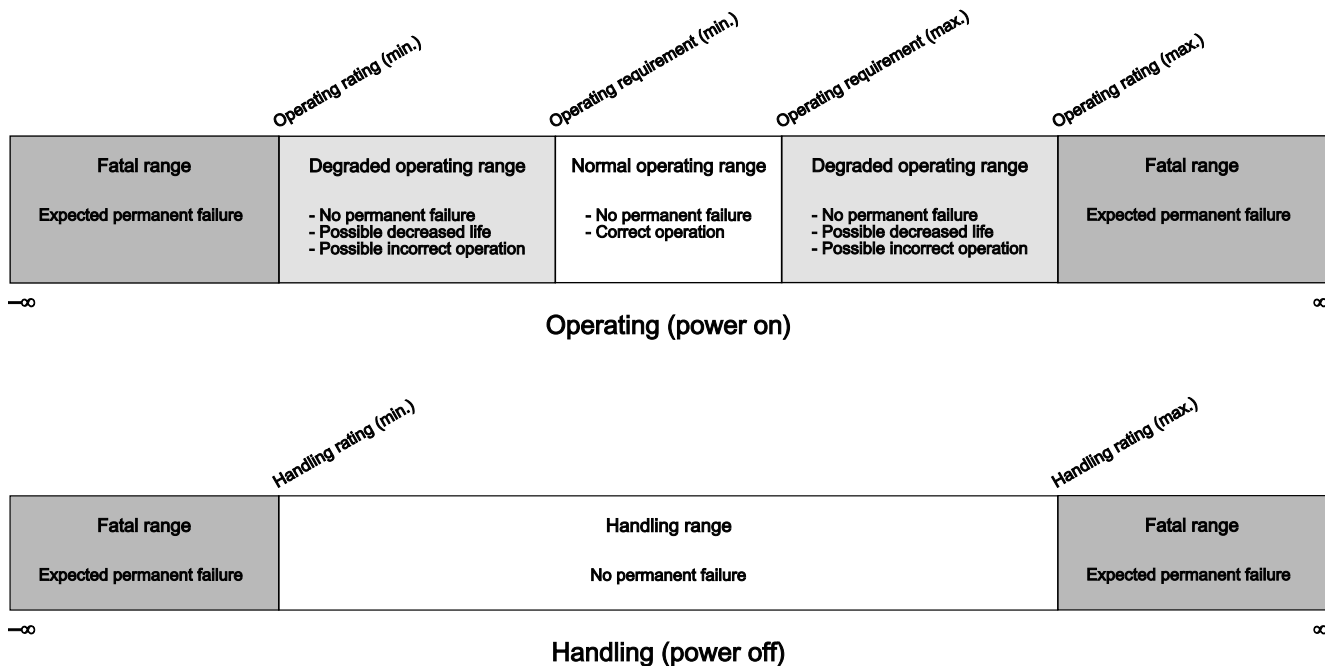
Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	-0.3	1.2	V

8.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

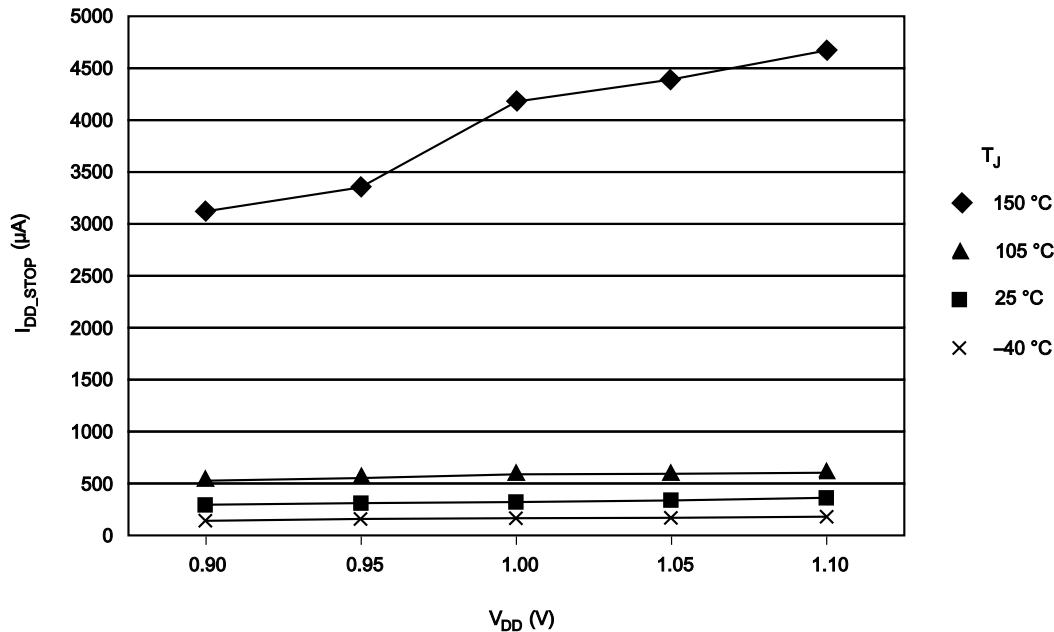
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 41. Typical value conditions

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	°C
V _{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 42. Revision history

Rev. No.	Date	Substantial Changes
3	3/2014	<ul style="list-style-type: none"> Updated the front page and restructured the chapters
4	5/2014	<ul style="list-style-type: none"> Updated Power consumption operating behaviors Updated USB electrical specifications Updated Definition: Operating behavior
5	08/2014	<ul style="list-style-type: none"> Updated related source in the front page Updated Power consumption operating behaviors Updated the note in USB electrical specifications