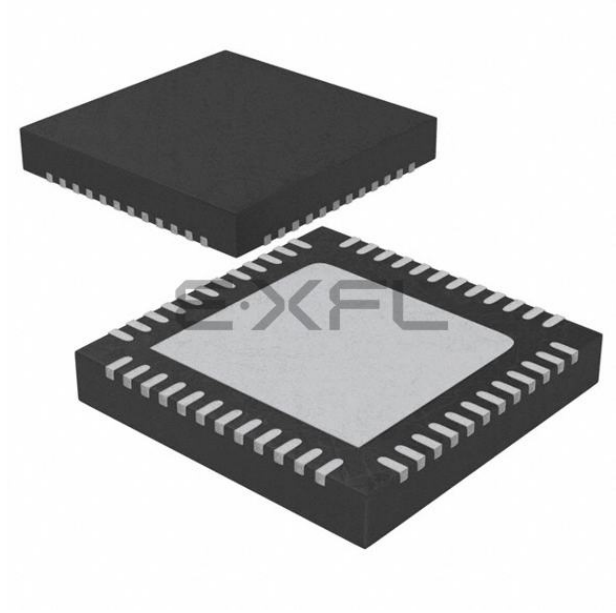

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART, USB, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 36 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D - 16bit; D/A - 12bit |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-VFQFN Exposed Pad |
| Supplier Device Package | 48-QFN (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl26z64vft4 |

# 1 Ratings

## 1.1 Thermal handling ratings

**Table 1. Thermal handling ratings**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

**Table 2. Moisture handling ratings**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

**Table 3. ESD handling ratings**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | –2000 | +2000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | –500 | +500 | V | 2 |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105 °C | –100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

**Table 6. $V_{DD}$ supply LVD and POR operating requirements (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{LVDH}$ | Falling low-voltage detect threshold — high range (LVDV = 01) | 2.48 | 2.56 | 2.64 | V | — |
| | Low-voltage warning thresholds — high range | | | | | 1 |
| $V_{LVW1H}$ | • Level 1 falling (LVWV = 00) | 2.62 | 2.70 | 2.78 | V | |
| $V_{LVW2H}$ | • Level 2 falling (LVWV = 01) | 2.72 | 2.80 | 2.88 | V | |
| $V_{LVW3H}$ | • Level 3 falling (LVWV = 10) | 2.82 | 2.90 | 2.98 | V | |
| $V_{LVW4H}$ | • Level 4 falling (LVWV = 11) | 2.92 | 3.00 | 3.08 | V | |
| $V_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | ±60 | — | mV | — |
| $V_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | — |
| | Low-voltage warning thresholds — low range | | | | | 1 |
| $V_{LVW1L}$ | • Level 1 falling (LVWV = 00) | 1.74 | 1.80 | 1.86 | V | |
| $V_{LVW2L}$ | • Level 2 falling (LVWV = 01) | 1.84 | 1.90 | 1.96 | V | |
| $V_{LVW3L}$ | • Level 3 falling (LVWV = 10) | 1.94 | 2.00 | 2.06 | V | |
| $V_{LVW4L}$ | • Level 4 falling (LVWV = 11) | 2.04 | 2.10 | 2.16 | V | |
| $V_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | ±40 | — | mV | — |
| $V_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | — |
| $t_{LPO}$ | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | — |

1. Rising thresholds are falling threshold + hysteresis voltage

## 2.2.3 Voltage and current operating behaviors

**Table 7. Voltage and current operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage — Normal drive pad (except RESET_b) | | | | 1, 2 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -5 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -2.5 mA | $V_{DD}$ – 0.5 | — | V | |
| $V_{OH}$ | Output high voltage — High drive pad (except RESET_b) | | | | 1, 2 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -20 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -10 mA | $V_{DD}$ – 0.5 | — | V | |
| $I_{OHT}$ | Output high current total for all ports | — | 100 | mA | |

*Table continues on the next page...*

**Table 10. Low power mode peripheral adders — typical value (continued)**

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| $I_{BG}$ | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode. | 45 | 45 | 45 | 45 | 45 | 45 | µA |
| $I_{ADC}$ | ADC peripheral adder combining the measured values at $V_{DD}$ and $V_{DDA}$ by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 366 | 366 | 366 | 366 | 366 | 366 | µA |

### 2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. $V_{DD}$ = 3.3 V, $T_A$ = 25 °C, $f_{OSC}$ = 8 MHz (crystal), $f_{SYS}$ = 48 MHz, $f_{BUS}$ = 24 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

### 2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

### 2.2.8 Capacitance attributes

**Table 12. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | — | 7 | pF |

## 2.3 Switching specifications

### 2.3.1 Device clock specifications

**Table 13. Device clock specifications**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| Normal run mode | | | | |
| $f_{SYS}$ | System and core clock | — | 48 | MHz |
| $f_{BUS}$ | Bus clock | — | 24 | MHz |
| $f_{FLASH}$ | Flash clock | — | 24 | MHz |
| $f_{SYS\_USB}$ | System and core clock when Full Speed USB in operation | 20 | — | MHz |
| $f_{LPTMR}$ | LPTMR clock | — | 24 | MHz |
| VLPR and VLPS modes[1] | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz |
| $f_{BUS}$ | Bus clock | — | 1 | MHz |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz |
| $f_{LPTMR}$ | LPTMR clock[2] | — | 24 | MHz |

*Table continues on the next page...*

### 2.4.2 Thermal attributes

**Table 16. Thermal attributes**

| Board type | Symbol | Description | 64 LQFP | 48 QFN | 32 QFN | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Single-layer (1S) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 71 | 83 | 98 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 53 | 30 | 34 | °C/W | |
| Single-layer (1S) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 59 | 68 | 82 | °C/W | |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 46 | 24 | 28 | °C/W | |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 35 | 12 | 13 | °C/W | 2 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 21 | 2.3 | 2.3 | °C/W | 3 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 6 | 5 | 8 | °C/W | 4 |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

# 3 Peripheral operating requirements and behaviors

## 3.1 Core modules

## Table 19. Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | • 24 MHz<br>• 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high gain mode (HGO=1) | | | | | 1 |
| | • 32 kHz | — | 25 | — | µA | |
| | • 4 MHz | — | 400 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 500 | — | µA | |
| | • 16 MHz | — | 2.5 | — | mA | |
| | • 24 MHz | — | 3 | — | mA | |
| | • 32 MHz | — | 4 | — | mA | |
| $C_x$ | EXTAL load capacitance | — | — | — | | 2, 3 |
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | kΩ | |
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation

3. $C_x$,$C_y$ can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 3.3.2.2 Oscillator frequency specifications

**Table 20. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 48 | MHz | 1, 2 |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

## 3.4 Memories and memory interfaces

### 3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

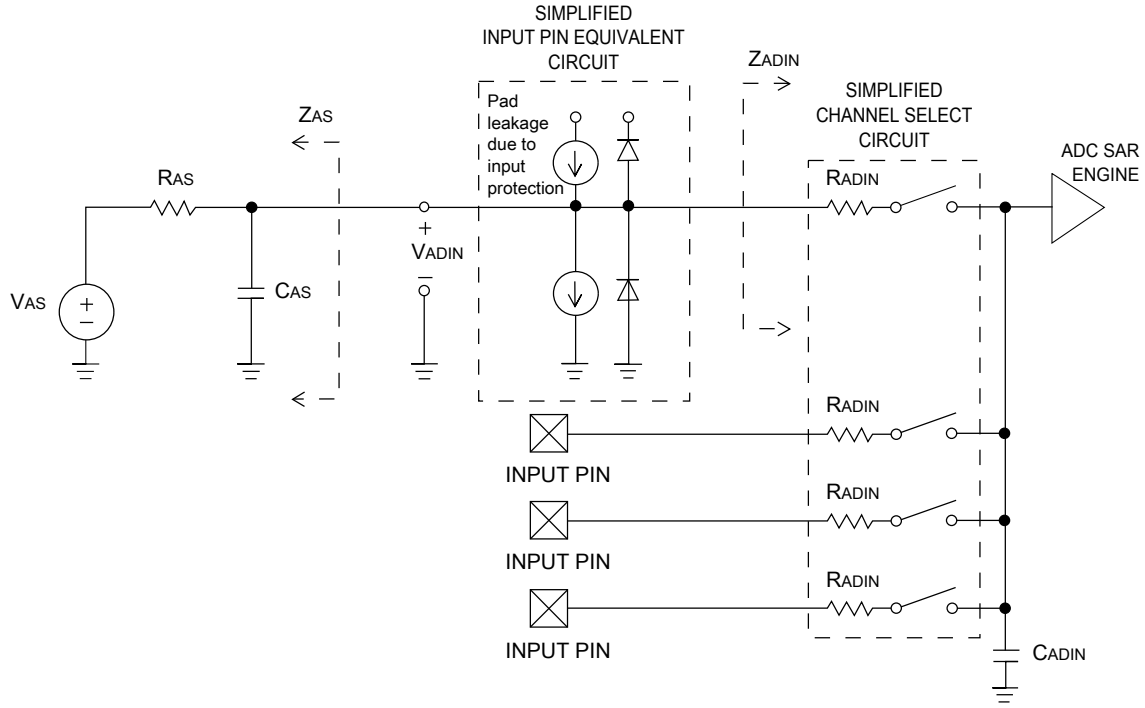



**Figure 6. ADC input impedance equivalency diagram**

## 3.6.1.2 16-bit ADC electrical characteristics

**Table 26. 16-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$)**

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $I_{DDA\_ADC}$ | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| $f_{ADACK}$ | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0<br>• ADLPC = 1, ADHSC = 1<br>• ADLPC = 0, ADHSC = 0<br>• ADLPC = 0, ADHSC = 1 | 1.2<br>2.4<br>3.0<br>4.4 | 2.4<br>4.0<br>5.2<br>6.2 | 3.9<br>6.1<br>7.3<br>9.5 | MHz<br>MHz<br>MHz<br>MHz | $t_{ADACK}$ = $1/f_{ADACK}$ |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12-bit modes<br>• <12-bit modes | —<br>— | ±4<br>±1.4 | ±6.8<br>±2.1 | LSB[4] | 5 |
| DNL | Differential non-linearity | • 12-bit modes<br>• <12-bit modes | —<br>— | ±0.7<br>±0.2 | –1.1 to +1.9<br>–0.3 to 0.5 | LSB[4] | 5 |

*Table continues on the next page...*

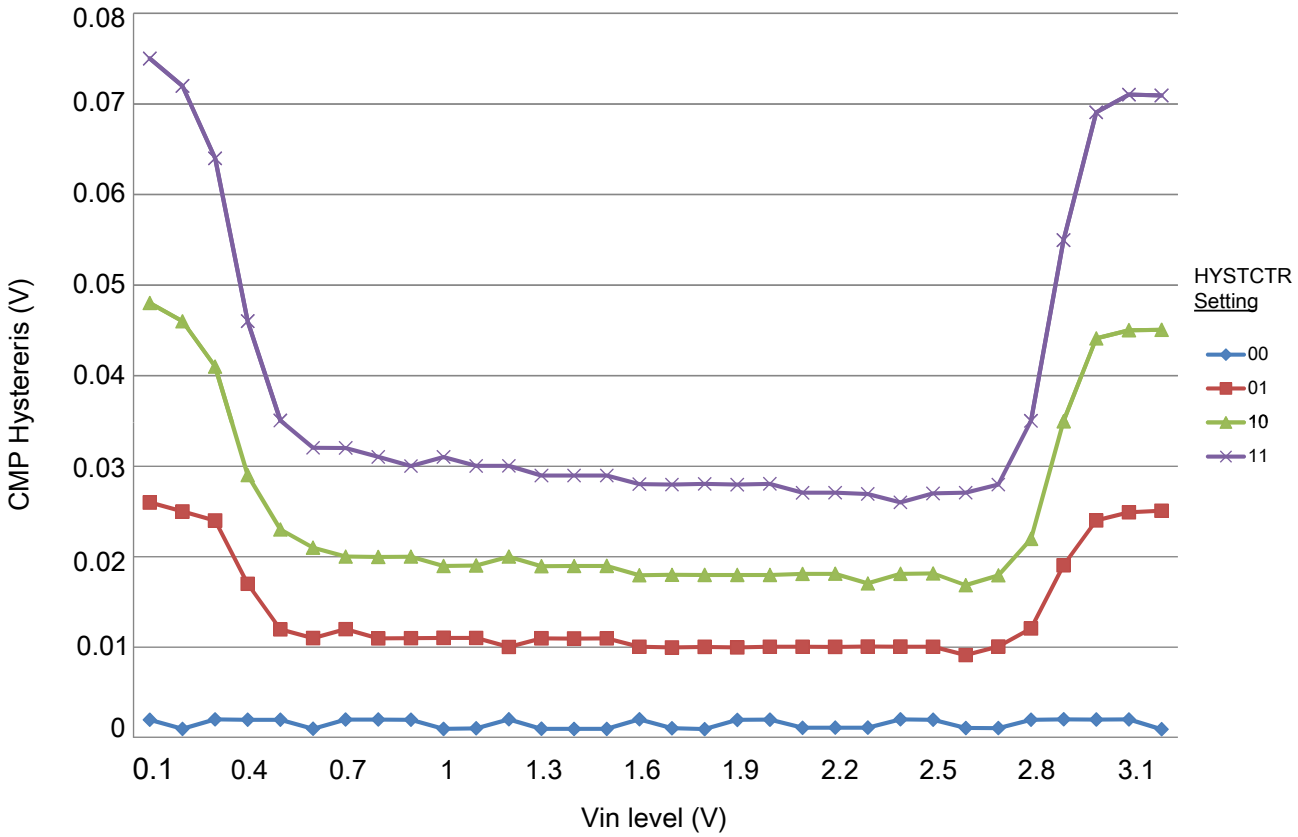



**Figure 9. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)**

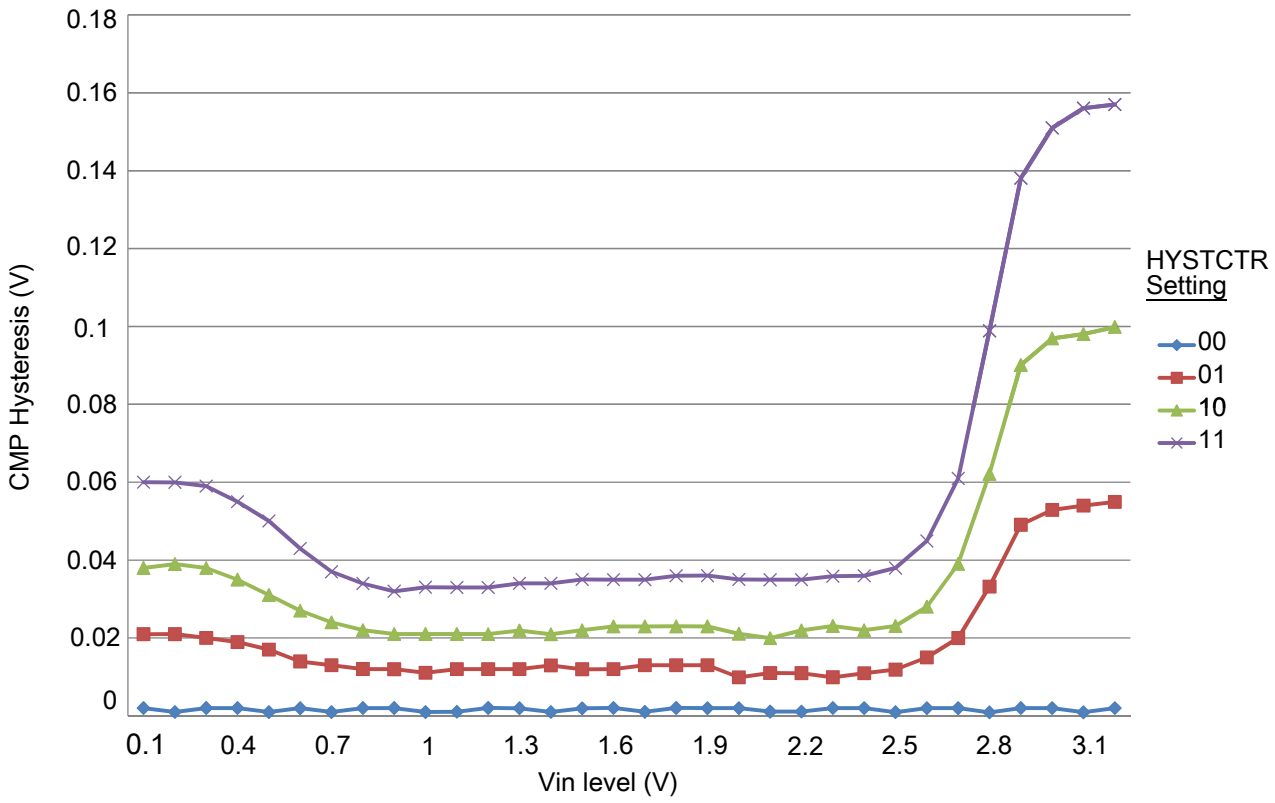



**Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)**

## 3.6.3 12-bit DAC electrical characteristics

### 3.6.3.1 12-bit DAC operating requirements

**Table 28. 12-bit DAC operating requirements**

| Symbol | Desciption | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DACR}$ | Reference voltage | 1.13 | 3.6 | V | 1 |
| $C_L$ | Output load capacitance | — | 100 | pF | 2 |
| $I_L$ | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be $V_{DDA}$ or VREFH.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

### 3.8.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$ thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

**Table 31. SPI master mode timing on slew rate disabled pads**

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{periph}$ | 2048 x $t_{periph}$ | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | 1024 x $t_{periph}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 18 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_{v}$ | Data valid (after SPSCK edge) | — | 15 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 10 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 11 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0 $f_{periph}$ is the bus clock ($f_{BUS}$). For SPI1 $f_{periph}$ is the system clock ($f_{SYS}$).
2. $t_{periph} = 1/f_{periph}$

**Table 32. SPI master mode timing on slew rate enabled pads**

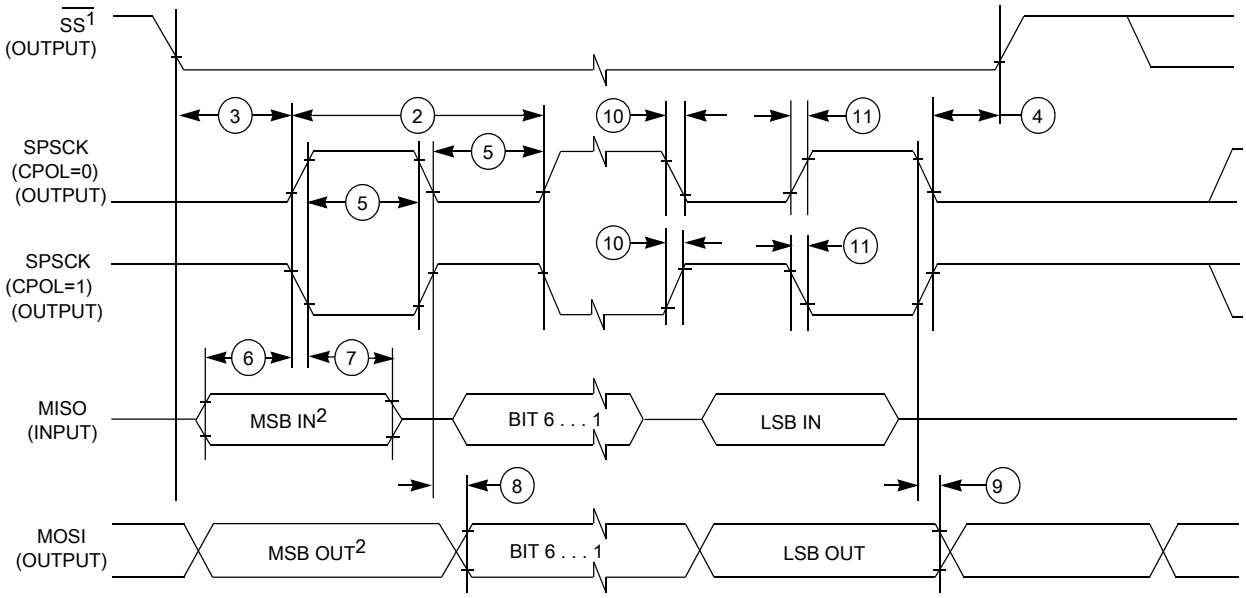
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{periph}$ | 2048 x $t_{periph}$ | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | 1024 x $t_{periph}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 96 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |

*Table continues on the next page...*

**Table 32. SPI master mode timing on slew rate enabled pads (continued)**

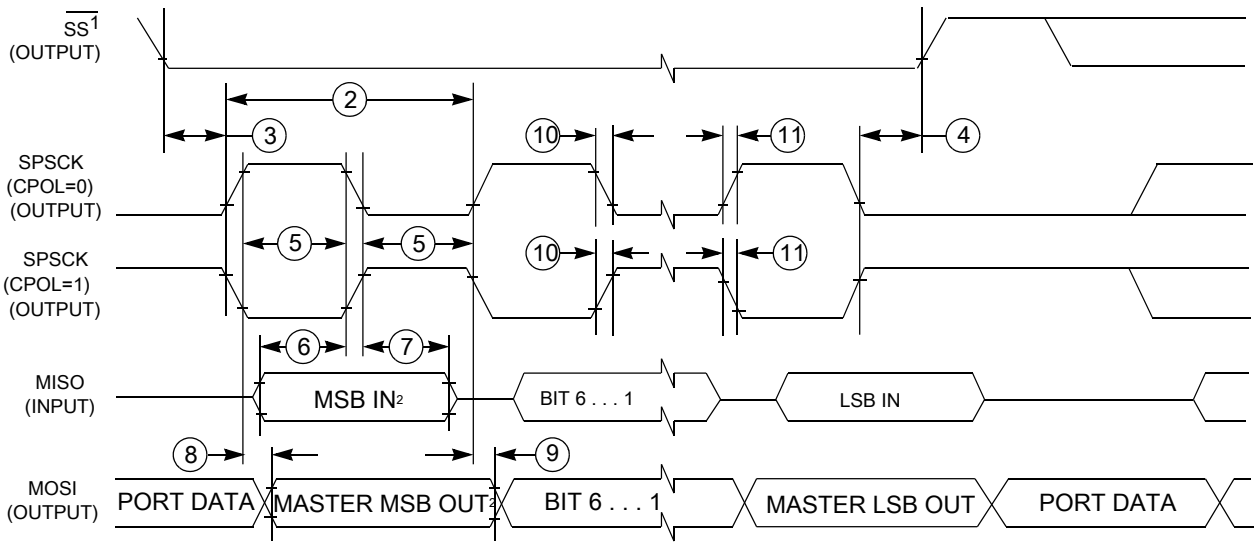
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 8 | $t_v$ | Data valid (after SPSCK edge) | — | 52 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 10 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 11 | $t_{RO}$ | Rise time output | — | 36 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0 $f_{periph}$ is the bus clock ($f_{BUS}$). For SPI1 $f_{periph}$ is the system clock ($f_{SYS}$).
2. $t_{periph} = 1/f_{periph}$




1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 13. SPI master mode timing (CPHA = 0)**




1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 14. SPI master mode timing (CPHA = 1)**

## Table 33. SPI slave mode timing on slew rate disabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{periph}$ | — | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{periph}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{periph}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 2.5 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 3.5 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{periph}$ | ns | 3 |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{periph}$ | ns | 4 |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 31 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0 $f_{periph}$ is the bus clock ($f_{BUS}$). For SPI1 $f_{periph}$ is the system clock ($f_{SYS}$).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

2. The master mode $I^2C$ deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode $I^2C$ bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode $I^2C$ bus specification) before the SCL line is released.
7. $C_b$ = total capacitance of the one bus line in pF.

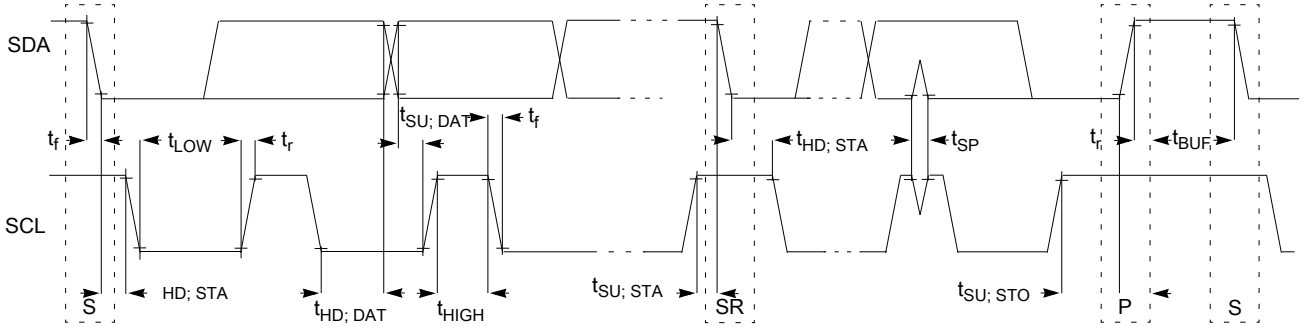



**Figure 17. Timing definition for fast and standard mode devices on the $I^2C$ bus**

## 3.8.5 UART

See General switching specifications.

## 3.8.6 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

**Table 37. I2S/SAI slave mode timing**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 10 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 33 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 10 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid[1] | — | 28 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

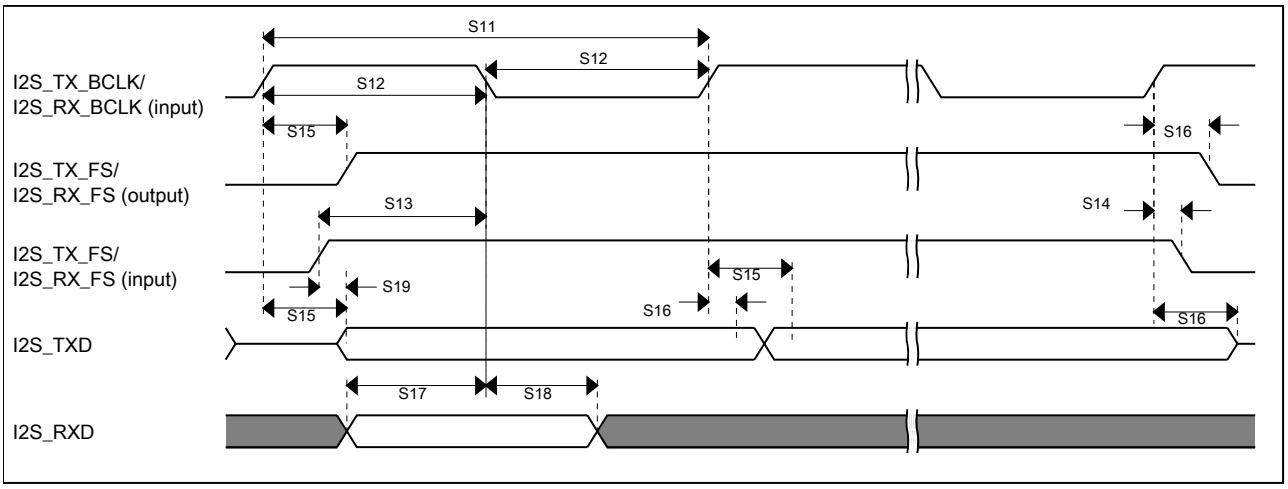



**Figure 19. I2S/SAI timing — slave modes**

### 3.8.6.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

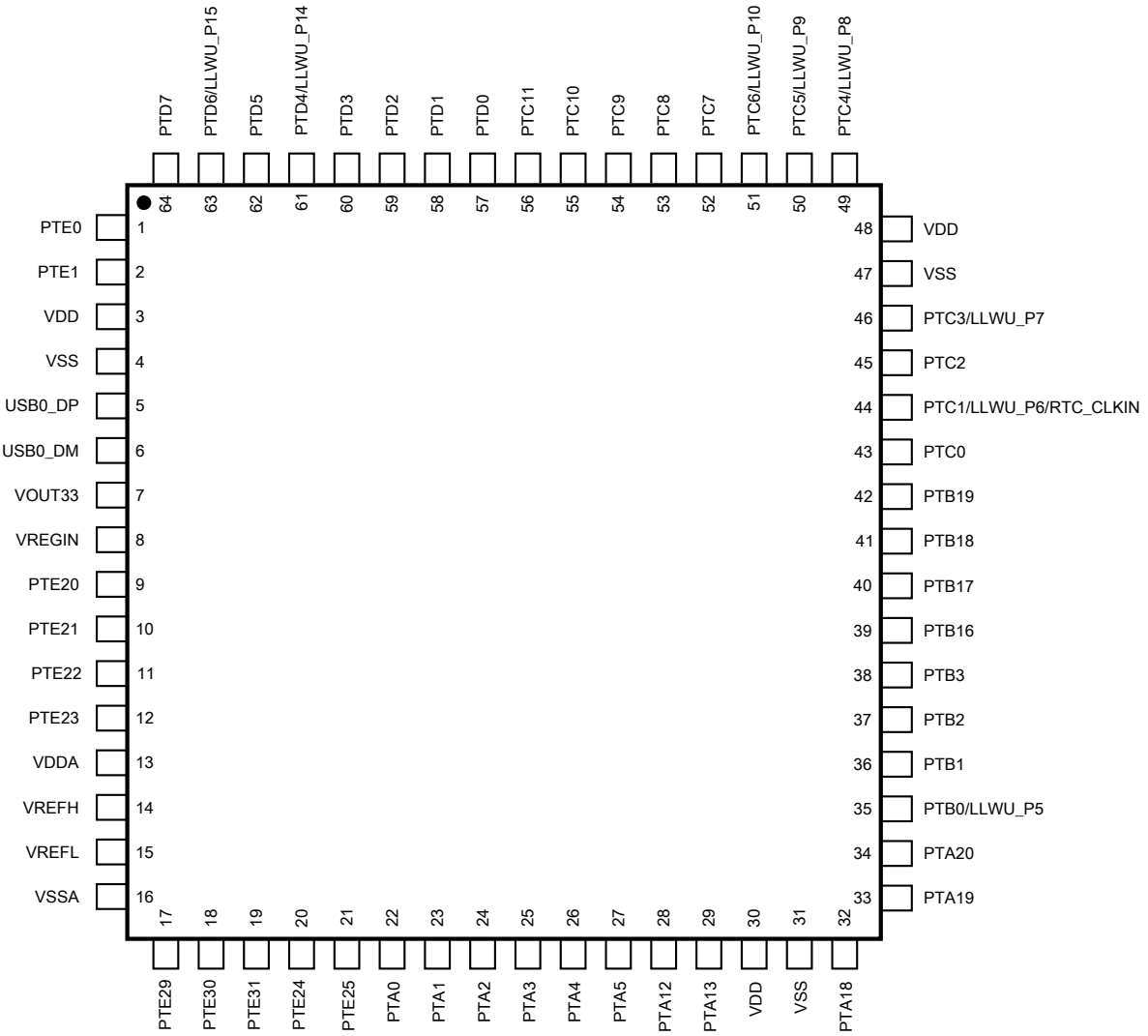



**Figure 22. KL26 64-pin LQFP pinout diagram**

## 7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

## 7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| KL## | Kinetis family | • KL26 |
| A | Key attribute | • Z = Cortex-M0+ |
| FFF | Program flash memory size | • 32 = 32 KB<br>• 64 = 64 KB<br>• 128 = 128 KB |
| R | Silicon revision | • (Blank) = Main<br>• A = Revision after main |
| T | Temperature range (°C) | • V = –40 to 105 |
| PP | Package identifier | • FM = 32 QFN (5 mm x 5 mm)<br>• FT = 48 QFN (7 mm x 7 mm)<br>• LH = 64 LQFP (10 mm x 10 mm) |
| CC | Maximum CPU frequency (MHz) | • 4 = 48 MHz |
| N | Packaging type | • R = Tape and reel |

## 7.4 Example

This is an example part number:

MKL26Z128VFM4

## 8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

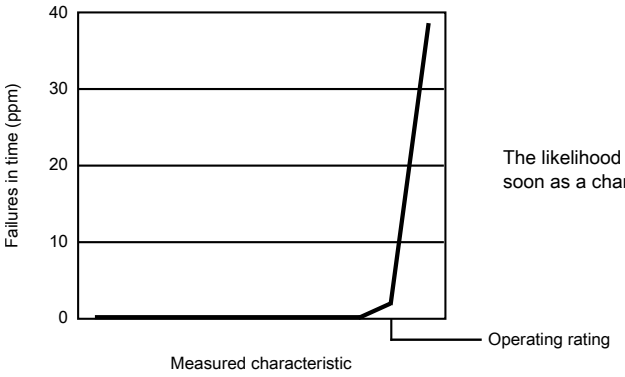
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 8.4.1 Example

This is an example of an operating rating:

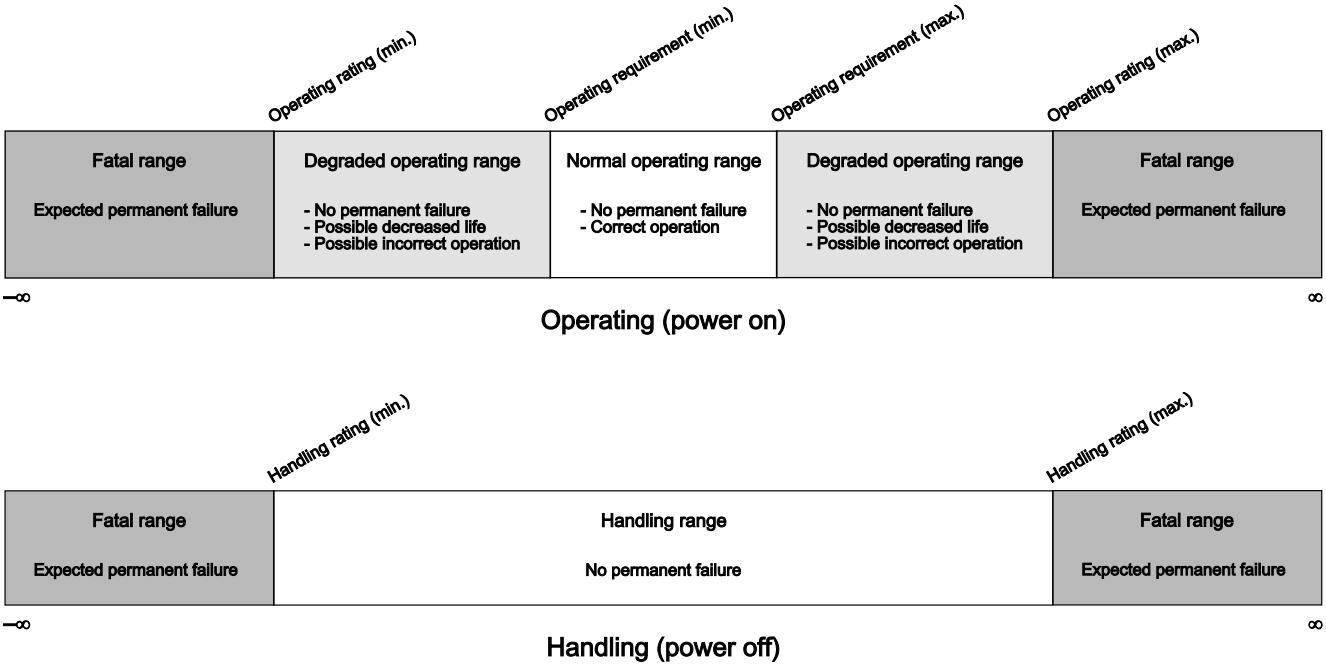
| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

## 8.5 Result of exceeding a rating




The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

## 8.6 Relationship between ratings and operating requirements




## 8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

**Table 41. Typical value conditions**

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

# 9 Revision history

The following table provides a revision history for this document.

**Table 42. Revision history**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 3 | 3/2014 | • Updated the front page and restructured the chapters |
| 4 | 5/2014 | • Updated Power consumption operating behaviors<br>• Updated USB electrical specifications<br>• Updated Definition: Operating behavior |
| 5 | 08/2014 | • Updated related source in the front page<br>• Updated Power consumption operating behaviors<br>• Updated the note in USB electrical specifications |