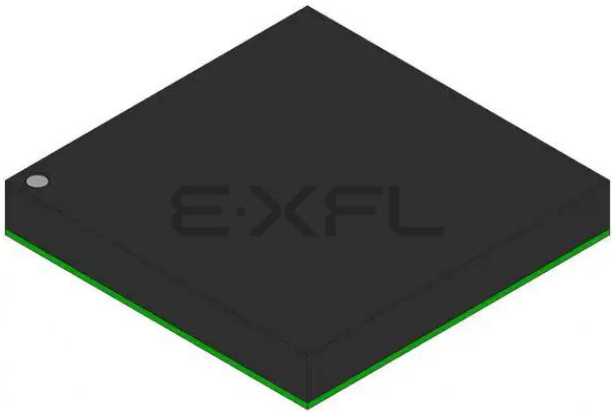

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx514ajm6c

Table 2. i.MX51A Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eSDHC-4 (muxed with P-ATA)	Enhanced Multi-Media Card/ Secure Digital Host Controller	Connectivity Peripherals	Can be configured as eSDHC (see above) and is muxed with the P-ATA interface.
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support both 10 Mbps and 100 Mbps ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
FIRI	Fast Infra-Red Interface	Connectivity Peripherals	Fast Infra-Red Interface
GPIO-1 GPIO-2 GPIO-3 GPIO-4	General Purpose I/O Modules	System Control Peripherals	These modules are used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with a programmable prescaler and compare and capture register. A timer counter value can be captured using an external event, and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU	Graphics Processing Unit	Multimedia Peripherals	The GPU provides hardware acceleration for 2D and 3D graphics algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD720 resolution. It supports color representation up to 32 bits per pixel. The GPU with its 128 KByte memory enables high performance mobile 3D and 2D vector graphics at rates up to 27 Mtriangles/sec, 166 Mpixels/sec, 664 Mpixels/sec (Z).
GPU2D	Graphics Processing Unit-2D Ver. 1	Multimedia Peripherals	The GPU2D provides hardware acceleration for 2D graphic algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD720 resolution.
I^2C-1 I^2C-2 HS-I^2C	I^2C Interface	Connectivity Peripherals	I^2C provides serial interface for controlling peripheral devices. Data rates of up to 400 Kbps are supported by two of the I^2C ports. Data rates of up to 3.4 Mbps (I^2C Specification v2.1) are supported by the HS-I^2C. **Note:** See the errata for the HS-I^2C in the i.MX51 Chip Errata. The two standard I^2C modules have no errata.

Table 21. UHVIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Hysteresis	VHYS	Low voltage mode High voltage mode	0.38 0.95	—	0.43 1.33	V
Schmitt trigger VT+[2,3]	VT+	—	0.5OVDD	—	—	V
Schmitt trigger VT–[2,4]	VT–	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = 0 Vin = OVDD	—	—	See Note [4]	—
Input current (22 kΩ Pull-up)	Iin	Vin = 0	—	—	202	µA
Input current (75 kΩ Pull-up)	Iin	Vin = 0	—	—	61	µA
Input current (100 kΩ Pull-up)	Iin	Vin = 0	—	—	47	µA
Input current (360 kΩ Pull-down)	Iin	Vin = OVDD	—	—	5.7	µA
Keeper Circuit Resistance	—	NA	—	17	—	kΩ

1 To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

2 Overshoot and undershoot conditions (transitions above OVDD and below OVSS) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4 I/O leakage currents are listed in Table 25.

The UHVIO type of I/O cells have to be configured properly according to their supply voltage level, in order to prevent permanent damage to them and in order to not degrade their timing performance.

The HVE control bit of the I/O cell (in IOMUX control registers) should be set to 1 for Low voltage operation and to 0 for High voltage operation.

The HVE bit should be set as follows:

- HVE = 0: High output voltage mode (3.0V to 3.6V)
- HVE = 1: Low output voltage mode (1.65V to 3.1V)

This is related to power domains, such as NVCC_NANDF, NVCC_PER15, and NVCC_PER17.

If HVE bit is not set properly when high voltage level is applied for long durations, it may cause permanent damage over a period of time, causing reduced timing performance of the pad. Similarly, not setting HVE bit properly for low voltage will degrade pad timing performance.

The below discussion clarifies concerns about boot-up period.

The HVE bit is set, by default, to 1 for low voltage operation. As a result, there might be a short period conflict between the HVE bit value and the applied voltage. This conflict is acceptable under the following conditions:

- The UHVIO pads receive supply voltage up to 3.3V (3.6V max); however, the pads do not toggle during the boot-up sequence (using another interface as a boot code source), for boot-up period of about 22 msec.
- The UHVIO pads receive up to 3.15V (3.3V max) and are used for accessing the boot code, for boot-up period of about 11 msec.

In any case, it is recommended to try to minimize the duration of this period and reduce the amount of toggling on the pads as much as possible. For this, it is recommended to add proper HVE bit programming to the DCD boot-up tables. DCD is a table located in the start of the image that can hold up to 60 address/values. ROM code reads addresses and writes values to it. This space should be sufficient to reprogram the NAND Flash pads for HVE bits.

4.3.5 I²C I/O DC Parameters

NOTE

See the errata for HS-I2C in i.MX51 Chip Errata document. The two standard I²C modules have no errata.

The DC Electrical Characteristics listed in Table 22 are guaranteed using operating ranges per Table 13, unless otherwise noted.

Table 22. I²C Standard/Fast/High-Speed Mode Electrical Parameters for Low/Medium Drive Strength

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low-level output voltage	Vol	Iol = 3 mA	—	—	0.4	V
High-Level DC input voltage [1]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1]	VIL	—	0	—	0.3 × OVDD	V
Input Hysteresis	VHYS	—	0.25	—	—	V
Schmitt trigger VT+[1,2]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT– [1,2]	VT–	—	—	—	0.5 × OVDD	V
I/O leakage current (no pull-up)	Iin	VI = OVDD or 0	—	—	See Note [3]	—

1 To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

2 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

3 I/O leakage currents are listed in Table 25.

4.3.6 USBOTG Electrical DC Parameters

This section describes the electrical DC parameters of USBOTG.

4.4.3 UHVIO Output Buffer Impedance

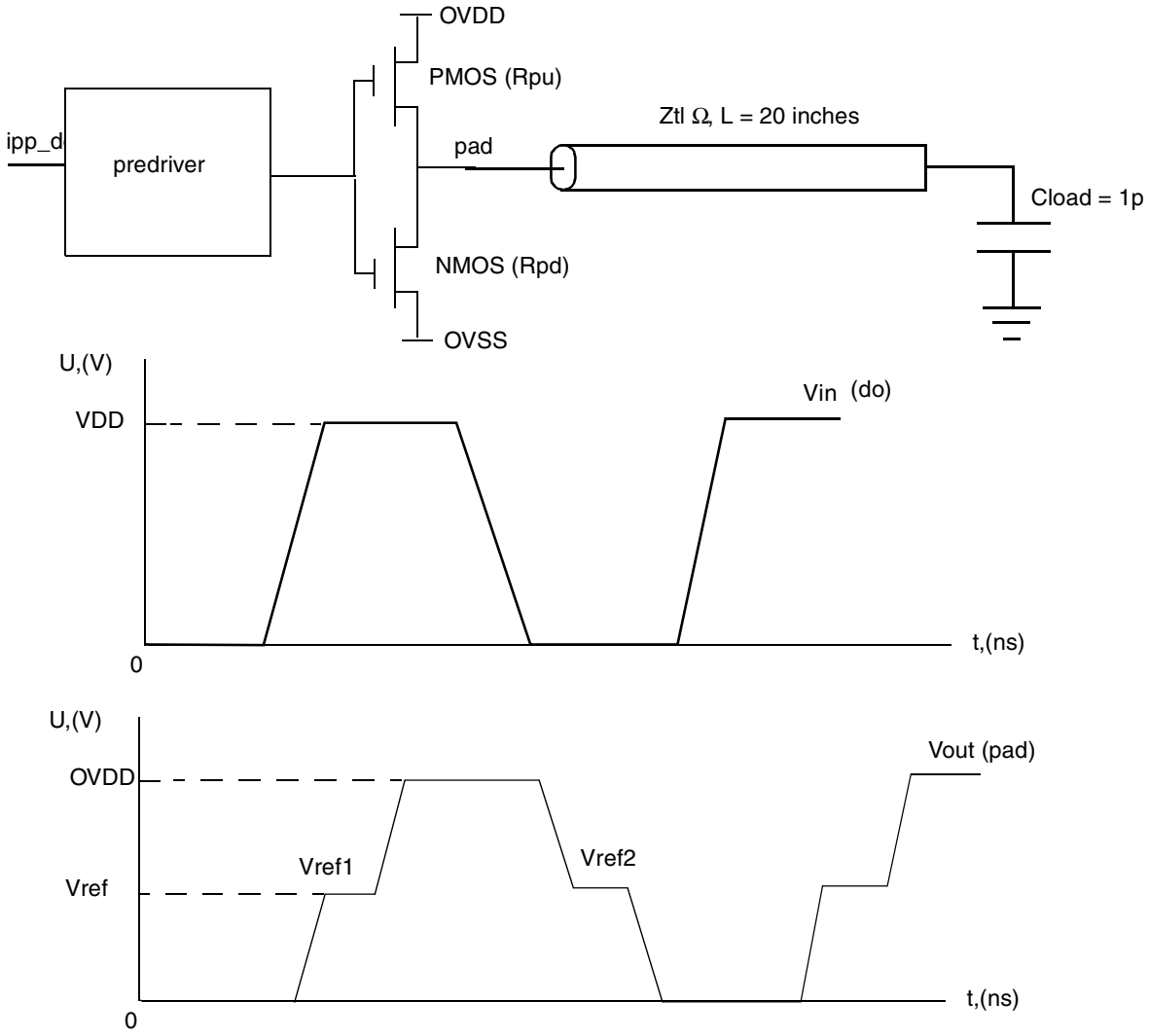
Table 28 shows the UHVIO output buffer impedance.

Table 28. UHVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min		Typ		Max		Unit
			OVDD 1.95 V	OVDD 3.0 V	OVDD 1.875 V	OVDD 3.3 V	OVDD 1.65 V	OVDD 3.6 V	
Output Driver Impedance	Rpu	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω	98 49 32	114 57 38	124 62 41	135 67 45	198 99 66	206 103 69	Ω
Output Driver Impedance	Rpd	Low Drive Strength, Ztl =1 50 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω	97 49 32	118 59 40	126 63 42	154 77 51	179 89 60	217 109 72	Ω

NOTE

Output driver impedance is measured with long transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission lime. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 3).



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 3. Impedance Matching Load for Measurement

Table 43. AC Electrical Characteristics of DDR_clk mobile IO Pads for Fast mode and ovdd=1.65 – 1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt (Low drive)[1]	di/dt	—	62	30	16	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.3/0.36	0.5/0.52	0.82/0.94	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR mobile for Slow mode and ovdd=1.65-1.95V, ipp_hve=0 are placed in Table 44.

Table 44. AC Electrical Characteristics of DDR mobile IO Pads for Slow Mode and ovdd=1.65 – 1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times (High Drive)[1]	tpr	15pF 35pF	1.42/1.42 3.01/2.96	1.20/1.27 2.38/2.40	1.43/1.49 2.37/2.44	ns
Output Pad Transition Times (Medium Drive)[1]	tpr	15pF 35pF	2.05/2.04 4.50/4.42	1.67/1.71 3.48/3.52	1.82/1.87 3.16/3.28	ns
Output Pad Transition Times (Low Drive)[1]	tpr	15pF 35pF	4.06/3.98 8.94/8.86	3.15/3.17 6.92/6.93	2.92/ 3.02 5.69/5.96	ns
Output Pad Propagation Delay (High Drive)[1]	tpo	15pF 35pF	2.07/2.23 3.21/3.48	2.46/2.62 3.35/3.63	3.92/3.93 4.84/4.97	ns
Output Pad Propagation Delay (Medium Drive)[1]	tpo	15pF 35pF	2.53/2.74 4.26/4.58	2.83/3.04 4.12/4.49	4.32/4.35 5.55/5.76	ns
Output Pad Propagation Delay (Low Drive)[1]	tpo	15pF 35pF	3.93/4.23 7.38/7.91	3.89/4.21 6.43/7.01	5.37/5.51 7.45/7.94	ns
Output Pad Slew Rate (High Drive)[1]	tps	15pF 35pF	0.82/0.82 0.39/0.40	0.90/0.85 0.45/0.45	0.69/0.66 0.42/0.41	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15pF 35pF	0.57/0.57 0.26/0.26	0.65/0.63 0.31/0.31	0.54/0.53 0.31/0.30	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15pF 35pF	0.29/0.29 0.13/0.13	0.34/0.34 0.16/0.16	0.34/0.33 0.17/0.17	V/ns
Output Pad di/dt (High Drive)[1]	di/dt	—	47	14	9	mA/ns
Output Pad di/dt (Medium drive)[1]	di/dt	—	27	9	6	mA/ns

4.6.9 DDR2 SDRAM Specific Parameters

Figure 35 shows the timing parameters for DDR2. The timing parameters for this diagram appear in Table 58.

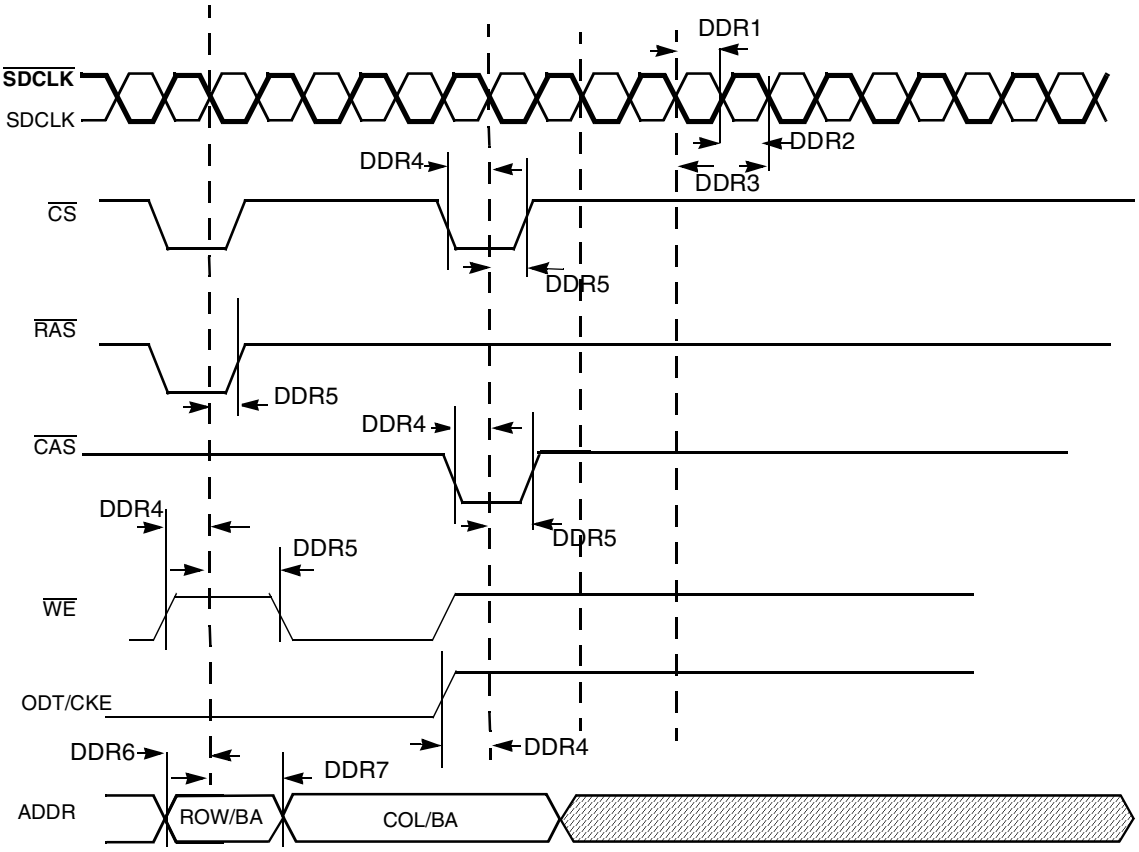


Figure 35. DDR2 SDRAM Basic Timing Parameters

Table 58. DDR2 SDRAM Timing Parameter Table

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
DDR3	SDRAM clock cycle time	t_{CK}	5	—	ns
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}[1]	1.5	—	ns
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}[1]	1.7	—	ns

4.7 External Peripheral Interfaces

The following sections provide information on external peripheral interfaces.

4.7.1 CSPI Timing Parameters

This section describes the timing parameters of the CSPI. The CSPI has separate timing parameters for master and slave modes. The nomenclature used with the CSPI modules and the respective routing of these signals is shown in Table 64.

Table 64. CSPI Nomenclature and Routing

Module	I/O Access
eCSPI1	CSPI1[1], USBH1, and DI1 via IOMUX
eCSPI2	NANDF and USBH1 via IOMUX
CSPI	NANDF, USBH1, SD1, SD2, and GPIO via IOMUX

[1] This set of BGA contacts is labeled CSPI, but is actually an eCSPI channel

4.7.1.1 CSPI Master Mode Timing

Figure 38 depicts the timing of CSPI in Master mode and Table 65 lists the CSPI Master Mode timing characteristics.

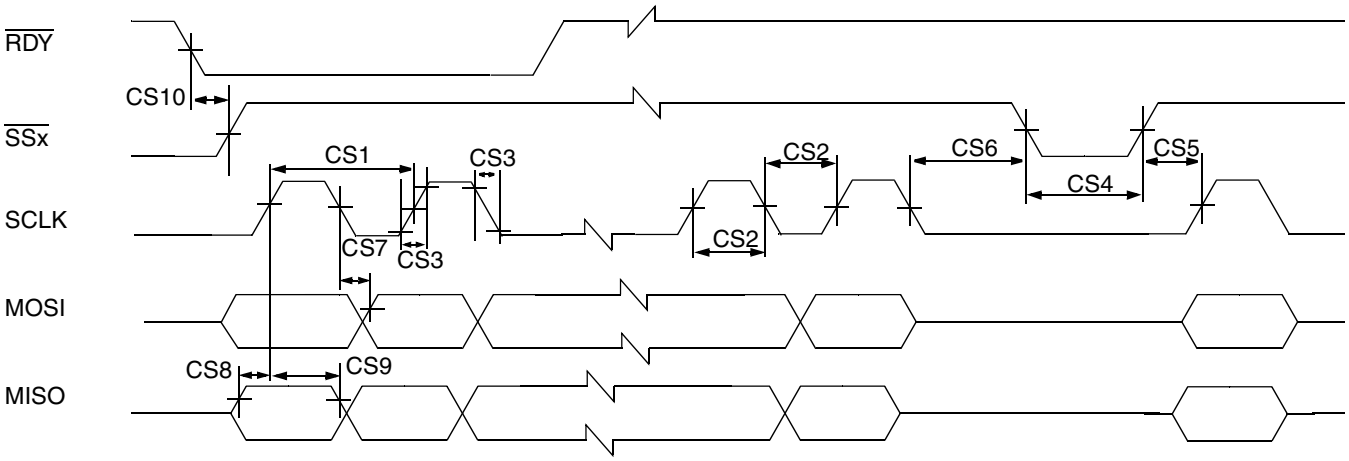


Figure 38. CSPI Master Mode Timing Diagram

Table 65. CSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	26	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	26	—	ns

Table 67. eCSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns
CS11	eCSPIx_DRYN Setup Time	t_{SDRY}	5	—	ns

4.7.2.2 eCSPI Slave Mode Timing

Figure 41 depicts the timing of eCSPI in Slave mode and Table 68 lists the eCSPI Slave Mode timing characteristics.

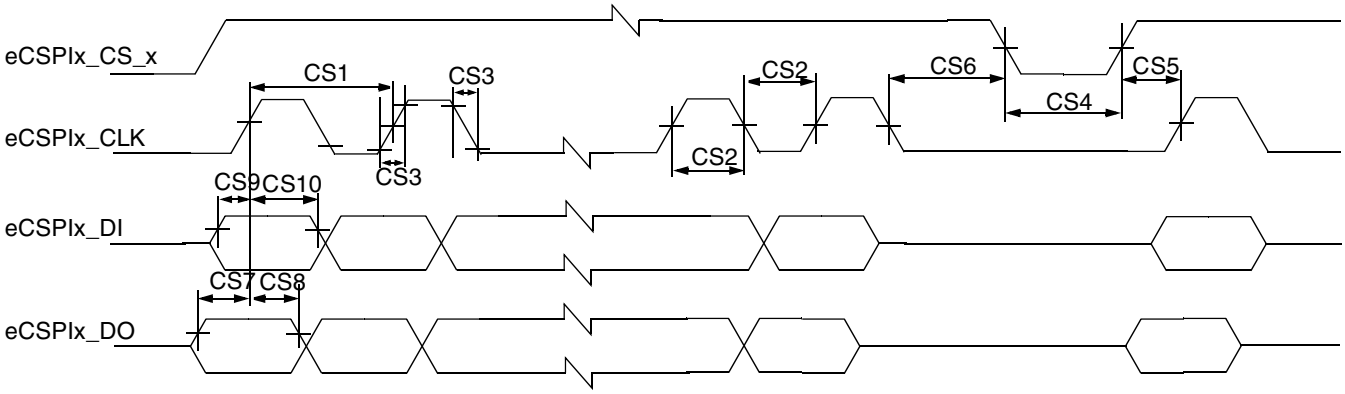


Figure 41. eCSPI Slave Mode Timing Diagram

Table 68. eCSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns

Table 78. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	120	MHz
IP2	Data and control setup time	Tsu	3	—	ns
IP3	Data and control holdup time	Thd	2	—	ns

4.7.8.3 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 79 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 80 shows timing characteristics of signals presented in Figure 54 and Figure 55.

Table 80. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	([1])	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define Display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to **n** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—Width of a horizontal blanking before a first active data in a line. (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH - BGXP - FW) × Tdicp	Width a horizontal blanking after a last active data in a line. (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line.The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT - BGYP - FH) × Tsw	width of second Vertical blanking interval in line.The FH should be built by suitable DI's counter.	ns

Table 80. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET— offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution) Defined by DISP_CLK counter	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET— offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution) The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}, & \text{for integer } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \\ T_{diclk}\left(floor\left[\frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK

DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency

Display interface clock period average value.

$$\bar{T}dicp = T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.75ns$$

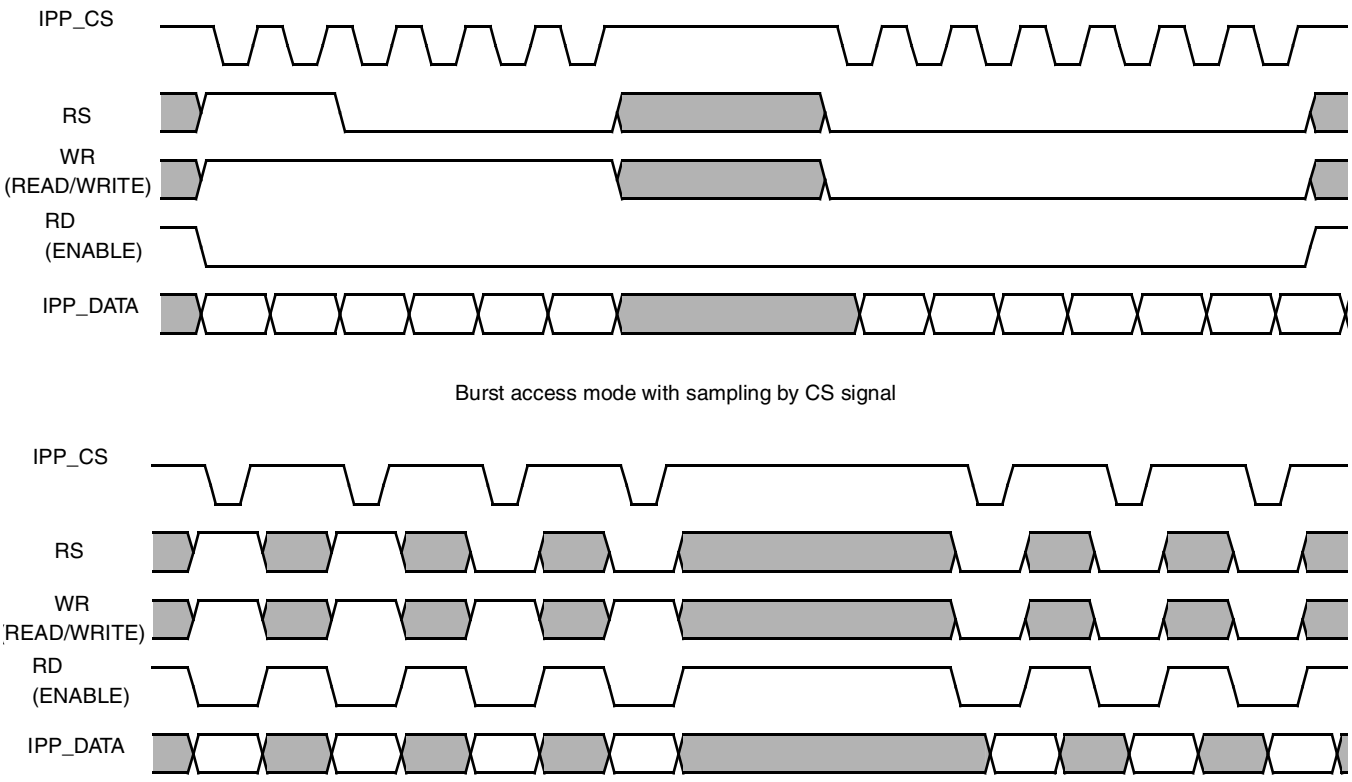


Figure 60. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

4.7.8.8.1 Asynchronous Serial Interface Timing Parameters

Figure 67 depicts timing of the serial interface. Table 85 shows timing characteristics at display access level.

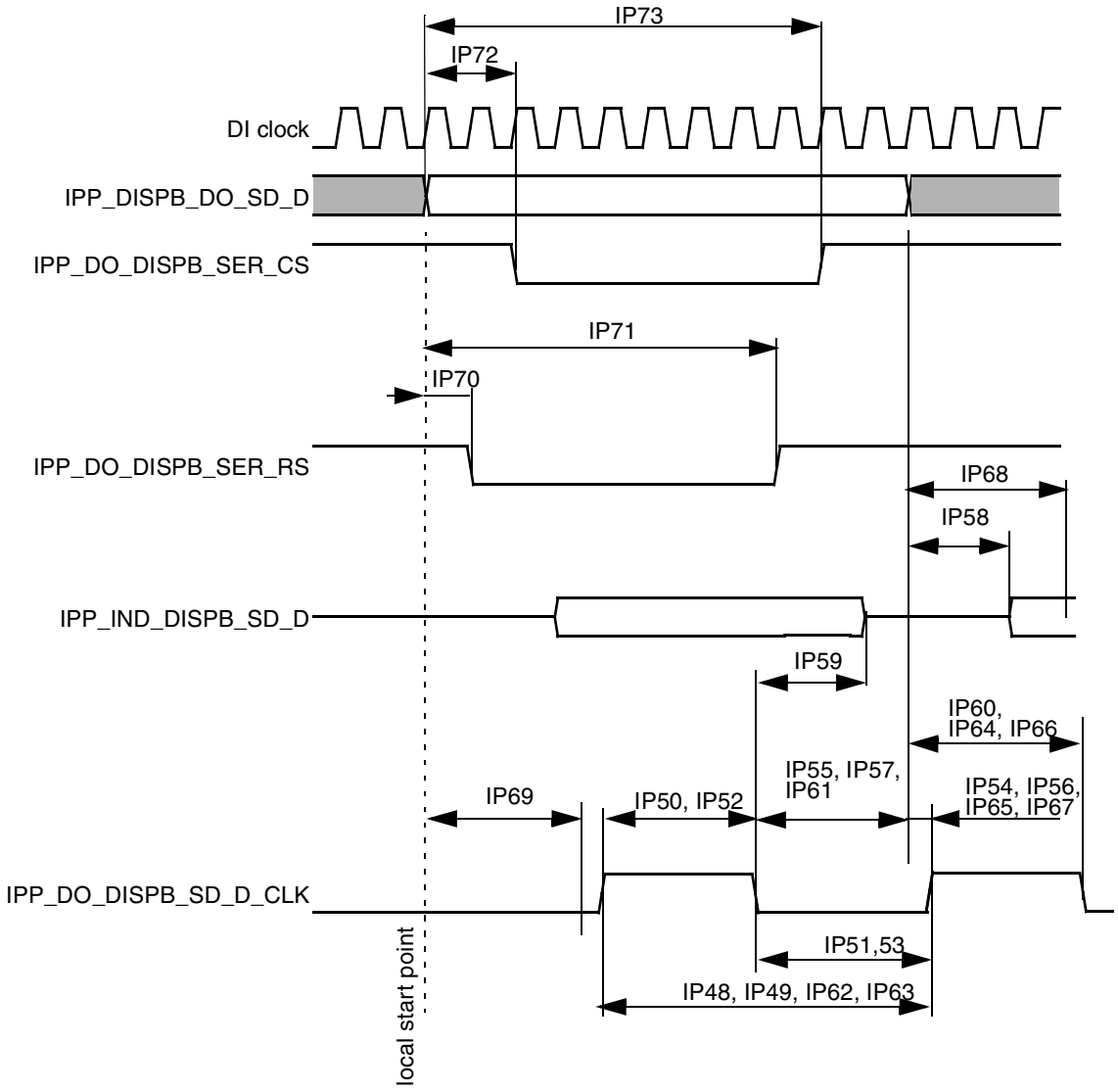


Figure 67. Asynchronous Serial Interface Timing Diagram

Table 85. Asynchronous Serial Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP48	Read system cycle time	Tcycr	Tdicpr–1.5	Tdicpr[2]	Tdicpr+1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw–1.5	Tdicpw[3]	Tdicpw+1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr–Tdicur–1.5	Tdicdr[4]–Tdicur[5]	Tdicdr–Tdicur+1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr–Tdicdr+Tdicur–1.5	Tdicpr–Tdicdr+ Tdicur	Tdicpr–Tdicdr+Tdicur+ 1.5	ns

Figure 80. UDMA In Device Terminates Transfer Timing Diagram

Table 95. UDMA In Burst Timing Parameters

ATA Parameter	Parameter from Figure 78, Figure 79, Figure 80	Description	Controlling Variable
tack	tack	tack (min) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) – (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp (min) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 ×tbuf + 2×tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh ×T) – (tskew1 + tskew2)	time_cvh
—	ton toff[2]	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

[1] There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

[2] Make ton and toff big enough to avoid bus contention.

4.7.17.1.1 USB DAT_SE0 Bi-Directional Mode

Table 113 shows the signal definitions in DAT_SE0 bi-directional mode and Figure 100 shows the USB transmit waveform in DAT_SE0 bi-directional mode.

Table 113. Signal Definitions—DAT_SE0 Bi-Directional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	TX data when USB_TXOE_B is low Differential RX data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 RX indicator when USB_TXOE_B is high

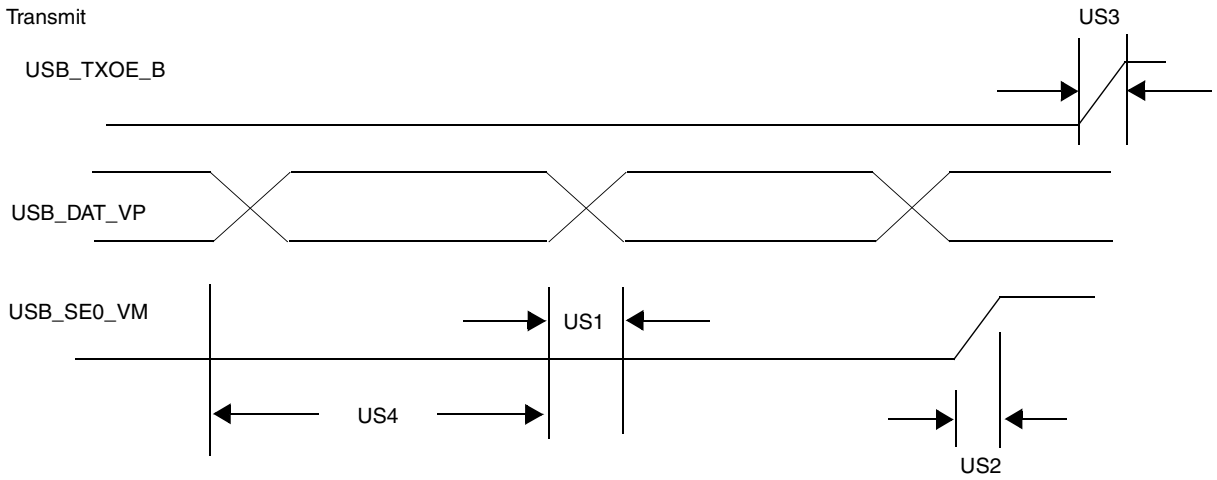


Figure 100. USB Transmit Waveform in DAT_SE0 Bi-Directional Mode

Figure 101 shows the USB receive waveform in DAT_SE0 bi-directional mode and Table 114 shows the definitions of USB receive waveform in DAT_SE0 bi-directional mode.

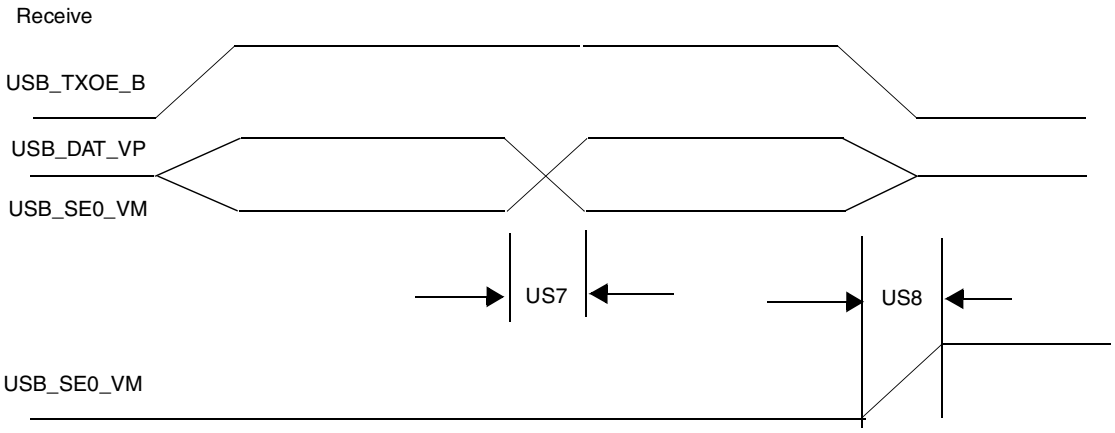


Figure 101. USB Receive Waveform in DAT_SE0 Bi-Directional Mode

Table 127. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
VDD_ANA_PLL_B	W19
VDD_DIG_PLL_A	U6
VDD_DIG_PLL_B	W18
VDD_FUSE	R7
VDDA	G8, H8, H12, M8, P16, T13
VDDA33	L18
VDDGP	F6, F7, F8, F9, F10, F11, F12, G6, G7, H7, J7, K7
VREFOUT	U15
VREF	R5
VREG	K21

5.1.2.2 19 x 19 mm, Signal Assignments, Power Rails, and I/O

Table 128 displays an alpha-sorted list of the signal assignments including power rails.

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
AUD3_BB_CK	C8	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_FS	A9	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_RXD	B9	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_TXD	E9	NVCC_PER9	GPIO	Input	Keeper
BOOT_MODE0	AB21	NVCC_PER3	LVIO	Input	100 kΩ pull-up
BOOT_MODE1	AB22	NVCC_PER3	LVIO	Input	100 kΩ pull-up
CKIH1	V19	NVCC_PER3	Analog	Input	Analog
CKIH2	AA20	NVCC_PER3	Analog	Input	Analog
CKIL	Y16	NVCC_SRTC_POW	GPIO	Input	Standard CMOS
CLK_SS	AA21	NVCC_PER3	LVIO	Input	100 kΩ pull-up
COMP[2]	Y17	AHVDDRGB	Analog	Input	Analog
CSI1_D10	R22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D11	R23	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D12	P22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D13	P23	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D14	M20	NVCC_HS10	HSGPIO	Input	Keeper

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DRAM_D26	H2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D27	J5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D28	G1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D29	G2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D3	R1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D30	G3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D31	G4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D4	R4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D5	P5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D6	P4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D7	N5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D8	N2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D9	N1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM0	P3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM1	M2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM2	K2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM3	H5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_RAS	W1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_SDCKE0	AA1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_SDCKE1	W5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_SDCLK	T3	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDCLK_B	T4	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS0	P2	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS0_B	P1	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS1	N4	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS1_B	N3	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS2	J1	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS2_B	J2	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS3	H3	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS3_B	H4	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDWE	U5	NVCC_EMI_DRAM	DDR2	Output	High
EIM_A16[3]	AA9	NVCC_EMI	GPIO	Input	100 kΩ pull-up

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
NANDF_D5	A5	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D6	B6	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D7	C6	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D8	A4	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D9	E7	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_RB0	D2	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB1	D4	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB2	D3	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB3	C1	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RDY_INT	B3	NVCC_NANDF_B	UHVIO	Input	100 kΩ pull-up
NANDF_RE_B	E2	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WE_B	E1	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WP_B	D1	NVCC_NANDF_A	UHVIO	Output	—
OWIRE_LINE	E14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
PMIC_INT_REQ	AA16	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_ON_REQ	W16	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_RDY	AA17	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_STBY_REQ	Y15	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
POR_B	U20	NVCC_PER3	LVIO	Input	100 kΩ pull-up
RESET_IN_B	Y21	NVCC_PER3	LVIO	Input	100 kΩ pull-up
SD1_CLK	A17	NVCC_PER15	UHVIO	Output	—
SD1_CMD	E16	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA0	D16	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA1	A18	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA2	F17	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA3	A19	NVCC_PER15	UHVIO	Input	360 kΩ pull-down
SD2_CLK	B18	NVCC_PER17	UHVIO	Output	—
SD2_CMD	G17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA0	E17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA1	B19	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA2	D17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA3	C17	NVCC_PER17	UHVIO	Input	360 kΩ pull-down

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
STR	A15	NVCC_PER12	—	—	—
TEST_MODE	V20	NVCC_PER3	GPIO	Input	100 kΩ pull-down
UART1_CTS	B14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_RTS	D13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_RXD	E13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_TXD	A13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART2_RXD	A14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART2_TXD	C14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART3_RXD	F14	NVCC_PER12	GPIO	Input	Keeper
UART3_TXD	B15	NVCC_PER12	GPIO	Input	Keeper
USBH1_CLK	D11	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA0	E12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA1	A11	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA2	B12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA3	C12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA4	D12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA5	A12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA6	B13	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA7	C13	NVCC_PER11	GPIO	Input	Keeper
USBH1_DIR	B11	NVCC_PER11	GPIO	Input	Keeper
USBH1_NXT	C11	NVCC_PER11	GPIO	Input	Keeper
USBH1_STP	E11	NVCC_PER11	GPIO	Input	Keeper
XTAL[2]	AC20	NVCC_OSC	Analog	Output	—

1 The state immediately after reset and before ROM firmware or software has executed.

2 See Table 3 on page 11 for more information.

3 During power-on reset this port acts as input for fuse override signal. See Table 129 on page 167 for more information.

4 During power-on reset this port acts as output for diagnostic signal. See Table 129 on page 167 for more information.