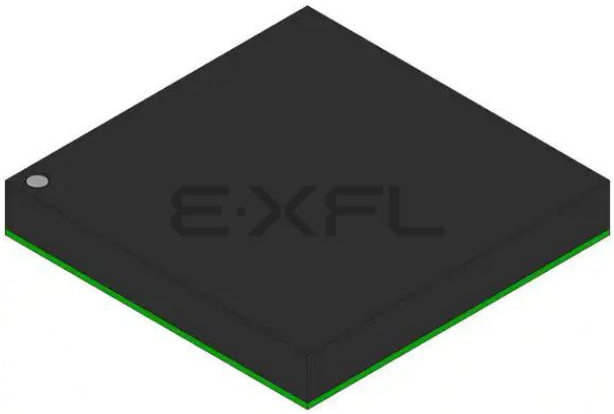


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx516ajm6c

Table 13 shows the i.MX51 operating ranges.

Table 13. i.MX51A Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP MCIMX51xA products	ARM core supply voltage $0 < f_{ARM} \leq 600$ MHz	0.95	1.0	1.1	V
	ARM core supply voltage Stop mode	0.9	0.95	1.05	V
VCC MCIMX51xA products	Peripheral supply voltage High Performance Mode (HPM) The clock frequencies are derived from AXI and AHB buses using 133 or 166 MHz (as needed). The DDR clock rate is 200 MHz. **Note:** For detailed information about the use of 133 or 166 MHz clocks, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).	1.175	1.225	1.275	V
	Peripheral supply voltage—Stop mode	0.9	0.95	1.275	V
VDDA	Memory arrays voltage—Run Mode	1.15	1.20	1.275	V
	Memory arrays voltage—Stop Mode	0.9	0.95	1.275	V
VDD_DIG_PLL_A VDD_DIG_PLL_B	PLL Digital supplies	1.15	1.2	1.35	V
VDD_ANA_PLL_A VDD_ANA_PLL_B	PLL Analog supplies	1.75	1.8	1.95	V
NVCC_EMI NVCC_PER5 NVCC_PER10 NVCC_PER11 NVCC_PER12 NVCC_PER13 NVCC_PER14	GPIO EMI Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_IPUx[3] NVCC_PER3 NVCC_PER8 NVCC_PER9	GPIO IPU Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_EMI_DRAM	DDR and Fuse Read Supply	1.65	1.8	1.95	V
VDD_FUSE[4]	Fusebox Program Supply (Write Only)	3.0	—	3.3	V
NVCC_NANDF_x[5] NVCC_PER15 NVCC_PER17	Ultra High voltage I/O (UHVIO) supplies	—			V
	UHVIO_L	1.65	1.875	1.95	
	UHVIO_H	2.5	2.775	3.1	
	UHVIO_UH	3.0	3.3	3.6	
NVCC_USBPHY NVCC_OSC	USB_PHY analog supply, oscillator analog supply[6]	2.25	2.5	2.75	V
TVDAC_DHVDD, NVCC_TV_BACK, AHVDDRGB	TVE-to-DAC level shifter supply, cable detector supply, analog power supply to RGB channel	2.69	2.75	2.91	V

4.5 I/O AC Parameters

The load circuit and output transition time waveforms are shown in Figure 4 and Figure 5. AC electrical characteristics for slow and fast I/O are presented in the Table 29 and Table 30, respectively.

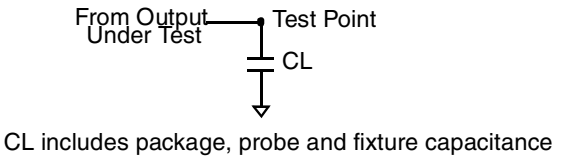


Figure 4. Load Circuit for Output

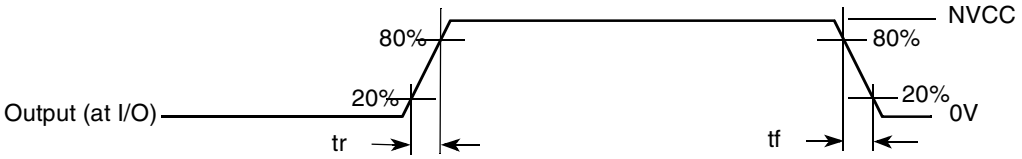


Figure 5. Output Transition Time Waveform

4.5.1 Slow I/O AC Parameters

Table 29 shows the slow I/O AC parameters.

Table 29. Slow I/O AC Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.98/1.52 3.08/2.69	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	2.31/1.838 3.8/2.4	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.92/2.43 5.37/4.99	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.93/4.53 10.55/9.79	ns
Output Pad Slew Rate (Max Drive)	tps	15 pF 35 pF	0.5/0.65 0.32/0.37	—	—	V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.43/0.54 0.26/0.41	—	—	V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.34/0.41 0.18/0.2	—	—	V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.20/0.22 0.09/0.1	—	—	V/ns
Output Pad di/dt (Max Drive)	tdit	—	—	—	30	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	23	mA/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	15	mA/ns

4.6.9 DDR2 SDRAM Specific Parameters

Figure 35 shows the timing parameters for DDR2. The timing parameters for this diagram appear in Table 58.

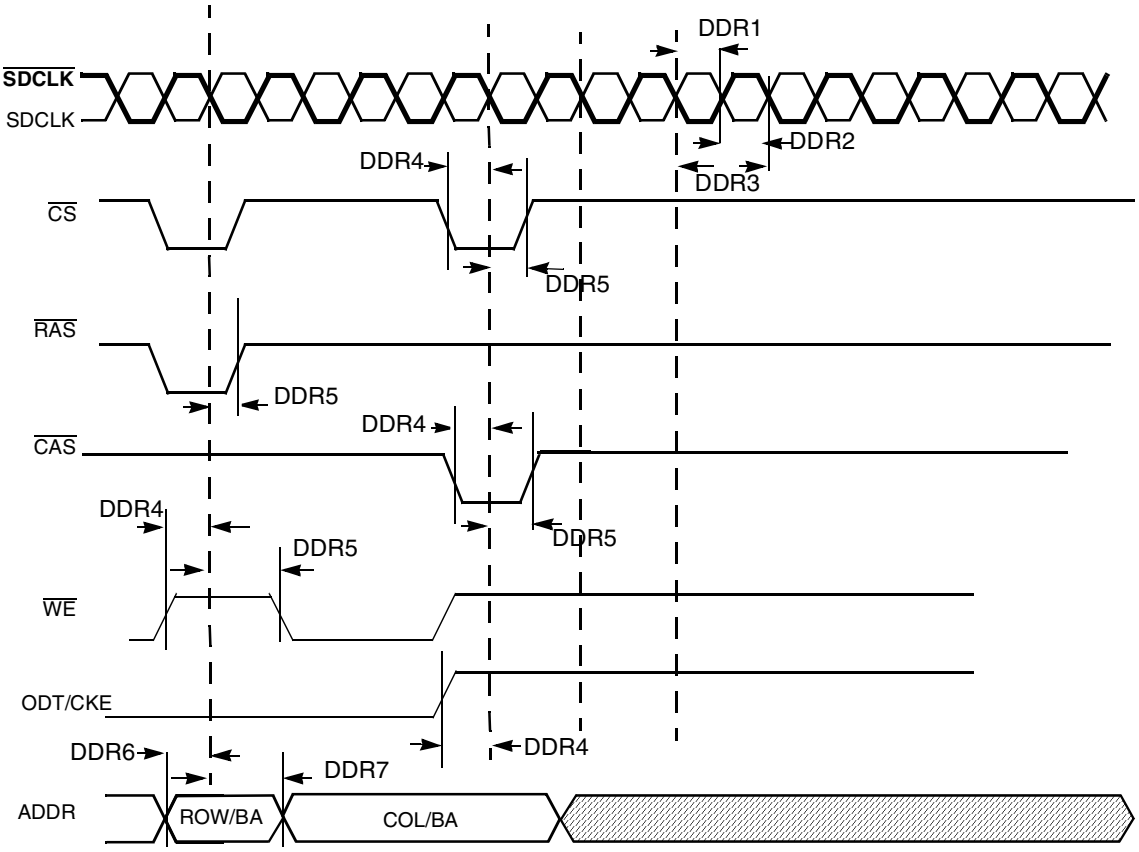


Figure 35. DDR2 SDRAM Basic Timing Parameters

Table 58. DDR2 SDRAM Timing Parameter Table

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
DDR3	SDRAM clock cycle time	t_{CK}	5	—	ns
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}[1]	1.5	—	ns
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}[1]	1.7	—	ns

Table 66. CSPI Slave Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS8	MOSI Hold Time	t_{Hmosi}	5	—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	0	35	ns

4.7.2 eCSPI Timing Parameters

This section describes the timing parameters of the eCSPI. The eCSPI has separate timing parameters for master and slave modes. The nomenclature used with the CSPI modules and the respective routing of these signals is shown in Table 64.

4.7.2.1 eCSPI Master Mode Timing

Figure 40 depicts the timing of eCSPI in Master mode and Table 67 lists the eCSPI Master Mode timing characteristics.

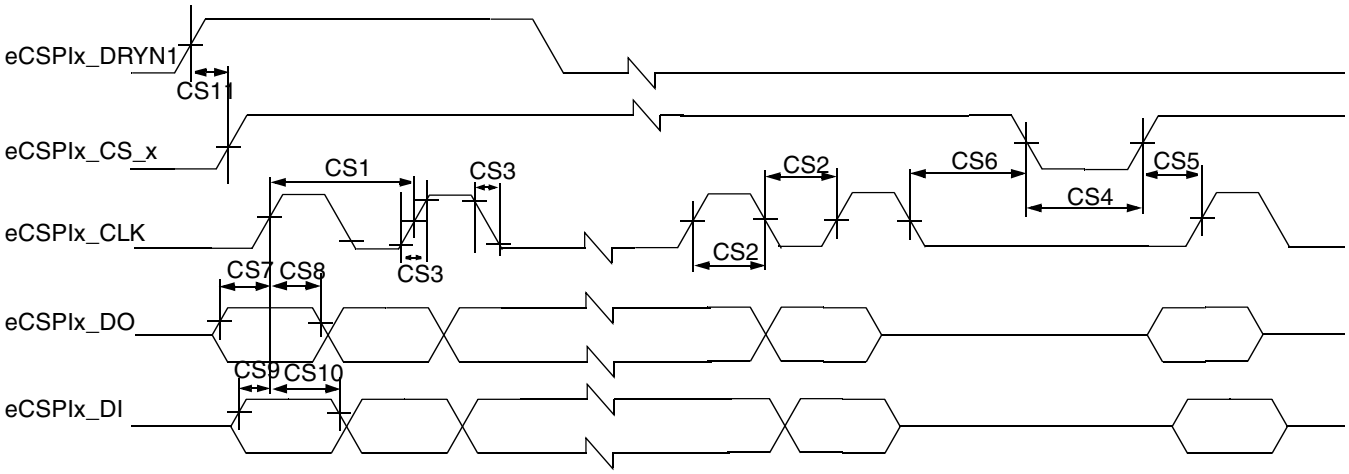


Figure 40. eCSPI Master Mode Timing Diagram

Table 67. eCSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns

internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC and DRDY signals.

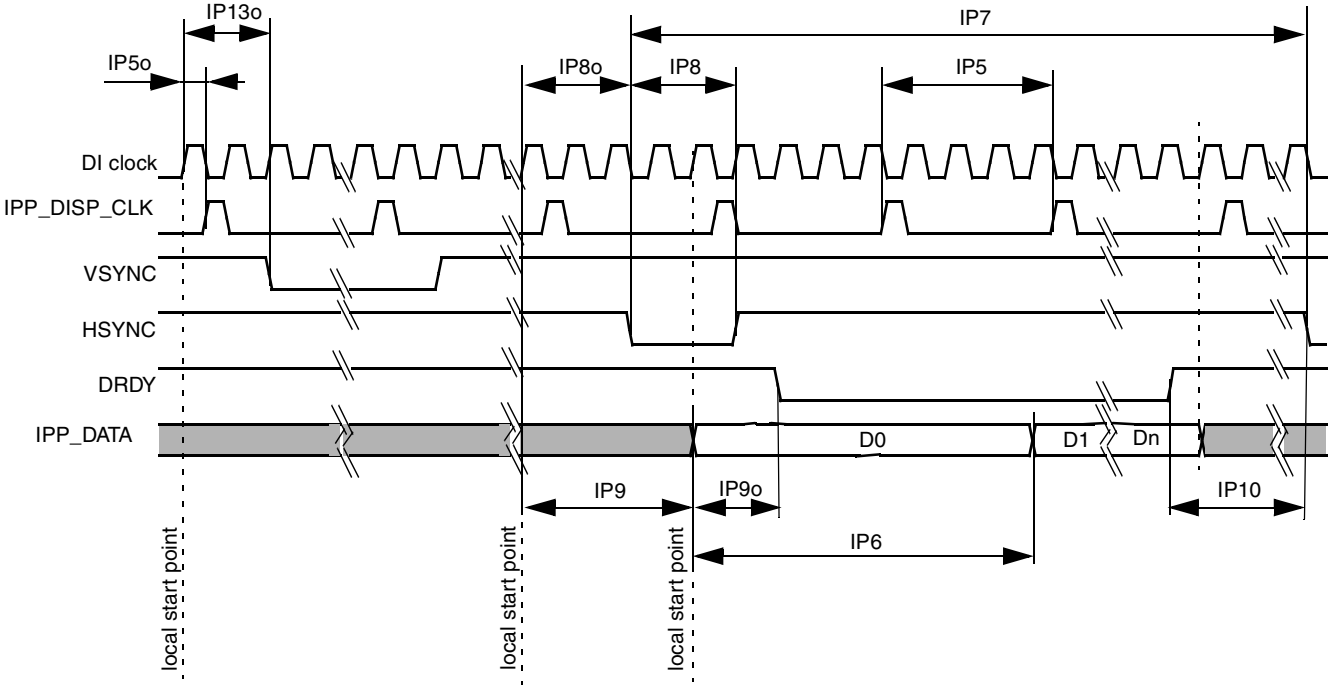


Figure 54. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 55 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

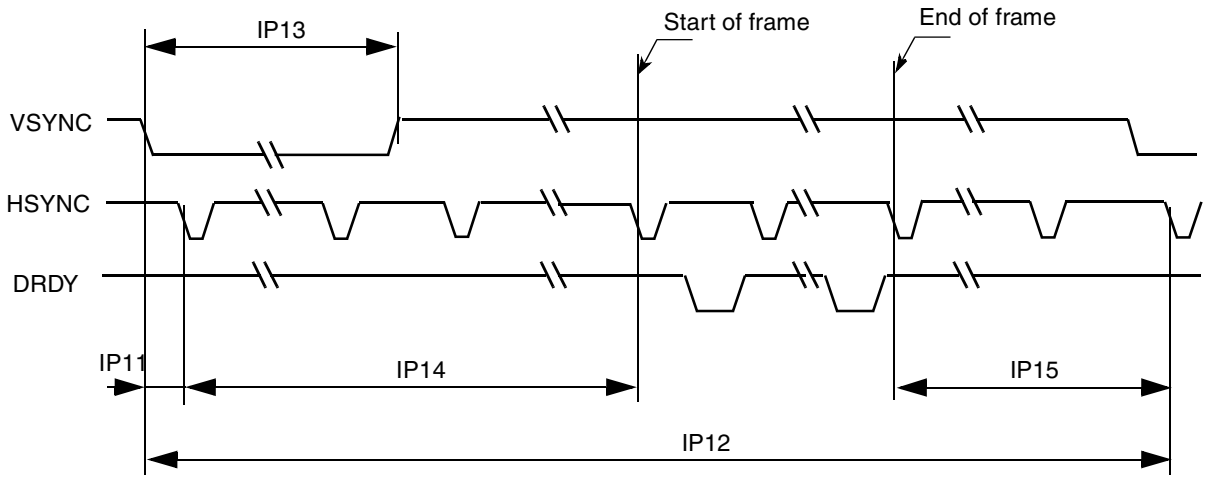


Figure 55. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 80 shows timing characteristics of signals presented in Figure 54 and Figure 55.

Table 80. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	([1])	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define Display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to **n** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—Width of a horizontal blanking before a first active data in a line. (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH - BGXP - FW) × Tdicp	Width a horizontal blanking after a last active data in a line. (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line.The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT - BGYP - FH) × Tsw	width of second Vertical blanking interval in line.The FH should be built by suitable DI's counter.	ns

The maximal accuracy of UP/DOWN edge of IPP_DATA is

$$Accuracy = T_{diclk} \pm 0.75ns$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are programmed via registers.

Figure 56 shows the synchronous display interface timing diagram for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set by using the register. Table 81 shows the timing characteristics for the diagram shown in Figure 56.

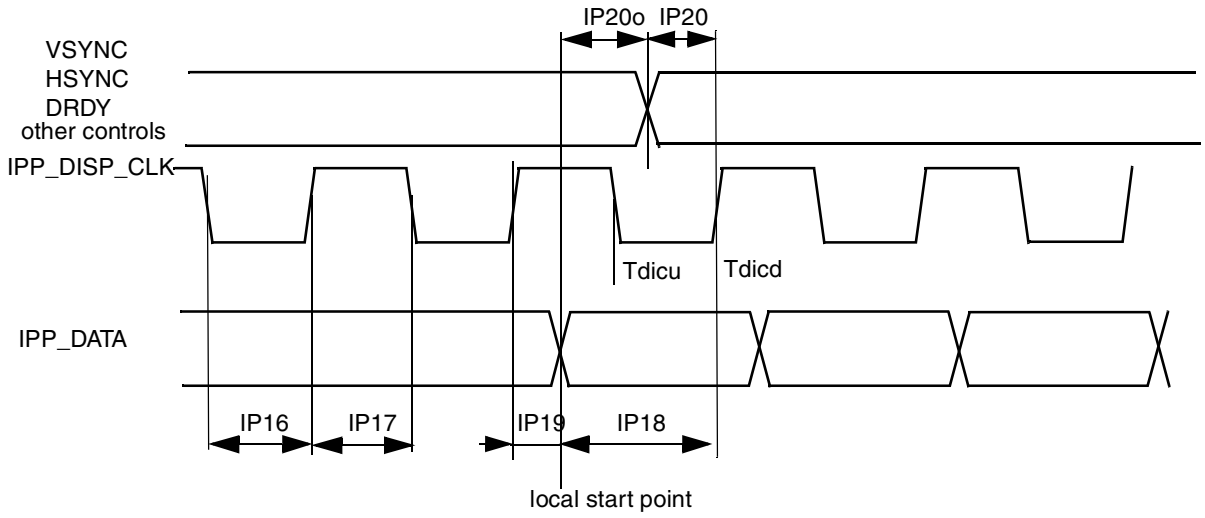


Figure 56. Synchronous Display Interface Timing Diagram—Access Level

Table 81. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu–1.5	Tdicd[2]–Tdicu[3]	Tdicd–Tdicu+1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp–Tdicd+Tdicu–1.5	Tdicp–Tdicd+Tdicu	Tdicp–Tdicd+Tdicu+1.5	ns
IP18	Data setup time	Tdsu	Tdicd–1.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp–Tdicd–1.5	Tdicp–Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu–1.5	Tocsu	Tocsu+1.5	—
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	Tdicd–1.5–Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

4.7.8.6.1 TV Encoder Performance Specifications

All the parameters in the table are defined under the following conditions:

Rset = 1.05 kΩ ±1%, resistor on VREFOUT pin to Ground

Rload = 37.5 Ω ±1%, output load to Ground

The TV encoder output specifications are shown in Table 82.

Table 82. TV Encoder Video Performance Specifications

Parameter	Conditions	Min	Typ	Max	Unit
DAC STATIC PERFORMANCE					
Resolution[1]	—	—	10	—	Bits
Integral Nonlinearity (INL)[2]	—	—	1	2	LSBs
Differential Nonlinearity (DNL)[2]	—	—	0.6	1	LSBs
Channel-to-channel gain matching[2]	—	—	2	—	%
Full scale output voltage[2]	Rset = 1.05 kΩ ±1% Rload = 37.5 Ω±1%	1.24	1.35	1.45	V
DAC DYNAMIC PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	F_{out} = 3.38 MHz F_{samp} = 216 MHz	—	59	—	dBc
Spurious Free Dynamic Range (SFDR)	F_{out} = 9.28 MHz F_{samp} = 297 MHz	—	54	—	dBc
VIDEO PERFORMANCE IN SD MODE[2, 3]					
Short Term Jitter (Line to Line)	—	—	2.5	—	±ns
Long Term Jitter (Field to Field)	—	—	3.5	—	±ns
Frequency Response	0-4.0 MHz	–0.1	—	0.1	dB
	5.75 MHz	–0.7	—	0	dB
Luminance Nonlinearity	—	—	0.5	—	±%
Differential Gain	—	—	0.35	—	%
Differential Phase	—	—	0.6	—	Degrees
Signal-to-Noise Ratio (SNR)	Flat field full bandwidth	—	75	—	dB
Hue Accuracy	—	—	0.8	—	±Degrees
Color Saturation Accuracy	—	—	1.5	—	±%
Chroma AM Noise	—	—	–70	—	dB
Chroma PM Noise	—	—	–47	—	dB
Chroma Nonlinear Phase	—	—	0.5	—	±Degrees
Chroma Nonlinear Gain	—	—	2.5	—	±%
Chroma/Luma Intermodulation	—	—	0.1	—	±%

Figure 75 shows timing for PIO write and Table 93 lists the timing parameters for PIO write.

Figure 75. Multi-word DMA (MDMA) Timing

Table 93. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 75	Value	Controlling Variable
t1	t1	t1 (min) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min) = time_2w × T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min) = (time_2w – time_on)× T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min) = time_4 × T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2×tbuf)	time_ax
t0	—	t0(min) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough	—
—	—	Avoid bus contention when switching buffer off by making toff long enough	—

Figure 76 shows timing for MDMA read, Figure 77 shows timing for MDMA write, and Table 94 lists the timing parameters for MDMA read and write.

Figure 76. MDMA Read Timing Diagram

Figure 77. MDMA Write Timing Diagram

Table 94. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 76, Figure 77	Value	Controlling Variable
tm, ti	tm	tm (min) = ti (min) = time_m × T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min) = td (min) = time_d × T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min) = (time_d + time_k) × T	time_d, time_k
tg(read)	tgr	tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min-drive) = 0	—
tg(write)	—	tg (min-write) = time_d × T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min-write) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k–2)×T – (tsu + tco + 2×tbuf + 2×tcable2)	time_d, time_k

Table 94. MDMA Read and Write Timing Parameters (continued)

ATA Parameter	Parameter from Figure 76, Figure 77	Value	Controlling Variable
tn, tj	tkjn	tn= tj= tkjn = (max(time_k,. time_jn) × T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.7.11.2 Ultra DMA (UDMA) Input Timing

Figure 78 shows timing when the UDMA in transfer starts, Figure 79 shows timing when the UDMA in host terminates transfer, Figure 80 shows timing when the UDMA in device terminates transfer, and Table 95 lists the timing parameters for UDMA in burst.

Figure 78. UDMA In Transfer Starts Timing Diagram

Figure 79. UDMA In Host Terminates Transfer Timing Diagram

Table 99. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.7.14 SPDIF Timing Parameters

Table 100 shows the timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF).

Table 100. SPDIF Timing

Characteristics	Symbol	All Frequencies		Unit
		Min	Max	
SPDIFOUT output (load = 50 pF) • Skew • Transition rising • Transition falling	—	 — — —	 1.5 24.2 31.3	 ns
SPDIFOUT output (load = 30 pF) • Skew • Transition rising • Transition falling	—	 — — —	 1.5 13.6 18.0	 ns

4.7.15 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces is summarized in Table 101.

Table 101. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External—AUD3 I/O
AUDMUX port 4	AUD4	External—EIM or CSPI1 I/O via IOMUX
AUDMUX port 5	AUD5	External—EIM or SD1 I/O via IOMUX

Table 101. AUDMUX Port Allocation (continued)

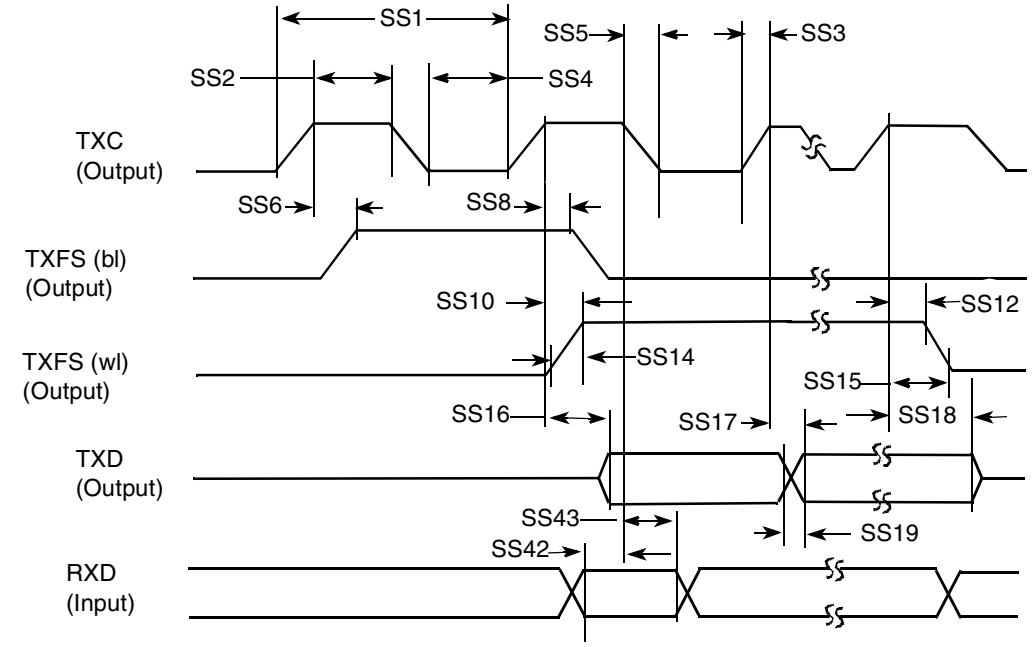
Port	Signal Nomenclature	Type and Access
AUDMUX port 6	AUD6	External—EIM or DISP2 via IOMUX
AUDMUX port 7	SSI 3	Internal

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

4.7.15.1 SSI Transmitter Timing with Internal Clock

Figure 92 depicts the SSI transmitter internal clock timing and Table 102 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only

Figure 92. SSI Transmitter Internal Clock Timing Diagram

4.7.15.2 SSI Receiver Timing with Internal Clock

Figure 93 depicts the SSI receiver internal clock timing and Table 103 lists the timing parameters for the SSI receiver internal clock.

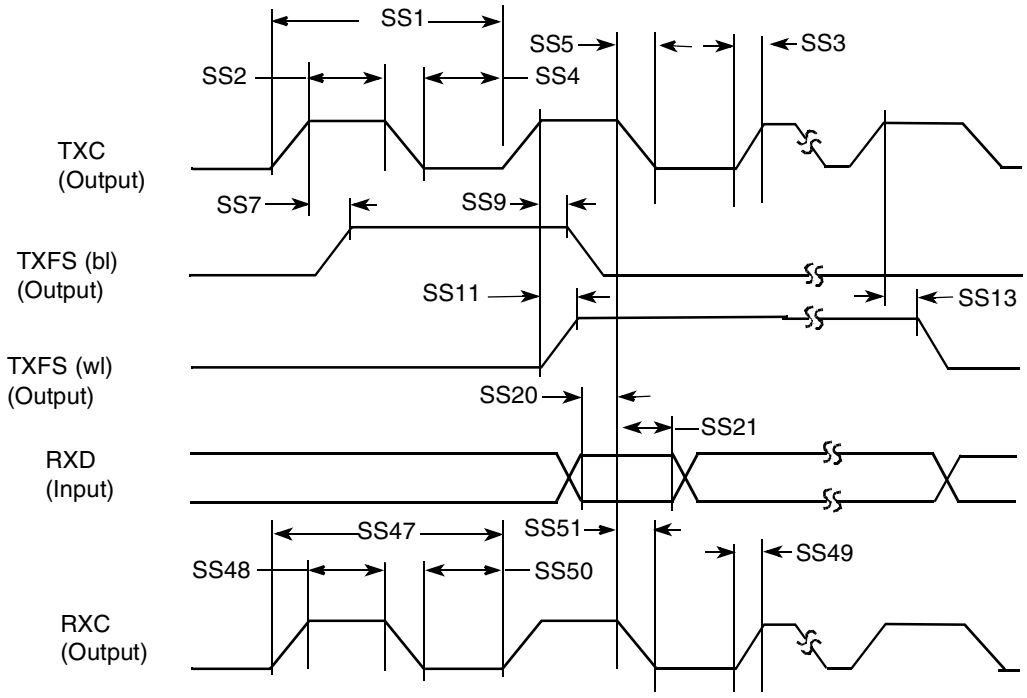


Figure 93. SSI Receiver Internal Clock Timing Diagram

Table 103. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	30	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns

Table 104. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.16.1.1 UART RS-232 Serial Mode Timing

UART Transmitter

Figure 96 depicts the transmit timing of UART in RS-232 serial mode, with 8 data bit/1 stop bit format. Table 107 lists the UART RS-232 serial mode transmit timing characteristics.

Figure 96. UART RS-232 Serial Mode Transmit Timing Diagram

Table 107. UART RS-232 Serial Mode Transmit Timing Diagram

ID	Parameter	Symbol	Min	Max	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1]$-T_{ref\_clk}$[2]	$1/F_{baud\_rate}+T_{ref\_clk}$	—

[1] $1/F_{baud\_rate}$: Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

UART Receiver

Figure 97 depicts the RS-232 serial mode receive timing, with 8 data bit/1 stop bit format. Table 108 lists serial mode receive timing characteristics.

Figure 97. UART RS-232 Serial Mode Receive Timing Diagram

Table 108. UART RS-232 Serial Mode Transmit Timing Diagram

ID	Parameter	Symbol	Min	Max	Units
UA1	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2]$-1/(16\times F_{baud\_rate})$	$1/F_{baud\_rate}+1/(16\times F_{baud\_rate})$	—

[1] The UART receiver can tolerate 1/(16×Fbaud_rate) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16×Fbaud_rate).

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

4.7.16.1.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.7.17.1.1 USB DAT_SE0 Bi-Directional Mode

Table 113 shows the signal definitions in DAT_SE0 bi-directional mode and Figure 100 shows the USB transmit waveform in DAT_SE0 bi-directional mode.

Table 113. Signal Definitions—DAT_SE0 Bi-Directional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	TX data when USB_TXOE_B is low Differential RX data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 RX indicator when USB_TXOE_B is high

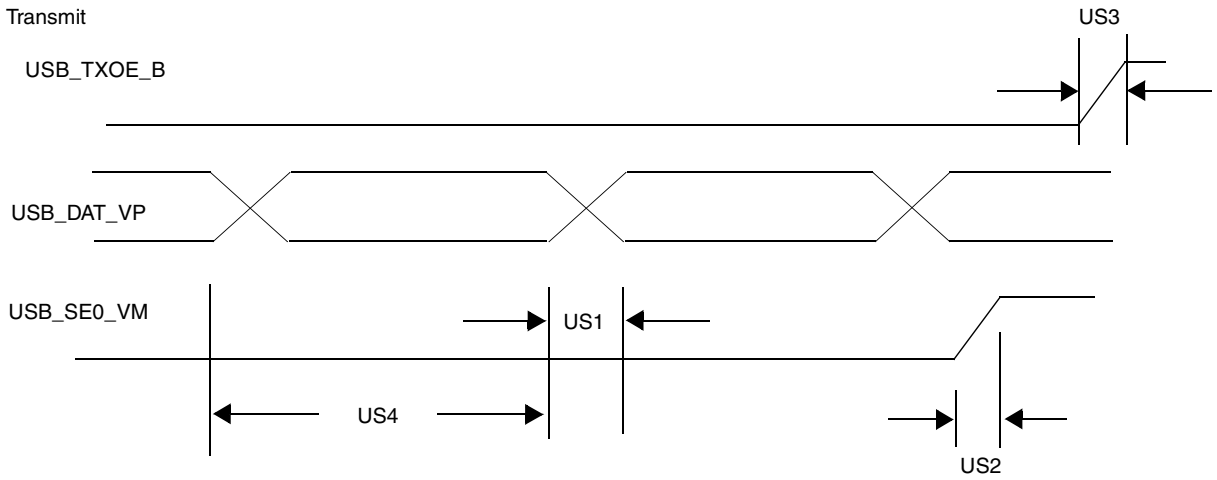


Figure 100. USB Transmit Waveform in DAT_SE0 Bi-Directional Mode

Figure 101 shows the USB receive waveform in DAT_SE0 bi-directional mode and Table 114 shows the definitions of USB receive waveform in DAT_SE0 bi-directional mode.

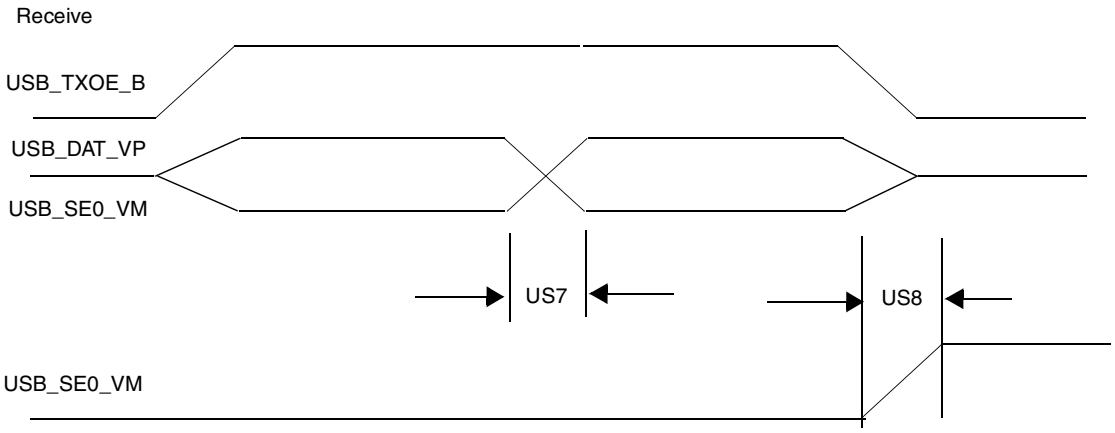


Figure 101. USB Receive Waveform in DAT_SE0 Bi-Directional Mode

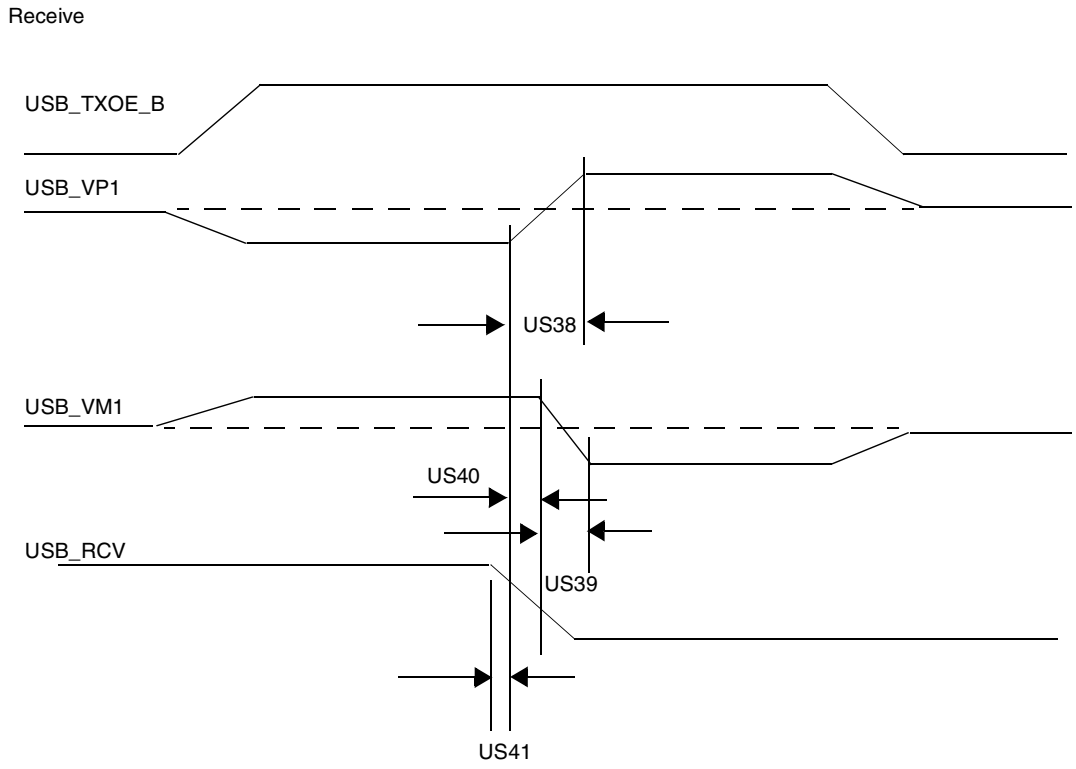


Figure 107. USB Receive Waveform in VP_VM Uni-directional Mode

Table 120 shows the USB port timing specification in VP_VM uni-directional mode.

Table 120. USB Timing Specification in VP_VM Unidirectional Mode

ID	Parameter	Signal	Direction	Min	Max	Unit	Conditions / Reference Signal
US30	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	TX Overlap	USB_SE0_VM	Out	–3.0	3.0	ns	USB_DAT_VP
US38	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US39	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF
US40	RX Skew	USB_VP1	In	–4.0	4.0	ns	USB_VM1
US41	RX Skew	USB_RCV	In	–6.0	2.0	ns	USB_VP1

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DISP1_DAT5	T23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT6[3]	C22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT7[3]	C23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT8[3]	D21	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT9[3]	E20	NVCC_IPU4	GPIO	Input	Keeper
DISP2_DAT0	R21	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT1	M19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT10	W22	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT11	R19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT12	Y23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT13	T19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT14	AA23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT15	T21	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT2	P20	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT3	P21	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT4	V22	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT5	V23	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT6	N19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT7	W23	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT8	P19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT9	R20	NVCC_IPU9	GPIO	Input	Keeper
DISPB2_SER_CLK	AC22	NVCC_IPU2	GPIO	Output	High
DISPB2_SER_DIN	U19	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_DIO	V21	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_RS	W21	NVCC_IPU2	GPIO	Output	High
DN	K22	VDDA33	Analog	Output	–
DP	K23	VDDA33	Analog	Output	–
DRAM_A0	AB1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A1	AA2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A10	V2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A11	U4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A12	U2	NVCC_EMI_DRAM	DDR2	Output	High

Table 130. 19 × 19 mm, 0.8 Pitch Ball Map (continued)

	AA	Y	W	V	U	T	R	
1	DRAM_SDCKE0	DRAM_A7	DRAM_RAS	EIM_SDBA0	DRAM_A13	DRAM_D0	DRAM_D3	1
2	DRAM_A1	DRAM_A5	DRAM_A8	DRAM_A10	DRAM_A12	DRAM_A14	DRAM_D2	2
3	DRAM_A2	DRAM_CS1	DRAM_A6	DRAM_A9	EIM_SDBA1	DRAM_SDCLK	DRAM_D1	3
4	EIM_BCLK	DRAM_CS0	DRAM_A4	DRAM_CAS	DRAM_A11	DRAM_SDCLK_B	DRAM_D4	4
5	EIM_CS5	EIM_DTACK	DRAM_SDCKE1	DRAM_A3	DRAM_SDWE	GND	VREF	5
6	EIM_CS4	EIM_CS1	EIM_CS0	VDD_ANA_PLL_A	VDD_DIG_PLL_A	NVCC_EMI_DRAM	NVCC_EMI_DRAM	6
7	EIM_OE	EIM_CS2	EIM_D31	NVCC_EMI	GND_ANA_PLL_A	GND_DIG_PLL_A	VDD_FUSE	7
8	EIM_A19	EIM_D29	EIM_D27	EIM_D23	NVCC_EMI	VCC	GND	8
9	EIM_A16	EIM_D25	EIM_D21	EIM_EB3	NVCC_EMI	VCC	GND	9
10	EIM_D24	EIM_D19	EIM_D17	EIM_EB2	NVCC_EMI	VCC	GND	10
11	EIM_D18	EIM_DA15	EIM_DA13	EIM_DA11	NVCC_EMI	VCC	GND	11
12	EIM_DA12	EIM_DA9	EIM_EB1	EIM_EB0	NVCC_EMI	VCC	GND	12
13	EIM_DA6	EIM_DA5	EIM_DA7	EIM_DA1	NVCC_PER14	VDDA	GND	13
14	EIM_DA2	JTAG_TDI	JTAG_TRSTB	JTAG_MOD	NVCC_SRTC_POW	NVCC_I2C	GND	14
15	JTAG_TDO	PMIC_STBY_REQ	I2C1_CLK	JTAG_TCK	VREFOUT	NGND_TV_BACK	GND	15
16	PMIC_INT_REQ	CKIL	PMIC_ON_REQ	TVDAC_DHVDD	NVCC_TV_BACK	GND	GND	16
17	PMIC_RDY	COMP	NVCC_OSC	NGND_OSC	GND_ANA_PLL_B	VCC	VCC	17
18	AHVDDRGB	AHVDDRGB	VDD_DIG_PLL_B	GND_DIG_PLL_B	NVCC_PER3	NVCC_IPU2	NVCC_IPU9	18
19	AHVSSRGB	AHVSSRGB	VDD_ANA_PLL_B	CKIH1	DISPB2_SER_DIN	DISP2_DAT13	DISP2_DAT11	19
20	CKIH2	FASTR_DIG	FASTR_ANA	TEST_MODE	POR_B	DI1_PIN13	DISP2_DAT9	20
21	CLK_SS	RESET_IN_B	DISPB2_SER_RS	DISPB2_SER_DIO	DI1_D0_CS	DISP2_DAT15	DISP2_DAT0	21
22	DI1_PIN12	DI1_PIN11	DISP2_DAT10	DISP2_DAT4	DISP1_DAT2	DISP1_DAT4	CSI1_D10	22
23	DISP2_DAT14	DISP2_DAT12	DISP2_DAT7	DISP2_DAT5	DISP1_DAT3	DISP1_DAT5	CSI1_D11	23
	AA	Y	W	V	U	T	R	