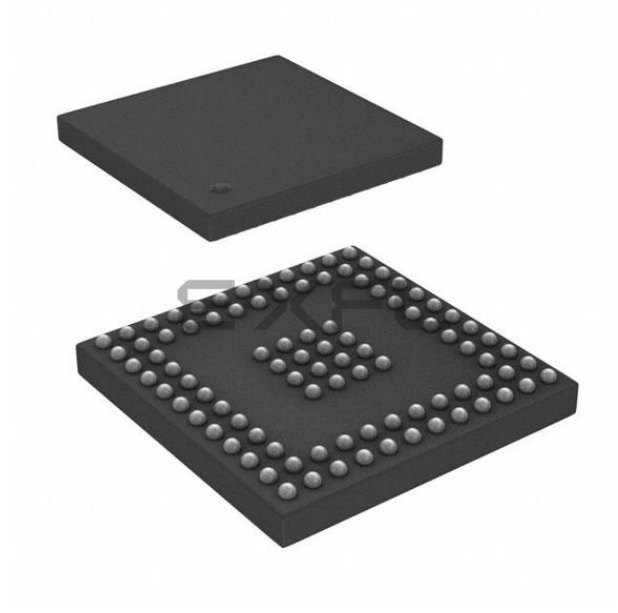

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XCore
Core Size	32-Bit 8-Core
Speed	400MIPS
Connectivity	Configurable
Peripherals	-
Number of I/O	42
Program Memory Size	64KB (16K x 32)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	0.90V ~ 5.5V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	96-LFBGA
Supplier Device Package	96-FBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xs1-a8a-64-fb96-c4

6 Product Overview

The XS1-A8A-64-FB96 comprises a digital and an analog node, as shown in Figure 3. The digital node comprises an xCORE Tile, a Switch, and a PLL (Phase-locked-loop). The analog node comprises a multi-channel ADC (Analog to Digital Converter), deep sleep memory, an oscillator, a real-time counter, and power supply control.

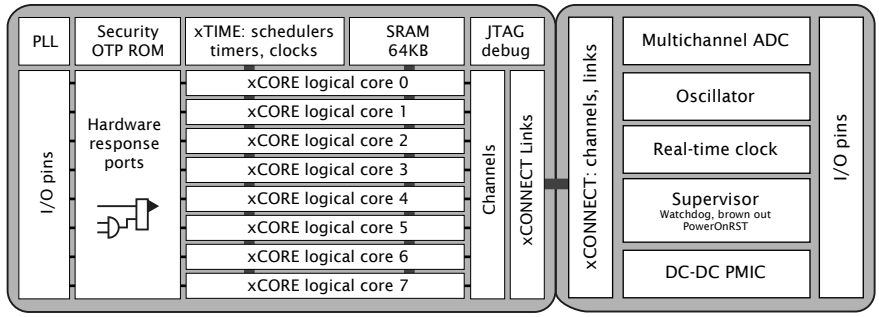


Figure 3: Block Diagram

All communication between the digital and analog node takes place over a link that is connected to the Switch of the digital node. As such, the analog node can be controlled from any node on the system. The analog functions can be configured using a set of node configuration registers, and a set of registers for each of the peripherals.

The device can be programmed using high-level languages such as C/C++ and the XMOS-originated XC language, which provides extensions to C that simplify the control over concurrency, I/O and timing, or low-level assembler.

6.1 XCore Tile

The xCORE Tile is a flexible multicore microcontroller component with tightly integrated I/O and on-chip memory. The tile contains multiple logical cores that run simultaneously, each of which is guaranteed a slice of processing power and can execute computational code, control software and I/O interfaces. The logical cores use channels to exchange data within a tile or across tiles. Multiple devices can be deployed and connected using an integrated switching network, enabling more resources to be added to a design. The I/O pins are driven using intelligent ports that can serialize data, interpret strobe signals and wait for scheduled times or events, making the device ideal for real-time control applications.

6.2 ADC and Power Management

Each XS1-A8A-64-FB96 device includes a set of analog components, including a 12b, 4-channel ADC, power management unit, watchdog timer, real-time counter and deep sleep memory. The device reduces the number of additional external components required and allows designs to be implemented using simple 2-layer boards.

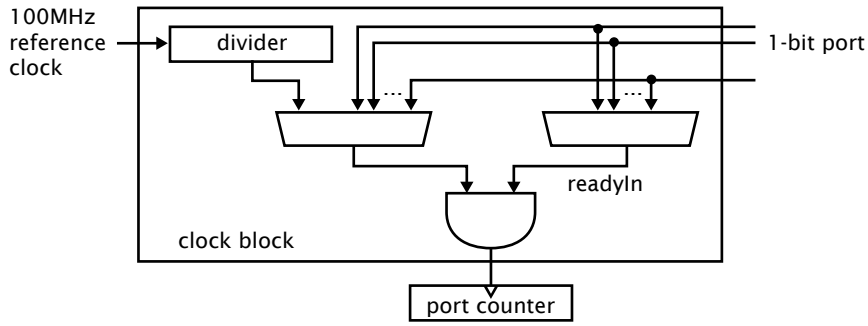


Figure 6: Clock block diagram

On reset, each port is connected to clock block 0, which runs from the processor reference clock.

7.5 Channels and Channel Ends

Logical cores communicate using point-to-point connections, formed between two channel ends. A channel-end is a resource on an xCORE tile, that is allocated by the program. Each channel-end has a unique system-wide identifier that comprises a unique number and their tile identifier. Data is transmitted to a channel-end by an output-instruction; and the other side executes an input-instruction. Data can be passed synchronously or asynchronously between the channel ends.

7.6 xCONNECT Switch and Links

XMOS devices provide a scalable architecture, where multiple xCORE devices can be connected together to form one system. Each xCORE device has an xCONNECT interconnect that provides a communication infrastructure for all tasks that run on the various xCORE tiles on the system.

The interconnect relies on a collection of switches and XMOS links. Each xCORE device has an on-chip switch that can set up circuits or route data. The switches are connected by xConnect Links. An XMOS link provides a physical connection between two switches. The switch has a routing algorithm that supports many different topologies, including lines, meshes, trees, and hypercubes.

The links operate in either 2 wires per direction or 5 wires per direction mode, depending on the amount of bandwidth required. Circuit switched, streaming and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between tiles , but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-L Link Performance and Design Guide, X2999.

If the ADC Is used, it requires a 100nF X5R or X7R ceramic decoupling capacitor placed as close as possible to the AVDD pin. Care should be taken to minimize noise on these inputs, and if necessary an extra 10uF decoupling capacitor and ferrite bead can be used to remove noise from this supply.

The crystal oscillator requires careful routing of the XI / XO nodes as these are high impedance and very noise sensitive. Hence, the traces should be as wide and short as possible, and routed over a continuous ground plane. They should not be routed near noisy supply lines or clocks. The device has a load capacitance of 18pF for the crystal. Care must be taken, so that the inductance and resistance of the ground returns from the capacitors to the ground of the device is minimized.

15.1 Land patterns and solder stencils

The land pattern recommendations in this document are based on a RoHS compliant process and derived, where possible, from the nominal *Generic Requirements for Surface Mount Design and Land Pattern Standards* IPC-7351B specifications. This standard aims to achieve desired targets of heel, toe and side fillets for solder-joints.

Solder paste and ground via recommendations are based on our engineering and development kit board production. They have been found to work and optimized as appropriate to achieve a high yield. These factors should be taken into account during design and manufacturing of the PCB.

The following land patterns and solder paste contains recommendations. Final land pattern and solder paste decisions are the responsibility of the customer. These should be tuned during manufacture to suit the manufacturing process.

The package is a 96 pin Ball Grid Array package on a 0.8mm pitch with 0.4mm balls.

An example land pattern is shown in Figure 20.

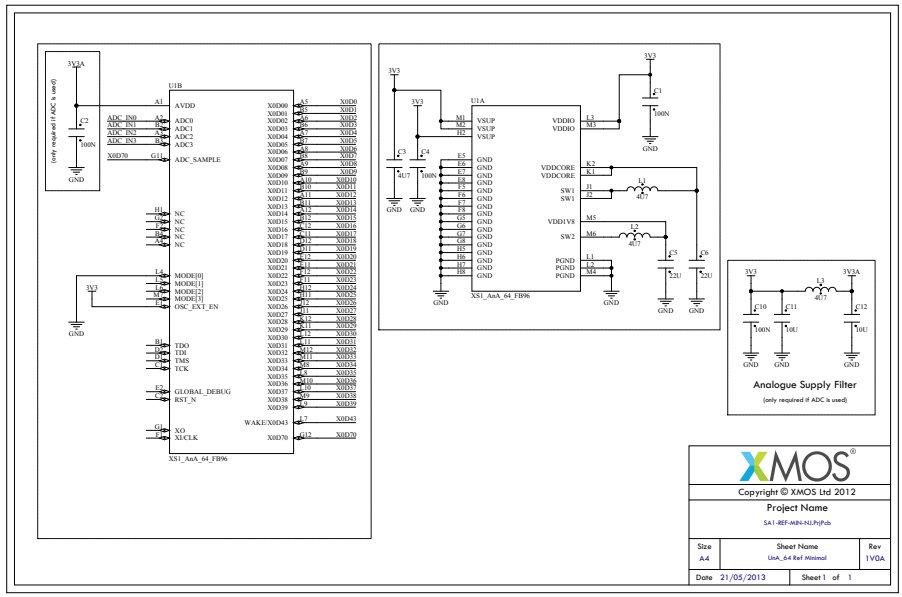
Pad widths and spacings are such that solder mask can still be applied between the pads using standard design rules. This is highly recommended to reduce solder shorts.

15.2 Ground and Thermal Vias

Vias next to each ground ball into the ground plane of the PCB are recommended for a low inductance ground connection and good thermal performance. Vias with with a 0.6mm diameter annular ring and a 0.3mm drill would be suitable.

15.3 Moisture Sensitivity

XMOS devices are, like all semiconductor devices, susceptible to moisture absorption. When removed from the sealed packaging, the devices slowly absorb moisture from the surrounding environment. If the level of moisture present in the device is too high during reflow, damage can occur due to the increased internal vapour



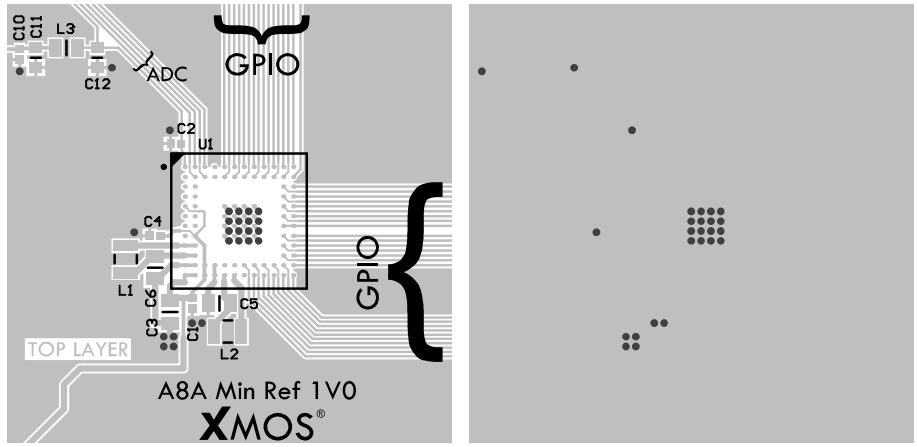


Figure 23: Example minimal system schematic, with top and bottom layout of a 2-layer PCB

17.3 DC2 Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDD1V8	1V8 Supply Voltage		1.80		V	
V(RIPPLE)	Ripple Voltage (peak to peak)		10	40	mV	
V(ACC)	Voltage Accuracy	-5		5	%	A
F(S)	Switching Frequency		1		MHz	
F(SVAR)	Variation in Switching Frequency	-10		10	%	
Effic	Efficiency		80		%	
PGT(HIGH)	Powergood Threshold (High)		95		%/VDD1V8	
PGT(LOW)	Powergood Threshold (Low)		80		%/VDD1V8	

Figure 26: DC2 characteristics

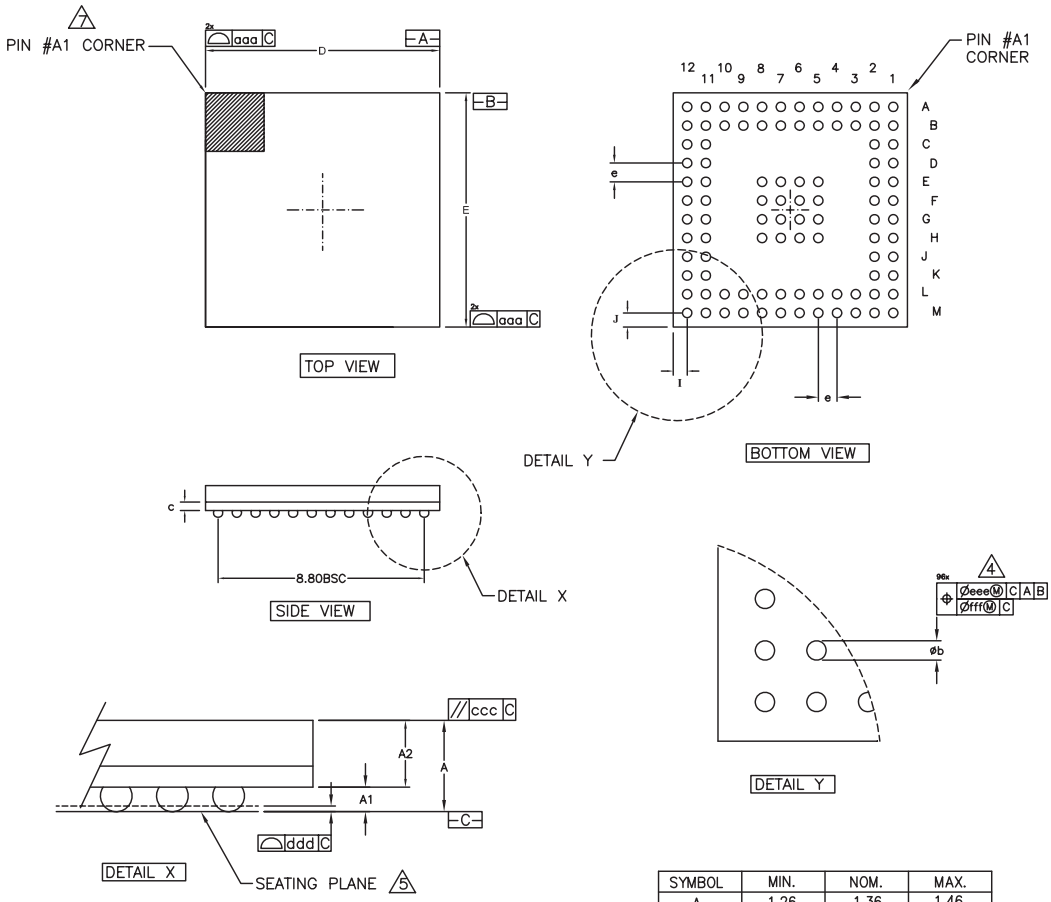
A If supplied externally.

17.4 ADC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
N	Resolution		12		bits	
Fs	Conversion Speed			1	MSPS	
Nch	Number of Channels		4			
Vin	Input Range	0		AVDD	V	
DNL	Differential Non Linearity	-1		1.5	LSB	
INL	Integral Non Linearity	-4		4	LSB	
E(GAIN)	Gain Error	-10		10	LSB	
E(OFFSET)	Offset Error	-3		3	mV	
T(PWRUP)	Power time for ADC Clock Fclk			7	1/Fclk	
ENOB	Effective Number of bits		10			

Figure 27: ADC characteristics

18 Package Information



SYMBOL	MIN.	NOM.	MAX.
A	1.26	1.36	1.46
A1	0.25	0.30	0.35
A2	1.01	1.06	1.11
D	9.90	10.00	10.10
E	9.90	10.00	10.10
I		0.60 REF.	
J		0.60 REF.	
M		10x10<DEPOPULATED>	
aaa			0.15
ccc			0.20
ddd			0.10
eee			0.15
fff			0.08
b	0.35	0.40	0.45
e		0.80 BSC.	
c		0.36 REF.	

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLE IS DEGREES.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE.
4. DEMENSIONS "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C .
5. PRIMARY DATUM C AND SEATING PLANE ARE DESIGNED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
7. A1 CORNER MUST BE IDENTIFIED BY LASER MARK.
8. PACKAGE DIMENSIONS CONFORM TO JEDEC REGISTRATION MO–275.

control-token 37	24-bit response channel-end identifier	8-bit register number	8-bit size	control-token 1

The response to the read message comprises either control token 3, data, and control-token 1 (for success), or control tokens 4 and 1 (for failure).

0x03: xCORE Tile boot status

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	RO		xCORE tile number on the switch.
15:9	RO	-	Reserved
8	RO		Set to 1 if boot from OTP is enabled.
7:0	RO		The boot mode pins MODE0, MODE1, ..., specifying the boot frequency, boot source, etc.

B.5 Security configuration: 0x05

Copy of the security register as read from OTP.

0x05: Security configuration

Bits	Perm	Init	Description
31:0	RO		Value.

B.6 Ring Oscillator Control: 0x06

There are four free-running oscillators that clock four counters. The oscillators can be started and stopped using this register. The counters should only be read when the ring oscillator is stopped. The counter values can be read using four subsequent registers. The ring oscillators are asynchronous to the xCORE tile clock and can be used as a source of random bits.

0x06: Ring Oscillator Control

Bits	Perm	Init	Description
31:2	RO	-	Reserved
1	RW	0	Set to 1 to enable the xCORE tile ring oscillators
0	RW	0	Set to 1 to enable the peripheral ring oscillators

B.7 Ring Oscillator Value: 0x07

This register contains the current count of the xCORE Tile Cell ring oscillator. This value is not reset on a system reset.

0x07: Ring Oscillator Value

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RO	-	Ring oscillator counter data.

C.21 SR of logical core 3: 0x63

0x63: SR of logical core 3

Bits	Perm	Init	Description
31:0	RO		Value.

C.22 SR of logical core 4: 0x64

0x64: SR of logical core 4

Bits	Perm	Init	Description
31:0	RO		Value.

C.23 SR of logical core 5: 0x65

0x65: SR of logical core 5

Bits	Perm	Init	Description
31:0	RO		Value.

C.24 SR of logical core 6: 0x66

0x66: SR of logical core 6

Bits	Perm	Init	Description
31:0	RO		Value.

C.25 SR of logical core 7: 0x67

0x67: SR of logical core 7

Bits	Perm	Init	Description
31:0	RO		Value.

C.26 Chanend status: 0x80 .. 0x9F

These registers record the status of each channel-end on the tile.

0x80 .. 0x9F: Chanend status

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:24	RO		00 - ChannelEnd, 01 - ERROR, 10 - PSCTL, 11 - Idle.
23:16	RO		Based on SRC_TARGET_TYPE value, it represents channelEnd ID or Idle status.
15:6	RO	-	Reserved
5:4	RO		Two-bit network identifier
3	RO	-	Reserved
2	RO		1 when the current packet is considered junk and will be thrown away.
1	RO	0	Set to 1 if the switch is routing data into the link, and if a route exists from another link.
0	RO	0	Set to 1 if the link is routing data into the switch, and if a route is created to another link on the switch.

E.8 Watchdog Disable: 0xD7

To enable the watchdog, write 0 to this register. To disable the watchdog, write the value 0x0D1SAB1E to this register.

0xD7: Watchdog Disable

Bits	Perm	Init	Description
31:0	RW	0x0D15AB1E	A value of 0x0D15AB1E written to this register resets and disables the watchdog timer.

F ADC Configuration

The device has a 12-bit Analogue to Digital Converter (ADC). It has multiple input pins, and on each positive clock edge on port 1I, it samples and converts a value on the next input pin. The data is transmitted to a channel-end that must be set on enabling the ADC input pin.

The *ADC* is peripheral 2. The control registers are accessed using 32-bit reads and writes (use `write_periph_32(device, 2, ...)` and `read_periph_32(device, 2, ...)` for reads and writes).

Figure 45: Summary

Number	Perm	Description
0x00	RW	ADC Control input pin 0
0x04	RW	ADC Control input pin 1
0x08	RW	ADC Control input pin 2
0x0C	RW	ADC Control input pin 3
0x20	RW	ADC General Control

F.1 ADC Control input pin 0: 0x00

Controls specific to ADC input pin 0.

0x00: ADC Control input pin 0

Bits	Perm	Init	Description
31:8	RW	0	The node and channel-end identifier to which data for this ADC input pin should be send to. This is the top 24 bits of the channel-end identifier as allocated on an xCORE Tile.
7:1	RO	-	Reserved
0	RW	0	Set to 1 to enable this input pin on the ADC.

I Real time clock Configuration

The *Real time clock* is peripheral 5. The control registers are accessed using 32-bit reads and writes (use `write_periph_32(device, 5, ...)` and `read_periph_32(device, 5, ...)` for reads and writes).

Figure 48: Summary

Number	Perm	Description
0x00	RW	Real time counter least significant 32 bits
0x04	RW	Real time counter most significant 32 bits

I.1 Real time counter least significant 32 bits: 0x00

This registers contains the lower 32-bits of the real-time counter.

0x00: Real time counter least significant 32 bits

Bits	Perm	Init	Description
31:0	RO	0	Least significant 32 bits of real-time counter.

I.2 Real time counter most significant 32 bits: 0x04

This registers contains the upper 32-bits of the real-time counter.

0x04: Real time counter most significant 32 bits

Bits	Perm	Init	Description
31:0	RO	0	Most significant 32 bits of real-time counter.

J Power control block Configuration

The *Power control block* is peripheral 6. The control registers are accessed using 32-bit reads and writes (use `write_periph_32(device, 6, ...)` and `read_periph_32(device, 6, ...)` for reads and writes).

Number	Perm	Description
0x00	RW	General control
0x04	RW	Time to wake-up, least significant 32 bits
0x08	RW	Time to wake-up, most significant 32 bits
0x0C	RW	Power supply states whilst ASLEEP
0x10	RW	Power supply states whilst WAKING1
0x14	RW	Power supply states whilst WAKING2
0x18	RW	Power supply states whilst AWAKE
0x1C	RW	Power supply states whilst SLEEPING1
0x20	RW	Power supply states whilst SLEEPING2
0x24	RW	Power sequence status
0x2C	RW	DCDC control
0x30	RW	Power supply status
0x34	RW	VDDCORE level control
0x40	RW	LDO5 level control

Figure 49: Summary

J.1 General control: 0x00

This register controls the basic settings for power modes.

0x00: General control

Bits	Perm	Init	Description
31:8	RO	-	Reserved
7	RW	0	By default, when waking up, the voltage levels stored in the LEVEL CONTROL registers are used. Set to 1 to use the power-on voltage levels.
6	WO		Set to 1 to re-apply the current contents of the AWAKE state. Use this when the program has changed the contents of the AWAKE state register. Self clearing.
5	RW	0	Set to 1 to use a 64-bit timer.
4	RW	0	Set to 1 to wake-up on the timer.
3	RW	1	If waking on the WAKE pin is enabled (see above), then by default the device wakes up when the WAKE pin is pulled high. Set to 0 to wake-up when the WAKE pin is pulled low.
2	RW	0	Set to 1 to wake-up when the WAKE pin is at the right level.
1	RW	0	Set to 1 to initiate sleep sequence - self clearing. Only set this bit when in AWAKE state.
0	RW	0	Sleep clock select. Set to 1 to use the default clock rather than the internal 31.25 kHz oscillator. Note: this bit is only effective in the ASLEEP state.

J.2 Time to wake-up, least significant 32 bits: 0x04

This register stores the time to wake-up. The value is only used if wake-up from the real-time clock is enabled, and the device is asleep.

0x04: Time to wake-up, least significant 32 bits

Bits	Perm	Init	Description
31:0	RW	0	Least significant 32 bits of time to wake-up.

J.3 Time to wake-up, most significant 32 bits: 0x08

This register stores the time to wake-up. The value is only used if wake-up from the real-time clock is enabled, if 64-bit comparisons are enabled, and the device is asleep. In most cases, 32-bit comparisons suffice.

0x18: Power supply states whilst AWAKE

Bits	Perm	Init	Description
31:15	RO	-	Reserved
14	RW	0	Set to 1 to disable clock to the xCORE Tile.
13:10	RO	-	Reserved
9	RW	0	Sets modulation used by DCDC2: 0: PWM modulation (max 475 mA) 1: PFM modulation (max 50 mA)
8	RW	0	Sets modulation used by DCDC1: 0: PWM modulation (max 700 mA) 1: PFM modulation (max 50 mA)
7:6	RO	-	Reserved
5	RW	1	Set to 1 to enable VOUT6 (IO supply).
4	RW	1	Set to 1 to enable LDO5 (core PLL supply).
3:2	RO	-	Reserved
1	RO	1	Set to 1 to enable DCDC2 (analogue supply).
0	RW	1	Set to 1 to enable DCDC1 (core supply).

J.8 Power supply states whilst SLEEPING1: 0x1C

This register controls what state the power control block should be in when in the SLEEPING1 state. It also defines the time that the system shall stay in this state.

0x24: Power sequence status

Bits	Perm	Init	Description
31:30	RO	-	Reserved
29	RO	0	1 if VOUT6 was enabled in the previous state.
28	RO	0	1 if LDO5 was enabled in the previous state.
27:26	RO	-	Reserved
25	RO	1	1 if DCDC2 was enabled in the previous state.
24	RO	0	1 if DCDC1 was enabled in the previous state.
23:19	RO	-	Reserved
18:16	RO		Current state of the power sequence state machine 0: Reset 1: Asleep 2: Waking 1 3: Waking 2 4: Awake Wait 5: Awake 6: Sleeping 1 7: Sleeping 2
15	RO	-	Reserved
14	RO	0	Set to 1 to disable clock to the xCORE Tile.
13:10	RO	-	Reserved
9	RO	0	Sets modulation used by DCDC2: 0: PWM modulation (max 475 mA) 1: PFM modulation (max 50 mA)
8	RO	0	Sets modulation used by DCDC1: 0: PWM modulation (max 700 mA) 1: PFM modulation (max 50 mA)
7:6	RO	-	Reserved
5	RO	0	Set to 1 to enable VOUT6 (IO supply).
4	RO	0	Set to 1 to enable LDO5 (core PLL supply).
3:2	RO	-	Reserved
1	RO	0	Set to 1 to enable DCDC2 (analogue supply).
0	RO	0	Set to 1 to enable DCDC1 (core supply).

J.11 DCDC control: 0x2C

This register controls the two DC-DC converters.

0x30: Power supply status

Bits	Perm	Init	Description
31:25	RO	-	Reserved
24	RO		1 if on-silicon oscillator is stable.
23:20	RO	-	Reserved
19	RO		1 if VDDPLL is good.
18:17	RO	-	Reserved
16	RO		1 if VDDCORE is good.
15:10	RO	-	Reserved
9	RO		1 if DCDC2 is in current limiting mode.
8	RO		1 if DCDC1 is in current limiting mode.
7:2	RO	-	Reserved
1	RO		1 if DCDC2 is in soft-start mode.
0	RO		1 if DCDC1 is in soft-start mode.

J.13 VDDCORE level control: 0x34

This register can be used to set the desired voltage on VDDCORE. If the level is to be raised or lowered, it should be raised in steps of no more than 10 mV per microsecond in order to prevent overshoot and undershoot. The default value depends on the MODE pins.

0x34: VDDCORE level control

Bits	Perm	Init	Description
31:7	RO	-	Reserved
6:0	RW	pin	The required voltage in 10 mV steps: 0: 0.60V 1: 0.61V 2: 0.62V ... 69: 1.29V 70: 1.30V

J.14 LDO5 level control: 0x40

This register can be used to set the desired voltage on LDO5. If the level is to be raised, it should be raised in steps of 1 (100 mV). The default value depends on the MODE pins.

K XMOS USB Interface

XMOS provides a low-level USB interface for connecting the device to a USB transceiver using the UTMI+ Low Pin Interface (ULPI). The ULPI signals must be connected to the pins named in Figure 50. Note also that some ports on the same tile are used internally and are not available for use when the USB driver is active (they are available otherwise).

Pin	Signal
X*n*D02	Unavailable when USB active
X*n*D03	
X*n*D04	
X*n*D05	
X*n*D06	
X*n*D07	
X*n*D08	
X*n*D09	

Pin	Signal
X*n*D12	ULPI_STP
X*n*D13	ULPI_NXT
X*n*D14	ULPI_DATA[0]
X*n*D15	ULPI_DATA[1]
X*n*D16	ULPI_DATA[2]
X*n*D17	ULPI_DATA[3]
X*n*D18	ULPI_DATA[4]
X*n*D19	ULPI_DATA[5]
X*n*D20	ULPI_DATA[6]
X*n*D21	ULPI_DATA[7]
X*n*D22	ULPI_DIR
X*n*D23	ULPI_CLK

Pin	Signal
X*n*D26	Unavailable when USB active
X*n*D27	
X*n*D28	
X*n*D29	
X*n*D30	
X*n*D31	
X*n*D32	
X*n*D33	

X*n*D37	Unavailable when USB active
X*n*D38	
X*n*D39	
X*n*D40	
X*n*D41	
X*n*D42	
X*n*D43	

Figure 50: ULPI signals provided by the XMOS USB driver

L Device Errata

This section describes minor operational differences from the data sheet and recommended workarounds. As device and documentation issues become known, this section will be updated the document revised.

To guarantee a logic low is seen on the pins DEBUG_N, MODE[3:0], TMS, TCK and TDI, the driving circuit should present an impedance of less than 100 Ω to ground. Usually this is not a problem for CMOS drivers driving single inputs. If one or more of these inputs are placed in parallel, however, additional logic buffers may be required to guarantee correct operation.

For static inputs tied high or low, the relevant input pin should be tied directly to GND or VDDIO.

N.4 JTAG, XScope, and debugging

- ☐ You have decided as to whether you need an XSYS header or not (Section M)
- ☐ If you included an XSYS header, you connected pin 3 to any MODE2/MODE3 pin that would otherwise be NC (Section M).
- ☐ If you have not included an XSYS header, you have devised a method to program the SPI-flash or OTP (Section M).

N.5 GPIO

- ☐ You have not mapped both inputs and outputs to the same multi-bit port.

N.6 Multi device designs

Skip this section if your design only includes a single XMOS device.

- ☐ One device is connected to a SPI flash for booting.
- ☐ Devices that boot from link have MODE2 grounded and MODE3 NC. These device must have link XLB connected to a device to boot from (see 9).
- ☐ If you included an XSYS header, you have included buffers for RST_N, TMS, TCK, MODE2, and MODE3 (Section L).

O PCB Layout Design Check List

☑ This section is a checklist for use by PCB designers using the XS1-A8A-64-FB96. Each of the following sections contains items to check for each design.

O.1 Ground Balls and Ground Plane

☐ There is one via for each ground ball to minimize impedance and conduct heat away from the device (Section 15.1).

☐ There are only few non-ground vias around the square of ground balls, to creating a good, solid, ground plane.

O.2 Power supply decoupling

☐ VSUP has a ceramic X5R or X7R bulk decoupler as close as possible to the VSUP and PGND (VDDCORE) pins; right next to the device (Section 15).

☐ The 1V0 decoupling cap is close to the VDDCORE and PGND pins (Section 15).

☐ The 1V8 decoupling cap is close to the VDD1V8 and PGND pins (Section 15).

☐ All PGND nets are connected together prior to connection to the main ground plane (Section 15).

An example PCB layout is shown in Section 16. Placing the decouplers too far away may lead to the device not coming up, or not operating properly.