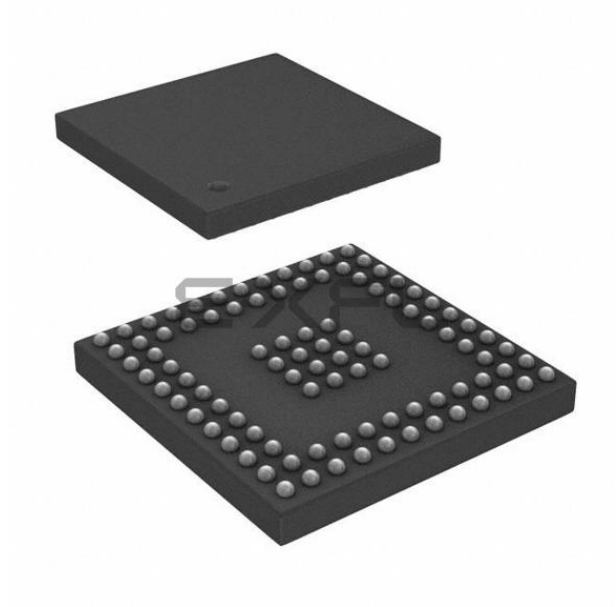

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | XCore |
| Core Size | 32-Bit 8-Core |
| Speed | 400MIPS |
| Connectivity | Configurable |
| Peripherals | - |
| Number of I/O | 42 |
| Program Memory Size | 64KB (16K x 32) |
| Program Memory Type | SRAM |
| EEPROM Size | - |
| RAM Size | - |
| Voltage - Supply (Vcc/Vdd) | 0.90V ~ 5.5V |
| Data Converters | A/D 4x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 96-LFBGA |
| Supplier Device Package | 96-FBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/xmos/xs1-a8a-64-fb96-i4 |

# 2 XS1-A8A-64-FB96 Features

- **Multicore Microcontroller with Advanced Multi-Core RISC Architecture**
  - Eight real-time logical cores
  - Core share up to 500 MIPS
  - Each logical core has:
    - Guaranteed throughput of between 1/4 and 1/8 of tile MIPS
    - 16x32bit dedicated registers
  - 159 high-density 16/32-bit instructions
    - All have single clock-cycle execution (except for divide)
    - 32x32→64-bit MAC instructions for DSP, arithmetic and user-definable cryptographic functions
- **12b 1MSPS 4-channel SAR Analog-to-Digital Converter**
- **1 x LDO**
- **2 x DC-DC converters and Power Management Unit**
- **Watchdog Timer**
- **Onchip clocks/oscillators**
  - Crystal oscillator
  - 20MHz/31kHz silicon oscillators
- **Programmable I/O**
  - 42 general-purpose I/O pins, configurable as input or output
    - Up to 16 x 1bit port, 6 x 4bit port, 3 x 8bit port, 1 x 16bit port
    - 2 xCONNECT links
  - Port sampling rates of up to 60 MHz with respect to an external clock
  - 32 channel ends for communication with other cores, on or off-chip
- **Memory**
  - 64KB internal single-cycle SRAM for code and data storage
  - 8KB internal OTP for application boot code
  - 128 bytes Deep Sleep Memory
- **Hardware resources**
  - 6 clock blocks
  - 10 timers
  - 4 locks
- **JTAG Module for On-Chip Debug**
- **Security Features**
  - Programming lock disables debug and prevents read-back of memory contents
  - AES bootloader ensures secrecy of IP held on external flash memory
- **Ambient Temperature Range**
  - Commercial qualification: 0°C to 70°C
  - Industrial qualification: -40°C to 85°C
- **Speed Grade**
  - 5: 500 MIPS
  - 4: 400 MIPS
- **Power Consumption (typical)**
  - 300 mW at 500 MHz (typical)
  - Sleep Mode: 500 µW
- **96-pin FBGA package 0.8 mm pitch**

# 3 Pin Configuration

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | AVDD | ADC0 | ADC2 | NC | 1A X0D00 | 4A X0D02 | 4B X0D04 | 4B X0D06 | 4A X0D08 | 1C X0D10 | 1E X0D12 | 4C X0D14 |
| B | TDO | ADC1 | ADC3 | NC | 1B X0D01 | 4A X0D03 | 4B X0D05 | 4B X0D07 | 4A X0D09 | 1D X0D11 | 1F X0D13 | 4C X0D15 |
| C | TCK | RST_N | | | | | | | | | 4D X0D17 | 4D X0D16 |
| D | TMS | TDI | | | | | | | | | 4D X0D19 | 4D X0D18 |
| E | OSC_ EXT_N | DEBUG_ N | | | GND | GND | GND | GND | | | 4C X0D21 | 4C X0D20 |
| F | XI/ CLK | NC | | | AVSS | GND | GND | GND | | | 1H X0D23 | 1G X0D22 |
| G | XO | NC | | | GND | GND | GND | GND | | | ADC_ SAMPLE | 32A X0D70 |
| H | NC | VSUP | | | GND | GND | GND | GND | | | 1J X0D25 | 1I X0D24 |
| J | SW1 | SW1 | | | | | | | | | 4E X0D27 | 4E X0D26 |
| K | VDDCORE | VDDCORE | | | | | | | | | 4F X0D29 | 4F X0D28 |
| L | PGND | PGND | VDDIO | MODE[0] | MODE[1] | MODE[2] | X0D43/ WAKE | 1L X0D35 | 1P X0D39 | 1N X0D37 | 4F X0D31 | 4F X0D30 |
| M | VSUP | VSUP | VDDIO | PGND | VDD1V8 | SW2 | MODE[3] | 1K X0D34 | 1O X0D38 | 1M X0D36 | 4E X0D33 | 4E X0D32 |

# 5 Example Application Diagram

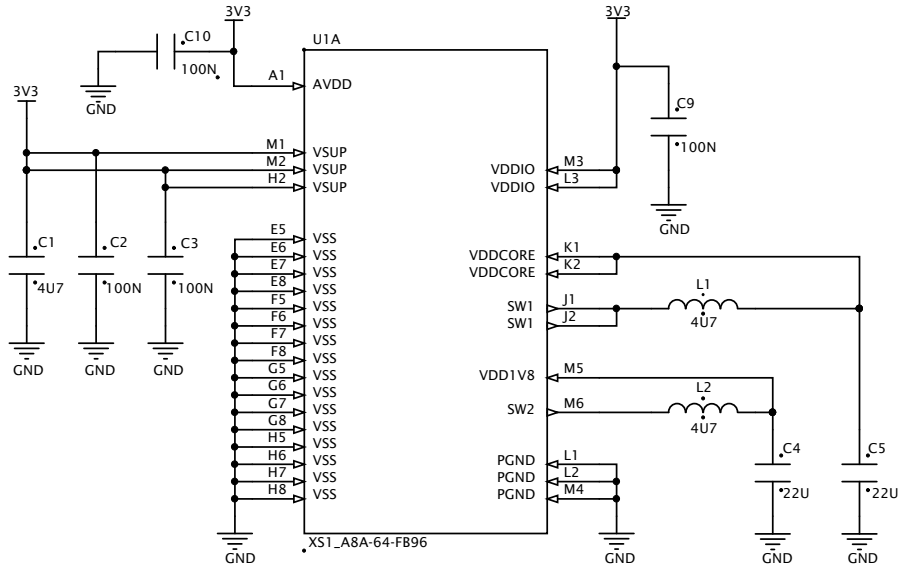



**Figure 2:** Simplified Reference Schematic

# 7 xCORE Tile Resources

## 7.1 Logical cores

The tile has 8 active logical cores, which issue instructions down a shared four-stage pipeline. Instructions from the active cores are issued round-robin. If up to four logical cores are active, each core is allocated a quarter of the processing cycles. If more than four logical cores are active, each core is allocated at least $1/n$ cycles (for $n$ cores). Figure 4 shows the guaranteed core performance depending on the number of cores used.

**Figure 4:** Logical core performance

| Speed grade | MIPS | Frequency | Minimum MIPS per core (for *n* cores) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 4 | 400 MIPS | 400 MHz | 100 | 100 | 100 | 100 | 80 | 67 | 57 | 50 |
| 5 | 500 MIPS | 500 MHz | 125 | 125 | 125 | 125 | 100 | 83 | 71 | 63 |

There is no way that the performance of a logical core can be reduced below these predicted levels. Because cores may be delayed on I/O, however, their unused processing cycles can be taken by other cores. This means that for more than four logical cores, the performance of each core is often higher than the predicted minimum but cannot be guaranteed.

The logical cores are triggered by events instead of interrupts and run to completion. A logical core can be paused to wait for an event.

## 7.2 xTIME scheduler

The xTIME scheduler handles the events generated by xCORE Tile resources, such as channel ends, timers and I/O pins. It ensures that all events are serviced and synchronized, without the need for an RTOS. Events that occur at the I/O pins are handled by the Hardware-Response ports and fed directly to the appropriate xCORE Tile. An xCORE Tile can also choose to wait for a specified time to elapse, or for data to become available on a channel.

Tasks do not need to be prioritised as each of them runs on their own logical xCORE. It is possible to share a set of low priority tasks on a single core using cooperative multitasking.

## 7.3 Hardware Response Ports

Hardware Response ports connect an xCORE tile to one or more physical pins and as such define the interface between hardware attached to the XS1-A8A-64-FB96, and the software running on it. A combination of 1bit, 4bit, 8bit, 16bit and 32bit ports are available. All pins of a port provide either output or input. Signals in different directions cannot be mapped onto the same port.

The port logic can drive its pins high or low, or it can sample the value on its pins, optionally waiting for a particular condition. Ports are accessed using dedicated instructions that are executed in a single processor cycle.

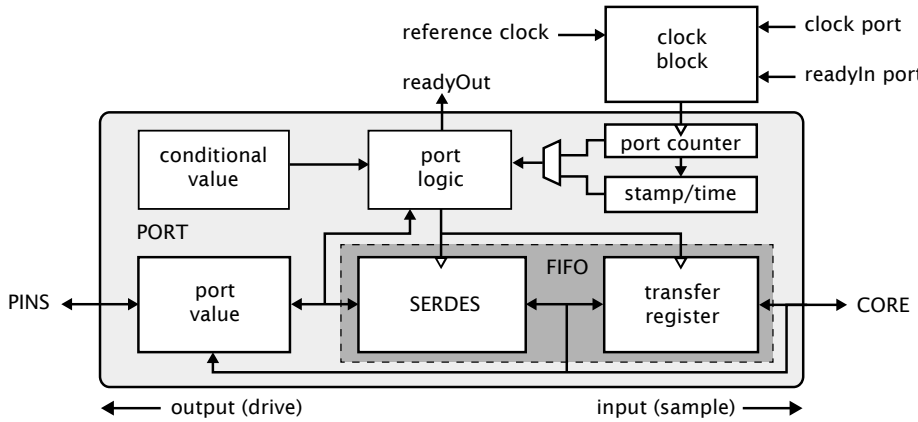



**Figure 5:** Port block diagram

Data is transferred between the pins and core using a FIFO that comprises a SERDES and transfer register, providing options for serialization and buffered data.

Each port has a 16-bit counter that can be used to control the time at which data is transferred between the port value and transfer register. The counter values can be obtained at any time to find out when data was obtained, or used to delay I/O until some time in the future. The port counter value is automatically saved as a timestamp, that can be used to provide precise control of response times.

The ports and xCONNECT links are multiplexed onto the physical pins. If an xConnect Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

## 7.4 Clock blocks

xCORE devices include a set of programmable clocks called clock blocks that can be used to govern the rate at which ports execute. Each xCORE tile has six clock blocks: the first clock block provides the tile reference clock and runs at a default frequency of 100MHz; the remaining clock blocks can be set to run at different frequencies.

A clock block can use a 1-bit port as its clock source allowing external application clocks to be used to drive the input and output interfaces.

In many cases I/O signals are accompanied by strobing signals. The xCORE ports can input and interpret strobe (known as readyIn and readyOut) signals generated by external sources, and ports can generate strobe signals to accompany output data.

# 12 Supervisor Logic

An independent supervisor circuit provides power-on-reset, brown-out, and watchdog capabilities. This facilitates the design of systems that fail gracefully, whilst keeping BOM costs down.

The reset supervisor holds the chip in reset until all power supplies are good. This provides a power-on-reset (POR). An external reset is optional and the pin RST_N can be left not-connected.

If at any time any of the power supplies drop because of too little supply or too high a demand, the power supervisor will bring the chip into reset until the power supplies have been restored. This will reboot the system as if a cold-start has happened.

The 16-bit watchdog timer provides 1ms accuracy and runs independently of the real-time counter. It can be programmed with a time-out of between 1 ms and 65 seconds (Appendix E). If the watchdog is not set before it times out, the XS1-A8A-64-FB96 is reset. On boot, the program can read a register to test whether the reset was due to the watchdog. The watchdog timer is only enabled and clocked whilst the processor is in the AWAKE power state.

# 13 Energy management

XS1-A8A-64-FB96 devices can be powered by:

- An external 5v core and 3.3v I/O supply.
- A single 3.3v supply.

## 13.1 DC-DC

XS1-A8A-64-FB96 devices include two DC-DC buck converters which can be configured to take input voltages between 3.3-5V power supply and output circuit voltages (nominally 1.8V and 1.0V) required by the analog peripherals and digital node.

## 13.2 Power mode controller

The device transitions through multiple states during the power-up and powerdown process.

The device is quiescent in the ASLEEP state, and is running in the AWAKE state. The other states allow a controlled transition between AWAKE and ASLEEP.

A transition from AWAKE state to ASLEEP state is instigated by a write to the general control register. Sleep requests must only be made in the AWAKE state.

A transition from the ASLEEP state into the AWAKE state is instigated by a wakeup request triggered by an input, or a timer. The device only responds to a wakeup

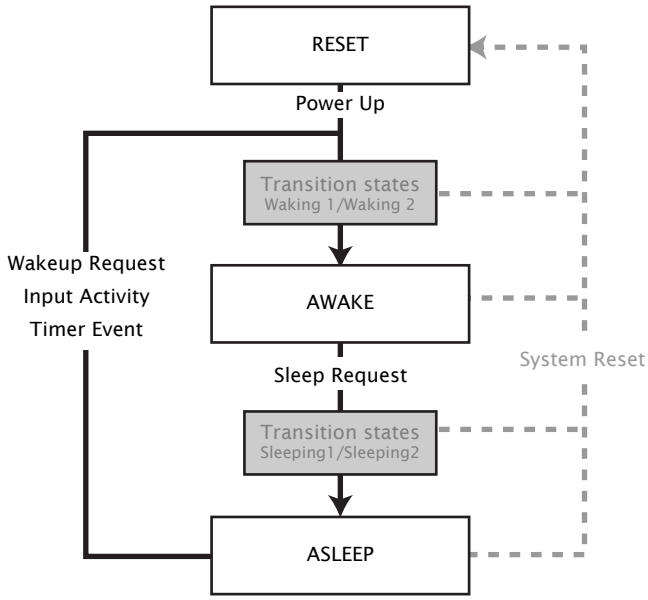



**Figure 14:** XS1-A8A-64-FB96 Power Up States and Transitions

stimulus in the ASLEEP state. If wakeup stimulus occurs whilst transitioning from AWAKE to ASLEEP, the appropriate response occurs when the ASLEEP state is reached.

Configuration is through a set of registers documented in Appendix J.

### 13.3 Deep Sleep Modes and Real-Time Counter

The normal mode in which the XS1-A8A-64-FB96 operates is the AWAKE mode. In this mode, all cores, memory, and peripherals operate as normal. To save power, the XS1-A8A-64-FB96 can be put into a deep sleep mode, called ASLEEP, where the digital node is powered down, and most peripherals are powered down. The XS1-A8A-64-FB96 will stay in the ASLEEP mode until one of two conditions:

1. An external pin is asserted or deasserted (set by the program);

2. The 64-bit real-time counter reaches a value set by the program; or

When the chip is awake, the real-time counter counts the number of clock ticks on the oscillator. As such, the real-time counter will run at a fixed ratio, but synchronously with the 100 MHz timers on the xCORE Tile. When asleep, the real-time counter can be automatically switched to the 31,250 Hz silicon oscillator to save power (see Appendix H). To ensure that the real-time counter increases linearly over time, a programmable value is added to the counter on every 31,250 Hz clock-tick. This means that the clock will run at a granularity of 31,250 Hz but still maintain real-time in terms of the frequency of the main oscillator. If an

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified in Figure 18. The OTP User ID field is read from bits [22:31] of the security register , *see* §10.1 (all zero on unprogrammed devices).

**Figure 18:** USERCODE return value

| Bit31 | | | | | | | | | | Usercode Register | | | | | | | | | | | | | | | | | | | | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OTP User ID | | | | | | | | | | Unused | | | | Silicon Revision | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | | | 0 | | | | 0 | | | | 2 | | | | C | | | | 0 | | | | 0 | | | | | | |

## 15 Board Integration

XS1-A8A-64-FB96 devices are optimized for layout on low cost PCBs using standard design rules. Careful layout is required to maximize the device performance. XMOS therefore recommends that the guidelines in this section are followed when laying out boards using the device.

The XS1-A8A-64-FB96 includes two DC-DC buck converters that take input voltages between 3.3-5V and output the 1.8V and 1.0V circuits required by the digital core and analogue peripherals. The DC-DC converters should have a 4.7uF X5R or X7R ceramic capacitor and a 100nF X5R or X7R ceramic capacitor on the VSUP input pins M1 and M2. These capacitors must be placed as close as possible to the those pins (within a maximum of 5mm), with the routing optimized to minimize the inductance and resistance of the traces.

The SW output pin must have an LC filter on the output with a 4.7uH inductor and 22uF X5R capacitor. The capacitor must have maximum ESR value of 0.015R, and the inductor should have a maximum DCR value of 0.07R, to meet the efficiency specifications of the DC-DC converter, although this requirement may be relaxed if a drop in efficiency is acceptable. A list of suggested inductors is in Figure 19.

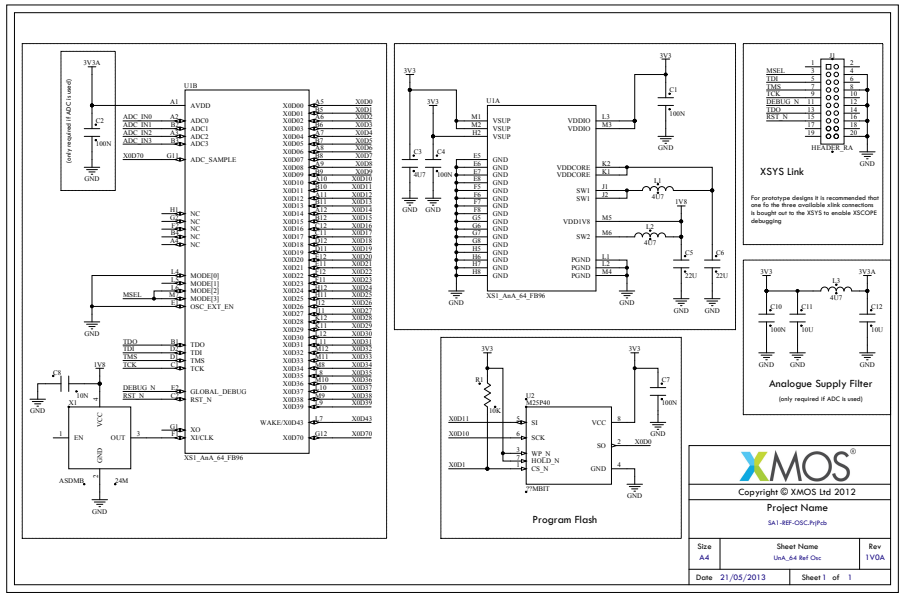
**Figure 19:** Example 4.7 $\mu$H inductors

| | Part number | Current | Max DCR | Package |
|---|---|---|---|---|
| Yuden | CBC2518T4R7M | 680 mA | 260 $m\Omega$ | 2518 (1007) |
| TDK | NLCV32T-4R7M-PFR | 620 mA | 200 $m\Omega$ | 3225 (1210) |
| Murata | LQM2HPN4R7MGC | 800 mA | 225 $m\Omega$ | 2520 (1008) |
| Sumida | 0420CDMCBDS-4R7MC | 3400 mA | 80 $m\Omega$ | 4.7 x 4.3 mm |
| Wurth | 744043004 | 1550 mA | 70 $m\Omega$ | 4.8 x 4.8 mm |
| Murata | LQH55DN4R7M03L | 2700 mA | 57 $m\Omega$ | 5750 (2220) |

The traces from the SW output pins to the inductor and from the output capacitor back to the VDD pins must be routed to minimize the coupling between them.

The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

The VDDIO supply to the XS1-A8A-64-FB96 requires a 100nF X5R or X7R ceramic decoupling capacitor placed as close as possible to the supply pins.



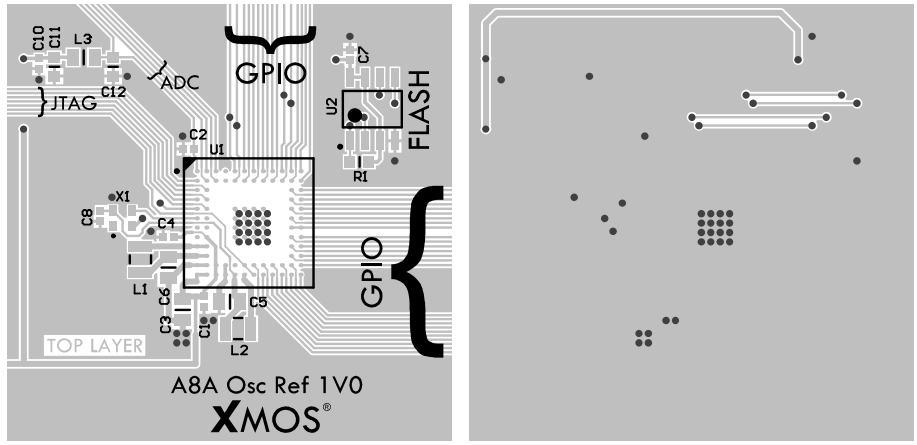




**Figure 22:** Example Oscillator schematic, with top and bottom layout of a 2-layer PCB

# 17 DC and Switching Characteristics

## 17.1 Operating Conditions

**Figure 24:** Operating conditions

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| VSUP | Power Supply (3.3V Mode) | 3.00 | 3.30 | 3.60 | V | |
| | Power Supply (5V Mode) | 4.50 | 5.00 | 5.50 | V | |
| VDDIO | I/O supply voltage | 3.00 | 3.30 | 3.60 | V | |
| AVDD | Analog Supply and Reference Voltage | 3.00 | 3.30 | 3.60 | V | |
| Cl | xCORE Tile I/O load capacitance | | | 25 | pF | |
| Ta | Ambient operating temperature (Commercial) | 0 | | 70 | °C | |
| | Ambient operating temperature (Industrial) | -40 | | 85 | °C | |
| Tj | Junction temperature | | | 125 | °C | |
| Tstg | Storage temperature | -65 | | 150 | °C | |

## 17.2 DC1 Characteristics

**Figure 25:** DC1 characteristics

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| VDDCORE | Tile Supply Voltage | 0.90 | 1.00 | 1.10 | V | |
| V(RIPPLE) | Ripple Voltage (peak to peak) | | 10 | 40 | mV | |
| V(ACC) | Voltage Accuracy | -5 | | 5 | % | A |
| F(S) | Switching Frequency | | 1 | | MHz | |
| F(SVAR) | Variation in Switching Frequency | -10 | | 10 | % | |
| Effic | Efficiency | | 80 | | % | |
| PGT(HIGH) | Powergood Threshold (High) | | 95 | | %/VDDCORE | |
| PGT(LOW) | Powergood Threshold (Low) | | 80 | | %/VDDCORE | |

A If supplied externally.

## 17.9 External Oscillator Characteristics

**Figure 32:** External oscillator characteristics

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| F(EXT) | External Frequency | | | 100 | MHz | |
| V(IH) | Input high voltage | 1.62 | | 1.98 | V | |
| V(IL) | Input low voltage | | | 0.4 | V | |

## 17.10 Power Consumption

**Figure 33:** xCORE Tile currents

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| P(AWAKE) | Active Power for awake states (Speed Grade 5) | TBC | 300 | TBC | mW | |
| | Active Power for awake states (Speed Grade 4) | TBC | 240 | TBC | mW | |
| P(SLEEP) | Power when asleep | TBC | 500 | TBC | µW | |

## 17.11 Clock

**Figure 34:** Clock

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| f(MAX) | Processor clock frequency (Speed Grade 5) | | | 500 | MHz | A |
| | Processor clock frequency (Speed Grade 4) | | | 400 | MHz | A |

A Assumes typical tile and I/O voltages with nominal activity.

## 17.12 Processor I/O AC Characteristics

**Figure 35:** I/O AC characteristics

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| T(XOVALID) | Input data valid window | 8 | | | ns | |
| T(XOINVALID) | Output data invalid window | 9 | | | ns | |
| T(XIFMAX) | Rate at which data can be sampled with respect to an external clock | | | 60 | MHz | |

The input valid window parameter relates to the capability of the device to capture data input to the chip with respect to an external clock source. It is calculated as the sum of the input setup time and input hold time with respect to the external clock as measured at the pins. The output invalid window specifies the time for which an output is invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the device provides functionality to delay the incoming clock with respect to the incoming data.

Information on interfacing to high-speed synchronous interfaces can be found in the XS1 Port I/O Timing document, X5821.

**0x03:** xCORE Tile boot status

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:24 | RO | - | Reserved |
| 23:16 | RO | | xCORE tile number on the switch. |
| 15:9 | RO | - | Reserved |
| 8 | RO | | Set to 1 if boot from OTP is enabled. |
| 7:0 | RO | | The boot mode pins MODE0, MODE1, ..., specifying the boot frequency, boot source, etc. |

## B.5 Security configuration: 0x05

Copy of the security register as read from OTP.

**0x05:** Security configuration

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | | Value. |

## B.6 Ring Oscillator Control: 0x06

There are four free-running oscillators that clock four counters. The oscillators can be started and stopped using this register. The counters should only be read when the ring oscillator is stopped. The counter values can be read using four subsequent registers. The ring oscillators are asynchronous to the xCORE tile clock and can be used as a source of random bits.

**0x06:** Ring Oscillator Control

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:2 | RO | - | Reserved |
| 1 | RW | 0 | Set to 1 to enable the xCORE tile ring oscillators |
| 0 | RW | 0 | Set to 1 to enable the peripheral ring oscillators |

## B.7 Ring Oscillator Value: 0x07

This register contains the current count of the xCORE Tile Cell ring oscillator. This value is not reset on a system reset.

**0x07:** Ring Oscillator Value

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:16 | RO | - | Reserved |
| 15:0 | RO | - | Ring oscillator counter data. |

0x15: Debug interrupt type

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:18 | RO | - | Reserved |
| 17:16 | DRW | | If the debug interrupt was caused by a hardware breakpoint or hardware watchpoint, this field contains the number of the breakpoint or watchpoint. If multiple breakpoints or watchpoints trigger at once, the lowest number is taken. |
| 15:8 | DRW | | If the debug interrupt was caused by a logical core, this field contains the number of that core. Otherwise this field is 0. |
| 7:3 | RO | - | Reserved |
| 2:0 | DRW | 0 | Indicates the cause of the debug interrupt<br>1: Host initiated a debug interrupt through JTAG<br>2: Program executed a DCALL instruction<br>3: Instruction breakpoint<br>4: Data watch point<br>5: Resource watch point |

## B.17 Debug interrupt data: 0x16

On a data watchpoint, this register contains the effective address of the memory operation that triggered the debugger. On a resource watchpoint, it countains the resource identifier.

0x16: Debug interrupt data

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | DRW | | Value. |

## B.18 Debug core control: 0x18

This register enables the debugger to temporarily disable logical cores. When returning from the debug interrupts, the cores set in this register will not execute. This enables single stepping to be implemented.

0x18: Debug core control

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:8 | RO | - | Reserved |
| 7:0 | DRW | | 1-hot vector defining which logical cores are stopped when not in debug mode. Every bit which is set prevents the respective logical core from running. |

**0x80 .. 0x83:** Resources breakpoint mask

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | DRW | | Value. |

## B.26 Resources breakpoint value: 0x90 .. 0x93

This set of registers contains the value for the four resource watchpoints.

**0x90 .. 0x93:** Resources breakpoint value

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | DRW | | Value. |

## B.27 Resources breakpoint control register: 0x9C .. 0x9F

This set of registers controls each of the four resource watchpoints.

**0x9C .. 0x9F:** Resources breakpoint control register

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:24 | RO | - | Reserved |
| 23:16 | DRW | 0 | A bit for each logical core in the tile allowing the breakpoint to be enabled individually for each logical core. |
| 15:2 | RO | - | Reserved |
| 1 | DRW | 0 | By default, resource watchpoints trigger when the resource id masked with the set Mask equals the Value. If set to 1, resource watchpoints trigger when the resource id masked with the set Mask is not equal to the Value. |
| 0 | DRW | 0 | When 1 the instruction breakpoint is enabled. |

### C.11 PC of logical core 1: 0x41

**0x41:** PC of logical core 1

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | | Value. |

### C.12 PC of logical core 2: 0x42

**0x42:** PC of logical core 2

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | | Value. |

### C.13 PC of logical core 3: 0x43

**0x43:** PC of logical core 3

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | | Value. |

### C.14 PC of logical core 4: 0x44

**0x44:** PC of logical core 4

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | | Value. |

### C.15 PC of logical core 5: 0x45

**0x45:** PC of logical core 5

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | | Value. |

### C.21 SR of logical core 3: 0x63

**0x63:** SR of logical core 3

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | | Value. |

### C.22 SR of logical core 4: 0x64

**0x64:** SR of logical core 4

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | | Value. |

### C.23 SR of logical core 5: 0x65

**0x65:** SR of logical core 5

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | | Value. |

### C.24 SR of logical core 6: 0x66

**0x66:** SR of logical core 6

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | | Value. |

### C.25 SR of logical core 7: 0x67

**0x67:** SR of logical core 7

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | | Value. |

### C.26 Chanend status: 0x80 .. 0x9F

These registers record the status of each channel-end on the tile.

0x0C: Directions 0-7

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:28 | RW | 0 | The direction for packets whose first mismatching bit is 7. |
| 27:24 | RW | 0 | The direction for packets whose first mismatching bit is 6. |
| 23:20 | RW | 0 | The direction for packets whose first mismatching bit is 5. |
| 19:16 | RW | 0 | The direction for packets whose first mismatching bit is 4. |
| 15:12 | RW | 0 | The direction for packets whose first mismatching bit is 3. |
| 11:8 | RW | 0 | The direction for packets whose first mismatching bit is 2. |
| 7:4 | RW | 0 | The direction for packets whose first mismatching bit is 1. |
| 3:0 | RW | 0 | The direction for packets whose first mismatching bit is 0. |

## D.9 Directions 8-15: 0x0D

This register contains eight directions, for packets with a mismatch in bits 15..8 of the node-identifier. The direction in which a packet will be routed is goverened by the most significant mismatching bit.

0x0D: Directions 8-15

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:28 | RW | 0 | The direction for packets whose first mismatching bit is 15. |
| 27:24 | RW | 0 | The direction for packets whose first mismatching bit is 14. |
| 23:20 | RW | 0 | The direction for packets whose first mismatching bit is 13. |
| 19:16 | RW | 0 | The direction for packets whose first mismatching bit is 12. |
| 15:12 | RW | 0 | The direction for packets whose first mismatching bit is 11. |
| 11:8 | RW | 0 | The direction for packets whose first mismatching bit is 10. |
| 7:4 | RW | 0 | The direction for packets whose first mismatching bit is 9. |
| 3:0 | RW | 0 | The direction for packets whose first mismatching bit is 8. |

## D.10 DEBUG_N configuration: 0x10

Configures the behavior of the DEBUG_N pin.

0x10: DEBUG_N configuration

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:2 | RO | - | Reserved |
| 1 | RW | 0 | Set to 1 to enable signals on DEBUG_N to generate DCALL on the core. |
| 0 | RW | 0 | When set to 1, the DEBUG_N wire will be pulled down when the node enters debug mode. |

### D.13 PLink status and network: 0x40 .. 0x43

These registers contain status information and the network number that each processor-link belongs to.

**0x40 .. 0x43:** PLink status and network

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:26 | RO | - | Reserved |
| 25:24 | RO | | If this link is currently routing data into the switch, this field specifies the type of link that the data is routed to:<br>0: plink<br>1: external link<br>2: internal control link |
| 23:16 | RO | 0 | If the link is routing data into the switch, this field specifies the destination link number to which all tokens are sent. |
| 15:6 | RO | - | Reserved |
| 5:4 | RW | 0 | Determines the network to which this link belongs, set for quality of service. |
| 3 | RO | - | Reserved |
| 2 | RO | 0 | Set to 1 if the current packet is junk and being thrown away. A packet is considered junk if, for example, it is not routable. |
| 1 | RO | 0 | Set to 1 if the switch is routing data into the link, and if a route exists from another link. |
| 0 | RO | 0 | Set to 1 if the link is routing data into the switch, and if a route is created to another link on the switch. |

### D.14 Link configuration and initialization: 0x80 .. 0x87

These registers contain configuration and debugging information specific to external links. The link speed and width can be set, the link can be initialized, and the link status can be monitored. The registers control links C, D, A, B, G, H, E, and F in that order.

# I Real time clock Configuration

The *Real time clock* is peripheral 5. The control registers are accessed using 32-bit reads and writes (use `write_periph_32(device, 5, ...)` and `read_periph_32(device, 5, ...)` for reads and writes).

**Figure 48: Summary**

| Number | Perm | Description |
|---|---|---|
| 0x00 | RW | Real time counter least significant 32 bits |
| 0x04 | RW | Real time counter most significant 32 bits |

## I.1 Real time counter least significant 32 bits: 0x00

This registers contains the lower 32-bits of the real-time counter.

**0x00: Real time counter least significant 32 bits**

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | 0 | Least significant 32 bits of real-time counter. |

## I.2 Real time counter most significant 32 bits: 0x04

This registers contains the upper 32-bits of the real-time counter.

**0x04: Real time counter most significant 32 bits**

| Bits | Perm | Init | Description |
|---|---|---|---|
| 31:0 | RO | 0 | Most significant 32 bits of real-time counter. |

# J Power control block Configuration

The *Power control block* is peripheral 6. The control registers are accessed using 32-bit reads and writes (use `write_periph_32(device, 6, ...)` and `read_periph_32(device, 6, ...)` for reads and writes).

| Number | Perm | Description |
|---|---|---|
| 0x00 | RW | General control |
| 0x04 | RW | Time to wake-up, least significant 32 bits |
| 0x08 | RW | Time to wake-up, most significant 32 bits |
| 0x0C | RW | Power supply states whilst ASLEEP |
| 0x10 | RW | Power supply states whilst WAKING1 |
| 0x14 | RW | Power supply states whilst WAKING2 |
| 0x18 | RW | Power supply states whilst AWAKE |
| 0x1C | RW | Power supply states whilst SLEEPING1 |
| 0x20 | RW | Power supply states whilst SLEEPING2 |
| 0x24 | RW | Power sequence status |
| 0x2C | RW | DCDC control |
| 0x30 | RW | Power supply status |
| 0x34 | RW | VDDCORE level control |
| 0x40 | RW | LDO5 level control |

**Figure 49:** Summary

## J.1 General control: 0x00

This register controls the basic settings for power modes.