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Details

Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	64MHz
Connectivity	ASC, CANbus, EBI/EMI, I ² C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	144-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f273z4q3

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Table 2. Pin description (continued)

Symbol	Pin	Type	Function		
P4.0 –P4.7	85-92	I/O	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. The input threshold is selectable (TTL or CMOS). Port 4.4, 4.5, 4.6 and 4.7 outputs can be configured as push-pull or open drain drivers. In case of an external bus configuration, Port 4 can be used to output the segment address lines:		
	85	O	P4.0	A16	Segment address line
	86	O	P4.1	A17	Segment address line
	87	O	P4.2	A18	Segment address line
	88	O	P4.3	A19	Segment address line
	89	O	P4.4	A20	Segment address line
		I		CAN2_RxD	CAN2: receive data input
		I/O		SCL	I ² C Interface: serial clock
	90	O	P4.5	A21	Segment address line
		I		CAN1_RxD	CAN1: receive data input
		I		CAN2_RxD	CAN2: receive data input
	91	O	P4.6	A22	Segment address line
		O		CAN1_TxD	CAN1: transmit data output
		O		CAN2_TxD	CAN2: transmit data output
	92	O	P4.7	A23	Most significant segment address line
		O		CAN2_TxD	CAN2: transmit data output
		I/O		SDA	I ² C Interface: serial data
$\overline{RD}$	95	O	External memory read strobe. $\overline{RD}$ is activated for every external instruction or data read access.		
$\overline{WR}/\overline{WRL}$	96	O	External memory write strobe. In $\overline{WR}$ -mode this pin is activated for every external data write access. In $\overline{WRL}$ mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in the SYSCON register for mode selection.		
$\overline{READY}/\overline{READY}$	97	I	Ready input. The active level is programmable. When the ready function is enabled, the selected inactive level at this pin, during an external memory access, will force the insertion of waitstate cycles until the pin returns to the selected active level.		
ALE	98	O	Address latch enable output. In case of use of external addressing or of multiplexed mode, this signal is the latch command of the address lines.		

7.2 Instruction set summary

The [Table 28](#) lists the instructions of the ST10F273Z4. The detailed description of each instruction can be found in the “ST10 Family Programming Manual”.

Table 28. Standard instruction set summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bit-wise AND, (word/byte operands)	2 / 4
OR(B)	Bit-wise OR, (word/byte operands)	2 / 4
XOR(B)	Bit-wise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bit-wise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4

13 Parallel ports

13.1 Introduction

The ST10F273Z4 MCU provides up to 111 I/O lines with programmable features. These capabilities bring very flexible adaptation of this MCU to wide range of applications.

ST10F273Z4 has nine groups of I/O lines gathered as follows:

- Port 0 is a two time 8-bit port named P0L (Low as less significant byte) and P0H (high as most significant byte)
- Port 1 is a two time 8-bit port named P1L and P1H
- Port 2 is a 16-bit port
- Port 3 is a 15-bit port (P3.14 line is not implemented)
- Port 4 is a 8-bit port
- Port 5 is a 16-bit port input only
- Port 6, Port 7 and Port 8 are 8-bit ports

These ports may be used as general purpose bidirectional input or output, software controlled with dedicated registers.

For example, the output drivers of six of the ports (2, 3, 4, 6, 7, 8) can be configured (bit-wise) for push-pull or open drain operation using ODPx registers.

The input threshold levels are programmable (TTL/CMOS) for all the ports. The logic level of a pin is clocked into the input latch once per state time, regardless whether the port is configured for input or output. The threshold is selected with PICON and XPICON registers control bits.

A write operation to a port pin configured as an input causes the value to be written into the port output latch, while a read operation returns the latched state of the pin itself. A read-modify-write operation reads the value of the pin, modifies it, and writes it back to the output latch.

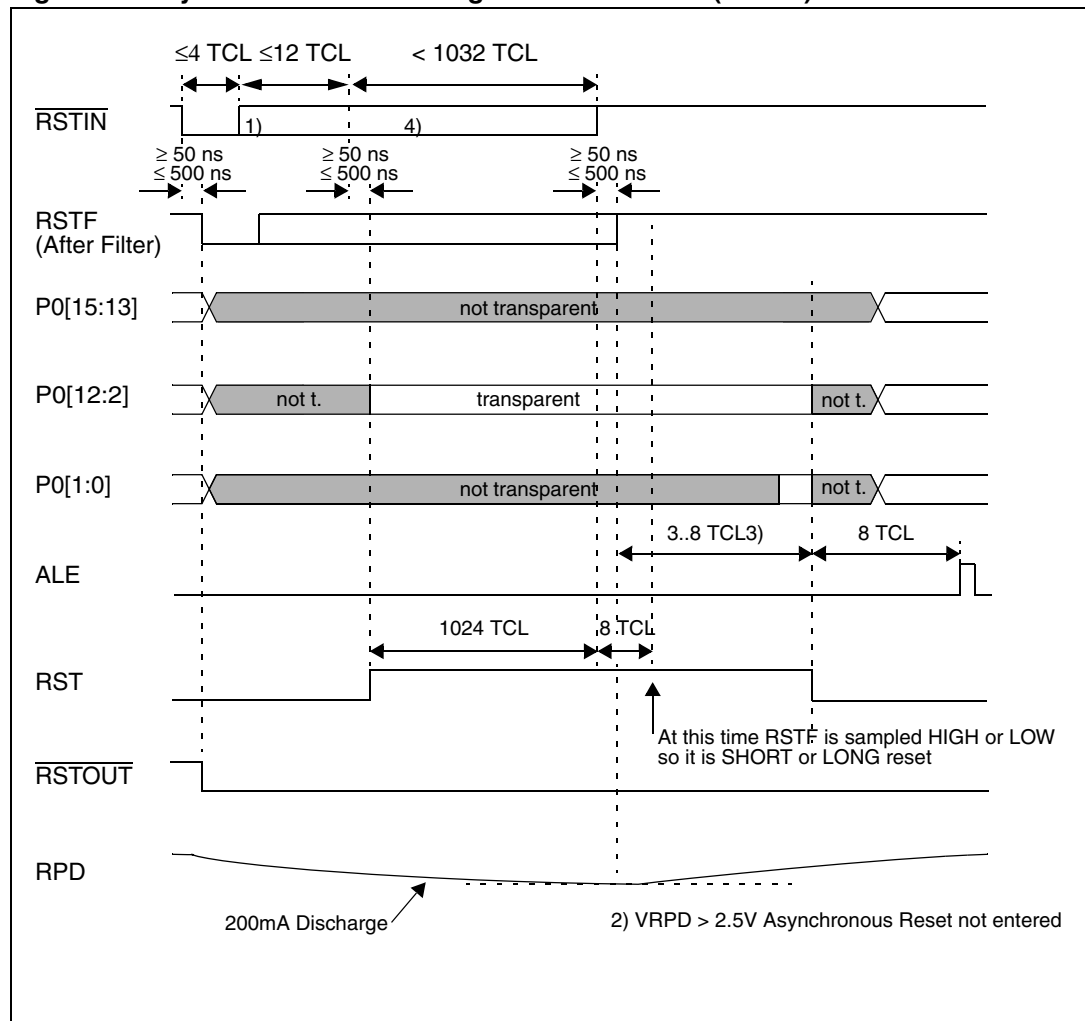
Writing to a pin configured as an output (DPx.y='1') causes the output latch and the pin to have the written value, since the output buffer is enabled. Reading this pin returns the value of the output latch. A read-modify-write operation reads the value of the output latch, modifies it, and writes it back to the output latch, thus also modifying the level at the pin.

I/O lines support an alternate function which is detailed in the following description of each port.

sufficient: anyway, a maximum of 100nF on V₁₈ pin should not generate problems of over-current (higher value is allowed if current is limited by the external hardware). External current limitation is anyway recommended also to avoid risks of damage in case of temporary short between V₁₈ and ground: the internal 1.8V drivers are sized to drive currents of several tens of Ampere, so the current shall be limited by the external hardware. The limit of current is imposed by power dissipation considerations (Refer to Electrical Characteristics Section).

In next Figures 15 and 16 Asynchronous Power-on timing diagrams are reported, respectively with boot from internal or external memory, highlighting the reset phase extension introduced by the embedded FLASH module when selected.

Note: Never power the device without keeping $\overline{RSTIN}$ pin grounded: the device could enter in unpredictable states, risking also permanent damages.

Figure 20. Synchronous short / long hardware RESET ($\overline{EA} = 0$)

Warning: During power-off phase, it is important that the external hardware maintains a stable ground level on $\overline{\text{RSTIN}}$ pin, without any glitch, in order to avoid spurious exiting from reset status with unstable power supply.

21.3.2 Exiting stand-by mode

After the system has entered the Stand-by mode, the procedure to exit this mode consists of a standard Power-on sequence, with the only difference that the RAM is already powered through $V_{18\text{SB}}$ internal reference (derived from V_{STBY} pin external voltage).

It is recommended to held the device under RESET ($\overline{\text{RSTIN}}$ pin forced low) until external V_{DD} voltage pin is stable. Even though, at the very beginning of the power-on phase, the device is maintained under reset by the internal low voltage detector circuit (implemented inside the main voltage regulator) till the internal V_{18} becomes higher than about 1.0V, **there is no warranty that the device stays under reset status if $\overline{\text{RSTIN}}$ is at high level during power ramp up. So, it is important the external hardware is able to guarantee a stable ground level on $\overline{\text{RSTIN}}$ along the power-on phase, without any temporary glitch.**

The external hardware shall be responsible to drive low the $\overline{\text{RSTIN}}$ pin until the V_{DD} is stable, even though the internal LVD is active.

Once the internal Reset signal goes low, the RAM (still frozen) power supply is switched to the main V_{18} .

At this time, everything becomes stable, and the execution of the initialization routines can start: XRAM2EN bit can be set, enabling the RAM.

21.3.3 Real-time clock and stand-by mode

When Stand-by mode is entered (turning off the main supply V_{DD}), the Real-Time Clock counting can be maintained running in case the on-chip 32 kHz oscillator is used to provide the reference to the counter. This is not possible if the main oscillator is used as reference for the counter: Being the main oscillator powered by V_{DD} , once this is switched off, the oscillator is stopped.

22 Programmable output clock divider

A specific register mapped on the XBUS allows to choose the division factor on the CLKOUT signal (P3.15). This register is mapped on X-Miscellaneous memory address range.

When CLKOUT function is enabled by setting bit CLKEN of register SYSCON, by default the CPU clock is output on P3.15. Setting bit XMISCEN of register XPERCON and bit XPEN of register SYSCON, it is possible to program the clock prescaling factor: in this way on P3.15 a prescaled value of the CPU clock can be output.

When CLKOUT function is not enabled (bit CLKEN of register SYSCON cleared), P3.15 does not output any clock signal, even though XCLKOUTDIV register is programmed.

Table 54. List of special function registers (continued)

Name		Physical address		8-bit address	Description	Reset value
DP0H	b	F102h	E	81h	P0h direction control register	- - 00h
DP1L	b	F104h	E	82h	P1L direction control register	- - 00h
DP1H	b	F106h	E	83h	P1h direction control register	- - 00h
DP2	b	FFC2h		E1h	Port 2 direction control register	0000h
DP3	b	FFC6h		E3h	Port 3 direction control register	0000h
DP4	b	FFCAh		E5h	Port 4 direction control register	- - 00h
DP6	b	FFCEh		E7h	Port 6 direction control register	- - 00h
DP7	b	FFD2h		E9h	Port 7 direction control register	- - 00h
DP8	b	FFD6h		EBh	Port 8 direction control register	- - 00h
DPP0		FE00h		00h	CPU data page pointer 0 register (10-bit)	0000h
DPP1		FE02h		01h	CPU data page pointer 1 register (10-bit)	0001h
DPP2		FE04h		02h	CPU data page pointer 2 register (10-bit)	0002h
DPP3		FE06h		03h	CPU data page pointer 3 register (10-bit)	0003h
EMUCON		FE0Ah		05h	Emulation control register	- - XXh
EXICON	b	F1C0h	E	E0h	External interrupt control register	0000h
EXISEL	b	F1DAh	E	EDh	External interrupt source selection register	0000h
IDCHIP		F07Ch	E	3Eh	Device identifier register (n is the device revision)	114nh
IDMANUF		F07Eh	E	3Fh	Manufacturer identifier register	0403h
IDMEM		F07Ah	E	3Dh	On-chip memory identifier register	30D0h
IDPROG		F078h	E	3Ch	Programming voltage identifier register	0040h
IDX0	b	FF08h		84h	MAC unit address pointer 0	0000h
IDX1	b	FF0Ah		85h	MAC unit address pointer 1	0000h
MAH		FE5Eh		2Fh	MAC unit accumulator - high word	0000h
MAL		FE5Ch		2Eh	MAC unit accumulator - low word	0000h
MCW	b	FFDCh		EEh	MAC unit control word	0000h
MDC	b	FF0Eh		87h	CPU multiply divide control register	0000h
MDH		FE0Ch		06h	CPU multiply divide register – high word	0000h
MDL		FE0Eh		07h	CPU multiply divide register – low word	0000h
MRW	b	FFDAh		EDh	MAC unit repeat word	0000h
MSW	b	FFDEh		EFh	MAC unit status word	0200h
ODP2	b	F1C2h	E	E1h	Port 2 open drain control register	0000h
ODP3	b	F1C6h	E	E3h	Port 3 open drain control register	0000h
ODP4	b	F1CAh	E	E5h	Port 4 open drain control register	- - 00h
ODP6	b	F1CEh	E	E7h	Port 6 open drain control register	- - 00h

Table 54. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
PW1	FE32h	19h	PWM module pulse width register 1	0000h
PW2	FE34h	1Ah	PWM module pulse width register 2	0000h
PW3	FE36h	1Bh	PWM module pulse width register 3	0000h
PWMCON0 b	FF30h	98h	PWM module control register 0	0000h
PWMCON1 b	FF32h	99h	PWM module control register 1	0000h
PWMIC b	F17Eh E	BFh	PWM module interrupt control register	- - 00h
QR0	F004h E	02h	MAC unit offset register r0	0000h
QR1	F006h E	03h	MAC unit offset register R1	0000h
QX0	F000h E	00h	MAC unit offset register X0	0000h
QX1	F002h E	01h	MAC unit offset register X1	0000h
RP0H b	F108h E	84h	System start-up configuration register (read only)	- - XXh
S0BG	FEB4h	5Ah	Serial channel 0 baud rate generator reload register	0000h
S0CON b	FFB0h	D8h	Serial channel 0 control register	0000h
S0EIC b	FF70h	B8h	Serial channel 0 error interrupt control register	- - 00h
S0RBUF	FEB2h	59h	Serial channel 0 receive buffer register (read only)	- - XXh
S0RIC b	FF6Eh	B7h	Serial channel 0 receive interrupt control register	- - 00h
S0TBIC b	F19Ch E	CEh	Serial channel 0 transmit buffer interrupt control reg.	- - 00h
S0TBUF	FEB0h	58h	Serial channel 0 transmit buffer register (write only)	0000h
S0TIC b	FF6Ch	B6h	Serial channel 0 transmit interrupt control register	- - 00h
SP	FE12h	09h	CPU system stack pointer register	FC00h
SSCBR	F0B4h E	5Ah	SSC Baud rate register	0000h
SSCCON b	FFB2h	D9h	SSC control register	0000h
SSCEIC b	FF76h	BBh	SSC error interrupt control register	- - 00h
SSCRB	F0B2h E	59h	SSC receive buffer (read only)	XXXXh
SSCRIC b	FF74h	BAh	SSC receive interrupt control register	- - 00h
SSCTB	F0B0h E	58h	SSC transmit buffer (write only)	0000h
SSCTIC b	FF72h	B9h	SSC transmit interrupt control register	- - 00h
STKOV	FE14h	0Ah	CPU stack overflow pointer register	FA00h
STKUN	FE16h	0Bh	CPU stack underflow pointer register	FC00h
SYSCON b	FF12h	89h	CPU system configuration register	0xx0h ¹⁾
T0	FE50h	28h	CAPCOM timer 0 register	0000h
T01CON b	FF50h	A8h	CAPCOM timer 0 and timer 1 control register	0000h
T0IC b	FF9Ch	CEh	CAPCOM timer 0 interrupt control register	- - 00h
T0REL	FE54h	2Ah	CAPCOM timer 0 reload register	0000h

Table 63. Thermal characteristics

Symbol	Description	Value (typical)	Unit
Θ_{JA}	Thermal resistance junction-ambient		
	PQFP 144 - 28 x 28 x 3.4 mm / 0.65 mm pitch	30	°C/W
	LQFP 144 - 20 x 20 mm / 0.5 mm pitch	40	
	LQFP 144 - 20 x 20 mm / 0.5 mm pitch on four layer FR4 board (2 layers signals / 2 layers power)	35	

Based on thermal characteristics of the package and with reference to the power consumption figures provided in next tables and diagrams, the following product classification can be proposed. Anyhow, the exact power consumption of the device inside the application must be computed according to different working conditions, thermal profiles, real thermal resistance of the system (including printed circuit board or other substrata), I/O activity, and so on.

Table 64. Product classification

Package	Ambient temperature range	CPU frequency range
Die	−40°C to +125°C	1 to 64 MHz
PQFP 144	−40°C to +125°C	1 to 64 MHz
LQFP 144	−40°C to +125°C	1 to 40 MHz
	−40°C to +105°C	1 to 48 MHz

24.4 Parameter interpretation

The parameters listed in the following tables represent the characteristics of the ST10F273Z4 and its demands on the system.

Where the ST10F273Z4 logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics, is included in the “Symbol” column. Where the external system must provide signals with their respective timing characteristics to the ST10F273Z4, the symbol “SR” for System Requirement, is included in the “Symbol” column.

24.7.2 A/D conversion accuracy

The A/D Converter compares the analog voltage sampled on the selected analog input channel to its analog reference voltage (V_{AREF}) and converts it into 10-bit digital data. The absolute accuracy of the A/D conversion is the deviation between the input analog value and the output digital value. It includes the following errors:

- Offset error (OFS)
- Gain Error (GE)
- Quantization error
- Non-Linearity error (Differential and Integral)

These four error quantities are explained below using [Figure 37](#).

Offset error

Offset error is the deviation between actual and ideal A/D conversion characteristics when the digital output value changes from the minimum (zero voltage) 00 to 01 ([Figure 37](#), see OFS).

Gain error

Gain error is the deviation between the actual and ideal A/D conversion characteristics when the digital output value changes from the 3FE to the maximum 3FF, once offset error is subtracted. Gain error combined with offset error represents the so-called full-scale error ([Figure 37](#), OFS + GE).

Quantization error

Quantization error is the intrinsic error of the A/D converter and is expressed as 1/2 LSB.

Non-linearity error

Non-Linearity error is the deviation between actual and the best-fitting A/D conversion characteristics (see [Figure 37](#)):

- Differential Non-Linearity error is the actual step dimension versus the ideal one (1 LSB_{IDEAL}).
- Integral Non-Linearity error is the distance between the center of the actual step and the center of the bisector line, in the actual characteristics. Note that for Integral Non-Linearity error, the effect of offset, gain and quantization errors is not included.

Note: *Bisector characteristic is obtained drawing a line from 1/2 LSB before the first step of the real characteristic, and 1/2 LSB after the last step again of the real characteristic.*

24.7.3 Total unadjusted error

The Total Unadjusted Error specifies the maximum deviation from the ideal characteristic: the number provided in the Data Sheet represents the maximum error with respect to the entire characteristic. It is a combination of the Offset, Gain and Integral Linearity errors. The different errors may compensate each other depending on the relative sign of the Offset and Gain errors. Refer to [Figure 37](#), see TUE.

24.8.7 Phase locked loop (PLL)

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and it provides the CPU clock (see [Table 70](#)). The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 ($f_{CPU} = f_{XTAL} \times F$). With every F'th transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, so the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{XTAL} . The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The real minimum value for TCL depends on the jitter of the PLL. The PLL tunes f_{CPU} to keep it locked on f_{XTAL} . The relative deviation of TCL is the maximum when it is referred to one TCL period.

This is especially important for bus cycles using wait states and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower Baud rates, etc.) the deviation caused by the PLL jitter is negligible. Refer to next [Section 24.8.9: PLL jitter](#) for more details.

24.8.8 Voltage controlled oscillator

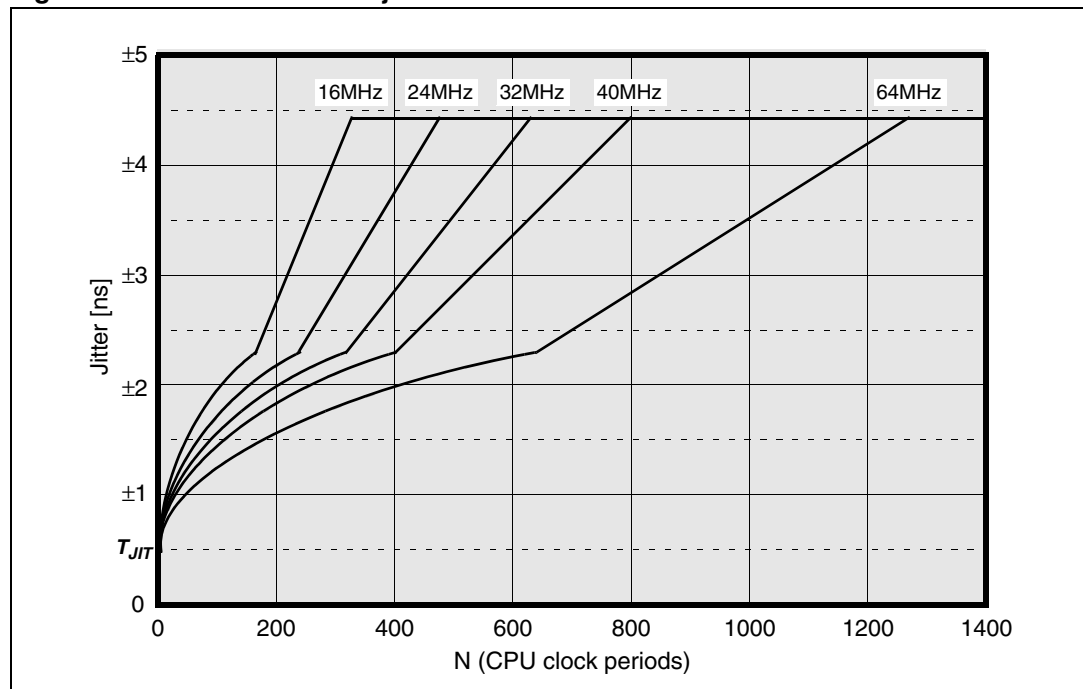
The ST10F273Z4 implements a PLL which combines different levels of frequency dividers with a Voltage Controlled Oscillator (VCO) working as frequency multiplier. In the following table, a detailed summary of the internal settings and VCO frequency is reported.

Table 71. Internal PLL divider mechanism

P0.15-13 (P0H.7-5)	XTAL frequency	Input prescaler	PLL		Output prescaler	CPU frequency $f_{CPU} = f_{XTAL} \times F$
			Multiply by	Divide by		
1 1 1	4 to 8 MHz	$F_{XTAL} / 4$	64	4	—	$F_{XTAL} \times 4$
1 1 0	5.3 to 10.6 MHz		48			$F_{XTAL} \times 3$
1 0 1	4 to 8 MHz		64	2		$F_{XTAL} \times 8$
1 0 0	6.4 to 12 MHz		40			$F_{XTAL} \times 5$
0 1 1	1 to 64 MHz	—	PLL bypassed		—	$F_{XTAL} \times 1$
0 1 0	4 to 6.4 MHz	$F_{XTAL} / 2$	40	2		$F_{XTAL} \times 10$
0 0 1	4 to 12 MHz ¹⁾	—	PLL bypassed			$F_{PLL} / 2$
0 0 0	4 MHz	$F_{XTAL} / 2$	64	2	—	$F_{XTAL} \times 16$

The PLL input frequency range is limited to 1 to 3.5 MHz, while the VCO oscillation range is 64 to 128 MHz. The CPU clock frequency range when PLL is used is 16 to 64 MHz.

Figure 44. ST10F273Z4 PLL jitter



24.8.10 PLL lock / unlock

During normal operation, if the PLL gets unlocked for any reason, an interrupt request to the CPU is generated, and the reference clock (oscillator) is automatically disconnected from the PLL input: in this way, the PLL goes into free-running mode, providing the system with a backup clock signal (free running frequency F_{free}). This feature allows to recover from a crystal failure occurrence without risking to go in an undefined configuration: the system is provided with a clock allowing the execution of the PLL unlock interrupt routine in a safe mode.

The path between reference clock and PLL input can be restored only by a hardware reset, or by a bidirectional software or watchdog reset event that forces the $\overline{RSTIN}$ pin low.

Note: The external RC circuit on $\overline{RSTIN}$ pin shall be properly sized in order to extend the duration of the low pulse to grant the PLL gets locked before the level at $\overline{RSTIN}$ pin is recognized high: bidirectional reset internally drives $\overline{RSTIN}$ pin low for just 1024 TCL (definitively not sufficient to get the PLL locked starting from free-running mode).

Table 72. PLL characteristics [$V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$]

Symbol	Parameter	Conditions	Value		Unit
			Min.	Max.	
T_{PSUP}	PLL start-up time ⁽¹⁾	Stable V_{DD} and reference clock	–	300	μs
T_{LOCK}	PLL lock-in time	Stable V_{DD} and reference clock, starting from free-running mode	–	250	
T_{JIT}	Single period jitter ⁽¹⁾ (cycle to cycle = 2 TCL)	6 sigma time period variation (peak to peak)	–500	+500	ps
F_{free}	PLL free running frequency	Multiplication factors: 3, 4 Multiplication factors: 5, 8, 10, 16	250 500	2000 4000	kHz

1. Not 100% tested, guaranteed by design characterization.

24.8.11 Main oscillator specifications

$V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$

Table 73. Main oscillator characteristics

Sym bol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
g_m	Oscillator transconductance		8	17	35	mA/V
V_{OSC}	Oscillation amplitude ⁽¹⁾	Peak to peak	–	$V_{DD} - 0.4$	–	V
V_{AV}	Oscillation voltage level ⁽¹⁾	Sine wave middle		$V_{DD} / 2 - 0.25$	–	
t_{STUP}	Oscillator start-up time ⁽¹⁾	Stable V_{DD} - crystal		3	4	ms
		Stable V_{DD} - resonator		2	3	

1. Not 100% tested, guaranteed by design characterization.

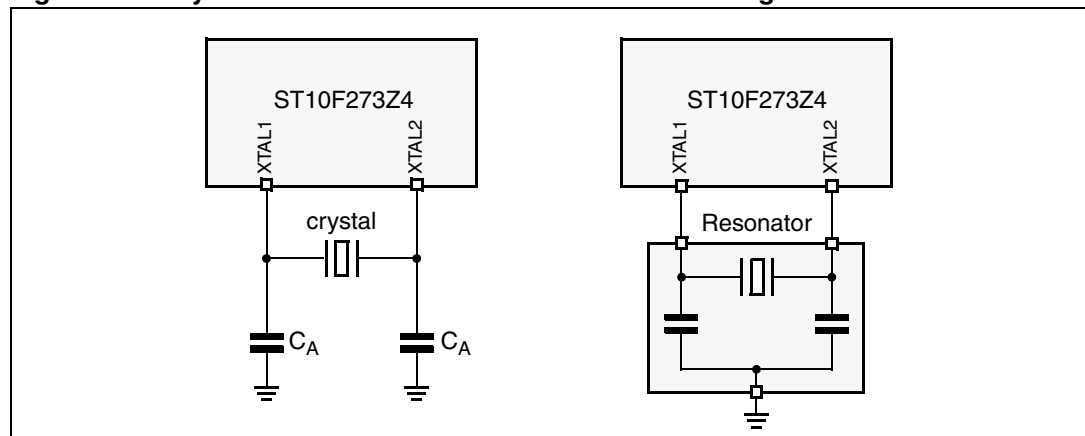
Figure 45. Crystal oscillator and resonator connection diagram

Figure 51. External memory cycle: multiplexed bus, with/without r/w delay, extended ALE, r/w CS

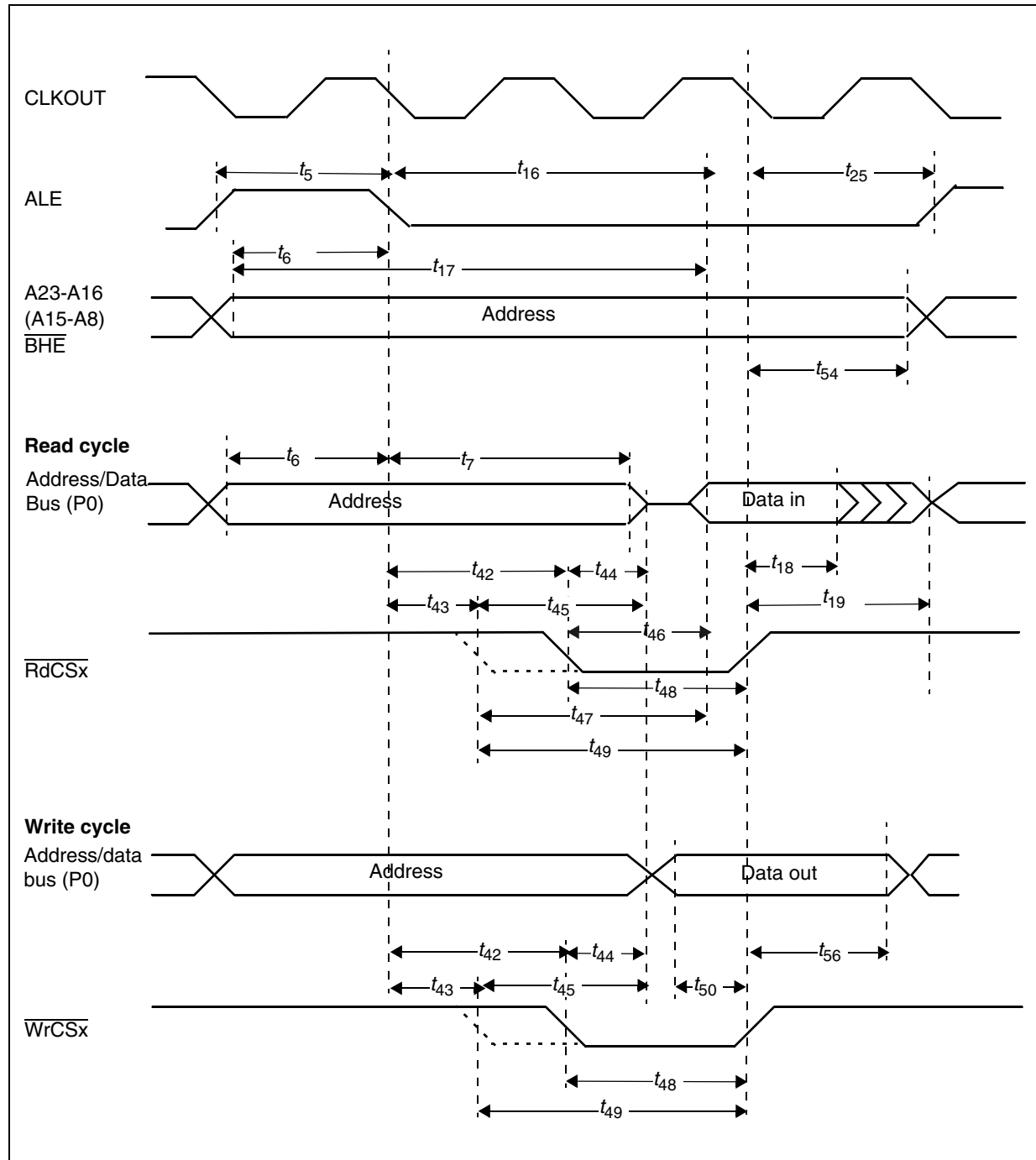
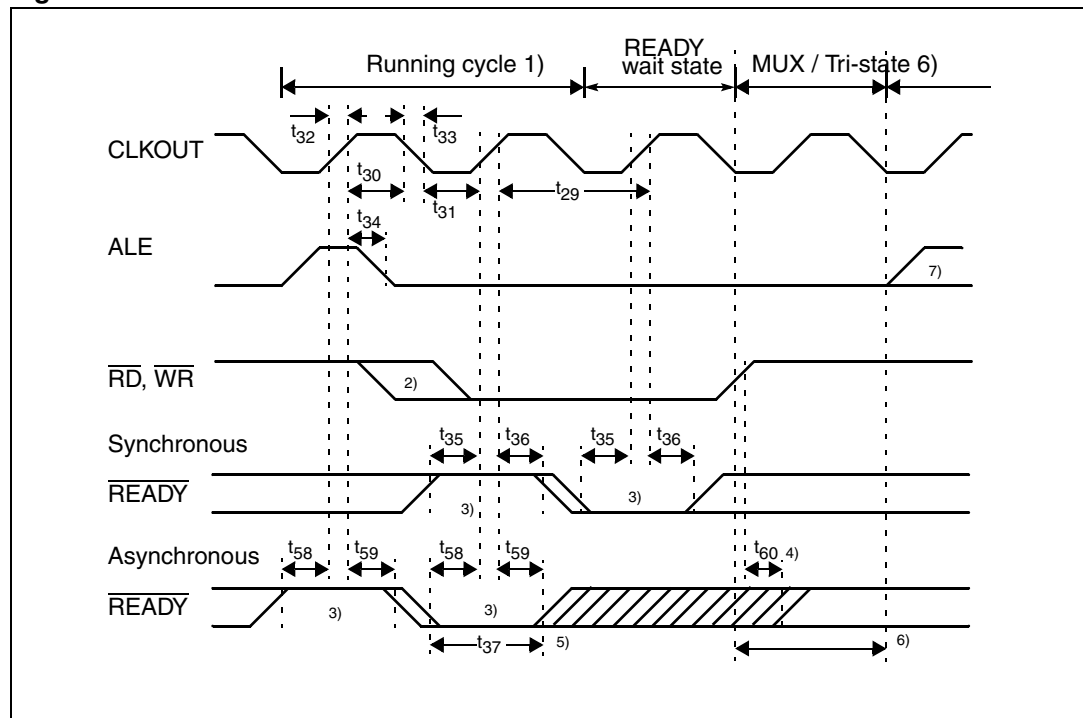


Figure 56. CLKOUT and $\overline{\text{READY}}$ 

1. Cycle as programmed, including MCTC wait states (Example shows 0 MCTC WS).
2. The leading edge of the respective command depends on RW-delay.
3. $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a READY controlled wait state, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.
4. $\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).
5. If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if $\overline{\text{READY}}$ is removed in response to the command (see Note 4).
6. Multiplexed bus modes have a MUX wait state added after a bus cycle, and an additional MTTC wait state may be inserted here.
For a multiplexed bus with MTTC wait state this delay is two CLKOUT cycles, for a demultiplexed bus without MTTC wait state this delay is zero.
7. The next external bus cycle may start here.

25.1.4 Spurious $\overline{\text{BREQ}}$ pulse in slave mode during external bus arbitration phase

Description

Sporadic bus errors may occur when the device operates as a slave and the $\overline{\text{HOLD}}$ signal is used for external bus arbitration.

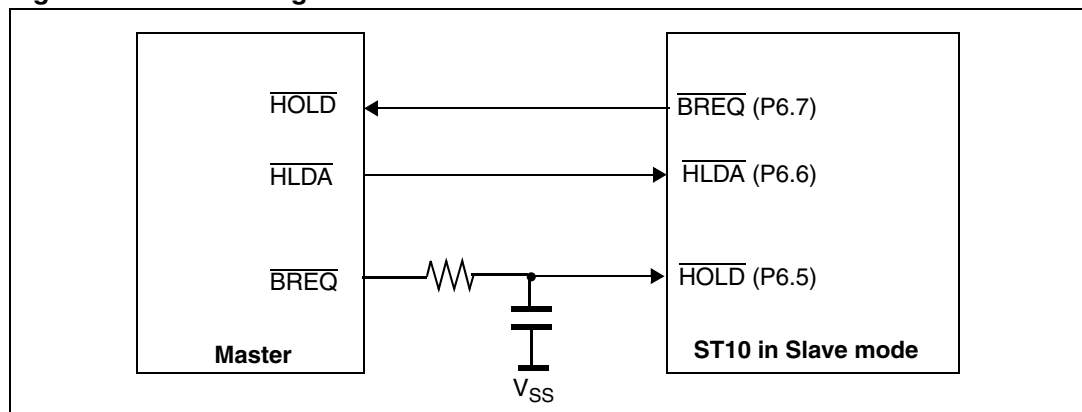
After the slave has been granted the bus, it deactivates sporadically $\overline{\text{BREQ}}$ signal for a short time, even though its access to the bus has not been completed. The master then starts accessing the bus, thus causing a bus conflict between master and slave.

Workaround

To avoid producing any spurious $\overline{\text{BREQ}}$ pulse during slave external bus arbitrations, it is necessary to ensure that the time between the $\overline{\text{HLDA}}$ assertion (Bus Acknowledge from Master device) and the following $\overline{\text{HOLD}}$ falling edge (Bus Request from Master) is longer than three clock cycles.

This can be achieved by delaying the $\overline{\text{HOLD}}$ signal with an RC circuit (see [Figure 63](#)).

Figure 63. Connecting an ST10 in slave mode



25.1.5 Executing PWRDN instructions

Description

The Power-down mode is not entered and the PWRDN instruction is ignored in the following cases:

- The PWRDN instruction is executed while $\overline{\text{NMI}}$ is high (PWDCFG bit of the SYSCON register cleared)
- The PWRDN instruction is executed while at least one of the Port 2 pins used to exit from Power-down mode (PWDCFG bit of the SYSCON register is set) is at the active level.

Figure 65. LQFP144 - 144 pin low profile quad flat package 20x20 mm, 0.5 mm pitch, package outline

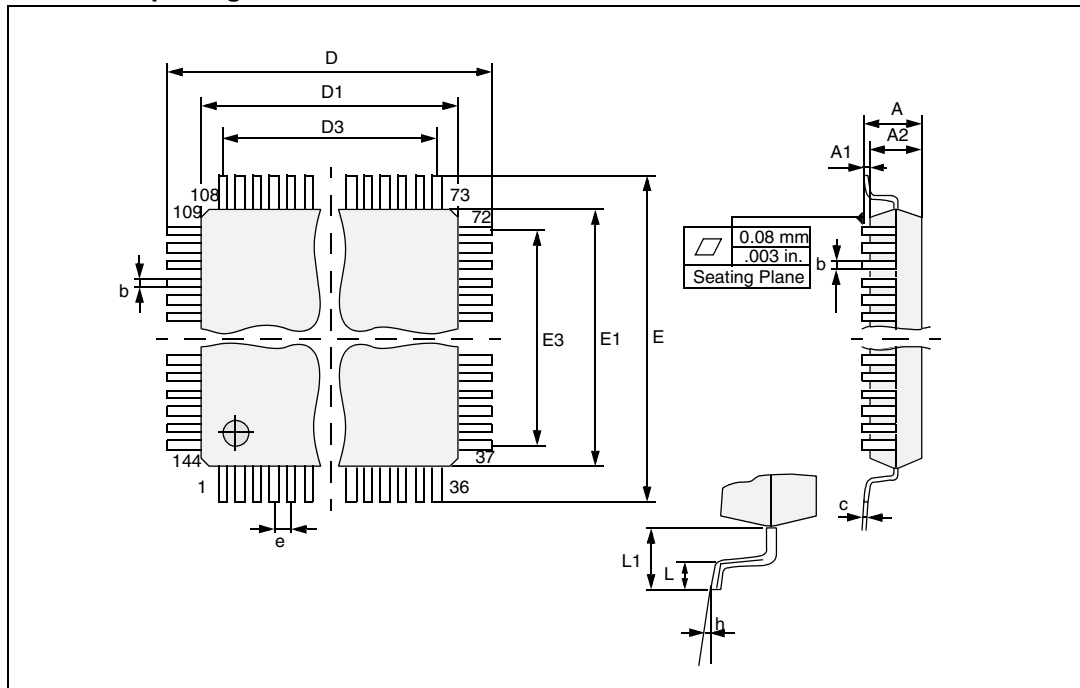


Table 85. LQFP144 - 144 pin low profile quad flat package 20x20mm, 0.5 mm pitch, package mechanical data

Dim.	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053		0.057
b	0.17	0.22	0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	21.80	22.00	22.20	0.858	0.867	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D3		17.50			0.689	
E	21.80	22.00	22.20	0.858	0.867	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E3		17.50			0.689	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	

1. Values in inches are converted from mm and rounded up to 4 decimal places.