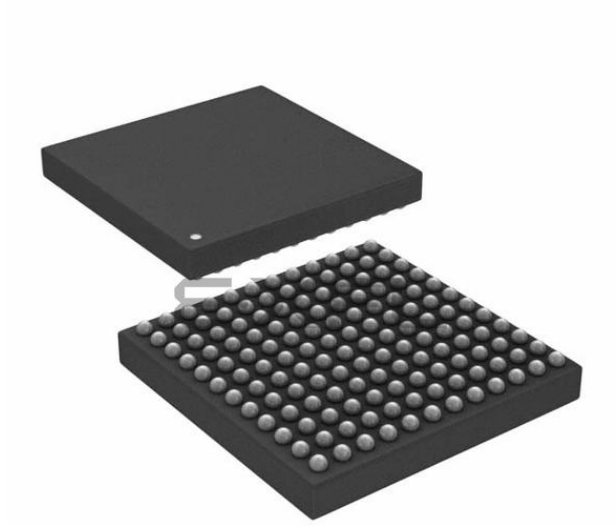

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SPI, SSP, UART
Clock Rate	160MHz
Non-Volatile Memory	External
On-Chip RAM	160kB
Voltage - I/O	3.00V, 3.30V
Voltage - Core	2.50V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-MiniBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2191mkca-160

- EE-156: Support for the H.100 protocol on the ADSP-2191
- EE-158: ADSP-2181 EZ-Kit Lite IDMA to PC Printer Port Interface
- EE-159: Initializing DSP System & Control Registers From C and C++
- EE-164: Advanced EPROM Boot and No-boot Scenarios with ADSP-219x DSPs
- EE-168: Using Third Overtone Crystals with the ADSP-218x DSP
- EE-17: ADSP-2187L Memory Organization
- EE-18: Choosing and Using FFTs for ADSP-21xx
- EE-188: Using C To Implement Interrupt-Driven Systems On ADSP-219x DSPs
- EE-2: Using ADSP-218x I/O Space
- EE-226: ADSP-2191 DSP Host Port Booting
- EE-227: CAN Configuration Procedure for ADSP-21992 DSPs
- EE-249: Implementing Software Overlays on ADSP-218x DSPs with VisualDSP++®
- EE-32: Language Extensions: Memory Storage Types, ASM & Inline Constructs
- EE-35: Troubleshooting your ADSP-218x EZ-ICE
- EE-356: Emulator and Evaluation Hardware Troubleshooting Guide for CCES Users
- EE-38: ADSP-2181 IDMA Port - Cycle Steal Timing
- EE-39: Interfacing 5V Flash Memory to an ADSP-218x (Byte Programming Algorithm)
- EE-5: ADSP-218x Full Memory Mode vs. Host Memory Mode
- EE-60: Simulating an RS-232 UART Using the Synchronous Serial Ports on the ADSP-21xx Family DSPs
- EE-64: Setting Mode Pins on Reset
- EE-68: Analog Devices JTAG Emulation Technical Reference
- EE-71: Minimum Rise Time Specs for Critical Interrupt and Clock Signals on the ADSP-21x1/21x5
- EE-74: Analog Devices Serial Port Development and Troubleshooting Guide
- EE-78: BDMA Usage on 100 pin ADSP-218x DSPs Configured for IDMA Use
- EE-79: EPROM Booting In Host Mode with 100 Pin 218x Processors
- EE-82: Using an ADSP-2181 DSP's IO Space to IDMA Boot Another ADSP-2181
- EE-89: Implementing A Software UART on the ADSP-2181 EZ-Kit-Lite
- EE-96: Interfacing Two AD73311 Codecs to the ADSP-218x

Data Sheet

- ADSP-2191M: DSP Microcomputer Data Sheet

Evaluation Kit Manuals

- ADSP-2191 EZ-KIT Lite® Manual

Integrated Circuit Anomalies

- ADSP-2191/95/96 Anomaly List for Revision 1.0

Processor Manuals

- ADSP-219x/2191 DSP Hardware Reference
- ADSP 21xx Processors: Manuals
- ADSP-219x DSP Instruction Set Reference
- ADSP-219x/2192 DSP Hardware Reference (Rev 1.1, April 2004)
- Using the ADSP-2100 Family Volume 1
- Using the ADSP-2100 Family Volume 2

Product Highlight

- ADSP-2191 16-Bit Fixed Point DSP Product Brief

Software Manuals

- VisualDSP++ 3.5 Assembler and Preprocessor Manual for ADSP-218x and ADSP-219x DSPs
- VisualDSP++ 3.5 C Compiler and Library Manual for ADSP-218x DSPs
- VisualDSP++ 3.5 C/C++ Compiler and Library Manual for ADSP-219x Processors
- VisualDSP++ 3.5 Component Software Engineering User's Guide for 16-Bit Processors
- VisualDSP++ 3.5 Getting Started Guide for 16-Bit Processors
- VisualDSP++ 3.5 Kernel VDK User's Guide for 16-Bit Processors
- VisualDSP++ 3.5 Linker and Utilities Manual for 16-Bit Processors
- VisualDSP++ 3.5 Loader Manual for 16-Bit Processors
- VisualDSP++ 3.5 Quick Installation Reference Card
- VisualDSP++ 3.5 User's Guide for 16-Bit Processors

SOFTWARE AND SYSTEMS REQUIREMENTS

- Software and Tools Anomalies Search

TOOLS AND SIMULATIONS

- ADSP-2191M: LQFP package
- ADSP-21xx Processors: Software and Tools
- ADSP-2191M IBIS Datafile (BGA Package), Version 2.1
- ADSP-2191M IBIS Datafile (LQFP Package)
- ADSP-2191M IBIS Datafile (LQFP Package), Version 2.1

ADSP-2191M

INTEGRATION FEATURES

160K Bytes On-Chip RAM Configured as 32K Words 24-Bit Memory RAM and 32K Words 16-Bit Memory RAM
Dual-Purpose 24-Bit Memory for Both Instruction and Data Storage
Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units with Dual 40-Bit Accumulators
Unified Memory Space Allows Flexible Address Generation, Using Two Independent DAG Units
Powerful Program Sequencer Provides Zero-Overhead Looping and Conditional Instruction Execution
Enhanced Interrupt Controller Enables Programming of Interrupt Priorities and Nesting Modes

SYSTEM INTERFACE FEATURES

Host Port with DMA Capability for Glueless 8- or 16-Bit Host Interface
16-Bit External Memory Interface for up to 16M Words of Addressable Memory Space
Three Full-Duplex Multichannel Serial Ports, with Support for H.100 and up to 128 TDM Channels with A-Law and μ-Law Companding Optimized for Telecommunications Systems
Two SPI-Compatible Ports with DMA Support
UART Port with DMA Support
16 General-Purpose I/O Pins with Integrated Interrupt Support
Three Programmable Interval Timers with PWM Generation, PWM Capture/Pulsewidth Measurement, and External Event Counter Capabilities
Up to 11 DMA Channels Can Be Active at Any Given Time for High I/O Throughput
On-Chip Boot ROM for Automatic Booting from External 8- or 16-Bit Host Device, SPI ROM, or UART with Autobaud Detection
Programmable PLL Supports 1× to 32× Input Frequency Multiplication and Can Be Altered during Runtime
IEEE JTAG Standard 1149.1 Test Access Port Supports On-Chip Emulation and System Debugging
2.5 V Internal Operation and 3.3 V I/O
144-Lead LQFP and 144-Ball Mini-BGA Packages

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The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Boot memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2191M to fetch two operands in a single cycle, one from program memory and one from data memory. The DSP's dual memory buses also let the ADSP-219x core fetch an operand from data memory and the next instruction from program memory in a single cycle.

DSP Peripherals Architecture

The functional block diagram on Page 1 shows the DSP's on-chip peripherals, which include the external memory interface, Host port, serial ports, SPI-compatible ports, UART port, JTAG test and emulation port, timers, flags, and interrupt controller. These on-chip peripherals can connect to off-chip devices as shown in Figure 1.

The ADSP-2191M has a 16-bit Host port with DMA capability that lets external Hosts access on-chip memory. This 24-pin parallel port consists of a 16-pin multiplexed data/address bus and provides a lowservice overhead data move capability. Configurable for 8 or 16 bits, this port provides a glueless interface to a wide variety of 8- and 16-bit microcontrollers. Two chip-selects provide Hosts access to the DSP's entire memory map. The DSP is bootable through this port.

The ADSP-2191M also has an external memory interface that is shared by the DSP's core, the DMA controller, and DMA capable peripherals, which include the UART, SPORT0, SPORT1, SPORT2, SPI0, SPI1, and the Host port. The external port consists of a 16-bit data bus, a 22-bit address bus, and control signals. The data bus is configurable to provide an 8- or 16-bit interface to external memory. Support for word packing lets the DSP access 16- or 24-bit words from external memory regardless of the external data bus width. When configured for an 8-bit interface, the unused eight lines provide eight programmable, bidirectional general-purpose Programmable Flag lines, six of which can be mapped to software condition signals.

The memory DMA controller lets the ADSP-2191M move data and instructions from between memory spaces: internal-to-external, internal-to-internal, and external-to-external. On-chip peripherals can also use this controller for DMA transfers.

The ADSP-2191M can respond to up to seventeen interrupts at any given time: three internal (stack, emulator kernel, and power-down), two external (emulator and reset), and twelve user-defined (peripherals) interrupts. The programmer assigns a peripheral to one of the 12 user-defined interrupts. The priority of each peripheral for interrupt service is determined by these assignments.

There are three serial ports on the ADSP-2191M that provide a complete synchronous, full-duplex serial interface. This interface includes optional companding in hardware as well as a wide variety of framed or frameless data transmit and receive modes

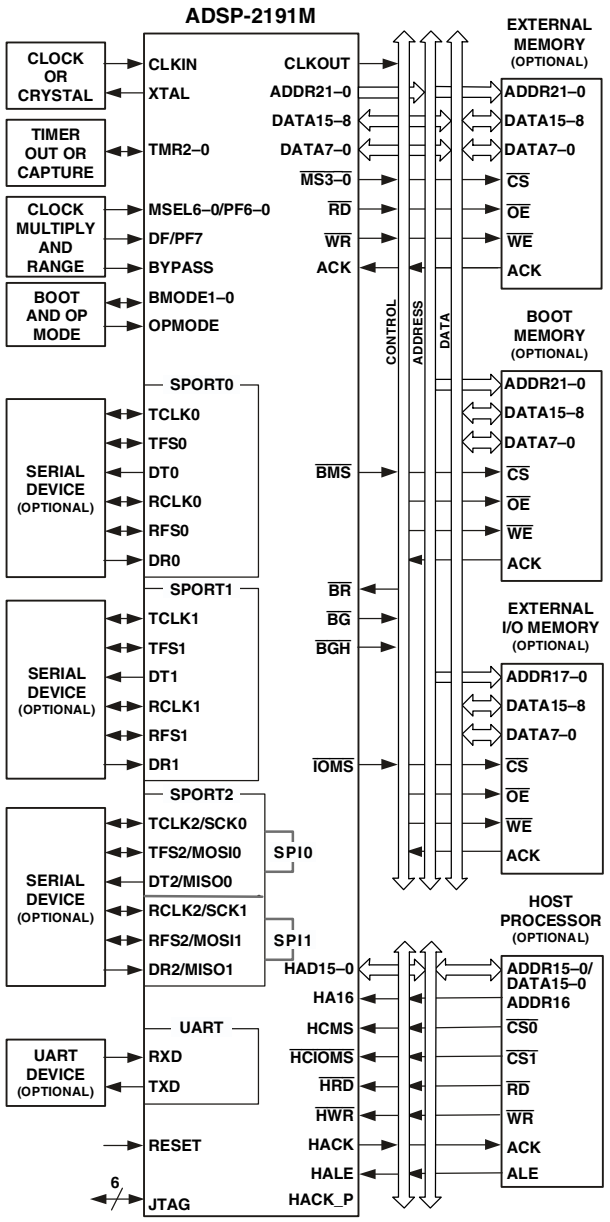

Figure 1. System Diagram

of operation. Each serial port can transmit or receive an internal or external, programmable serial clock and frame syncs. Each serial port supports 128-channel Time Division Multiplexing.

The ADSP-2191M provides up to sixteen general-purpose I/O pins, which are programmable as either inputs or outputs. Eight of these pins are dedicated-general purpose Programmable Flag pins. The other eight of them are multifunctional pins, acting as general-purpose I/O pins when the DSP connects to an 8-bit external data bus and acting as the upper eight data pins when the DSP connects to a 16-bit external data bus. These Programmable Flag pins can implement edge- or level-sensitive interrupts, some of which can be used to base the execution of conditional instructions.

the instruction provides an immediate 24-bit address value. The PC allows linear addressing of the full 24-bit address range.

- For indirect jumps and calls that use a 16-bit DAG address register for part of the branch address, the Program Sequencer relies on an 8-bit Indirect Jump page (IJPG) register to supply the most significant eight address bits. Before a cross page jump or call, the program must set the program sequencer's IJPG register to the appropriate memory page.

The ADSP-2191M has 1K word of on-chip ROM that holds boot routines. If peripheral booting is selected, the DSP starts executing instructions from the on-chip boot ROM, which starts the boot process from the selected peripheral. For more information, see "Booting Modes" on Page 11. The on-chip boot ROM is located on Page 255 in the DSP's memory space map.

External (Off-Chip) Memory

Each of the ADSP-2191M's off-chip memory spaces has a separate control register, so applications can configure unique access parameters for each space. The access parameters include read and write wait counts, waitstate completion mode, I/O clock divide ratio, write hold time extension, strobe polarity, and data bus width. The core clock and peripheral clock ratios influence the external memory access strobe widths. For more information, see "Clock Signals" on Page 11. The off-chip memory spaces are:

- External memory space ($\overline{\text{MS3–0}}$ pins)
- I/O memory space ($\overline{\text{IOMS}}$ pin)
- Boot memory space ($\overline{\text{BMS}}$ pin)

All of these off-chip memory spaces are accessible through the External Port, which can be configured for data widths of 8 or 16 bits.

External Memory Space

External memory space consists of four memory banks. These banks can contain a configurable number of 64K word pages. At reset, the page boundaries for external memory have Bank0 containing Pages 1–63, Bank1 containing Pages 64–127, Bank2 containing Pages 128–191, and Bank3 that contains Pages 192–254. The $\overline{\text{MS3–0}}$ memory bank pins select Banks 3–0, respectively. The external memory interface is byte-addressable and decodes the 8 MSBs of the DSP program address to select one of the four banks. Both the ADSP-219x core and DMA-capable peripherals can access the DSP's external memory space.

I/O Memory Space

The ADSP-2191M supports an additional external memory called I/O memory space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports a total of 256K locations. The first 8K addresses are reserved for on-chip peripherals. The upper 248K addresses are available for external peripheral devices. The DSP's instruction set provides instructions for accessing I/O space. These instructions use an 18-bit address that is assembled from an 8-bit I/O page (IOPG) register and a 10-bit immediate value supplied in the instruction. Both the ADSP-219x core and a Host (through the Host Port Interface) can access I/O memory space.

Boot Memory Space

Boot memory space consists of one off-chip bank with 63 pages. The $\overline{\text{BMS}}$ memory bank pin selects boot memory space. Both the ADSP-219x core and DMA-capable peripherals can access the DSP's off-chip boot memory space. After reset, the DSP always starts executing instructions from the on-chip boot ROM. Depending on the boot configuration, the boot ROM code can start booting the DSP from boot memory. For more information, see "Booting Modes" on Page 11.

Interrupts

The interrupt controller lets the DSP respond to 17 interrupts with minimum overhead. The controller implements an interrupt priority scheme as shown in Table 1. Applications can use the unassigned slots for software and peripheral interrupts.

Table 2 shows the ID and priority at reset of each of the peripheral interrupts. To assign the peripheral interrupts a different priority, applications write the new priority to their corresponding control bits (determined by their ID) in the Interrupt Priority Control register. The peripheral interrupt's position in the IMASK and IRPTL register and its vector address depend on its priority level, as shown in Table 1. Because the IMASK and IRPTL registers are limited to 16 bits, any peripheral interrupts assigned a priority level of 11 are aliased to the lowest priority bit position (15) in these registers and share vector address 0x00 01E0.

Table 1. Interrupt Priorities/Addresses

Interrupt	IMASK/ IRPTL	Vector Address[1]
Emulator (NMI)— Highest Priority	NA	NA
Reset (NMI)	0	0x00 0000
Power-Down (NMI)	1	0x00 0020
Loop and PC Stack	2	0x00 0040
Emulation Kernel	3	0x00 0060
User Assigned Interrupt	4	0x00 0080
User Assigned Interrupt	5	0x00 00A0
User Assigned Interrupt	6	0x00 00C0
User Assigned Interrupt	7	0x00 00E0
User Assigned Interrupt	8	0x00 0100
User Assigned Interrupt	9	0x00 0120
User Assigned Interrupt	10	0x00 0140
User Assigned Interrupt	11	0x00 0160
User Assigned Interrupt	12	0x00 0180
User Assigned Interrupt	13	0x00 01A0
User Assigned Interrupt	14	0x00 01C0
User Assigned Interrupt— Lowest Priority	15	0x00 01E0

[1]These interrupt vectors start at address 0x10000 when the DSP is in "no-boot," run from external memory mode.

Table 6. Select Boot Mode (OPMODE, BMODE1, and BMODE0)

OPMODE	BMODE1	BMODE0	Function
0	0	0	Execute from external memory 16 bits (No Boot)
0	0	1	Boot from EPROM
0	1	0	Boot from Host
0	1	1	Reserved
1	0	0	Execute from external memory 8 bits (No Boot)
1	0	1	Boot from UART
1	1	0	Boot from SPI, up to 4K bits
1	1	1	Boot from SPI, >4K bits up to 512K bits

The OPMODE, BMODE1, and BMODE0 pins, sampled during hardware reset, and three bits in the Reset Configuration Register implement these modes:

- Execute from memory external 16 bits—The memory boot routine located in boot ROM memory space executes a boot-stream-formatted program located at address 0x010000 of boot memory space, packing 16-bit external data into 24-bit internal data. The External Port Interface is configured for the default clock multiplier (128) and read waitstates (7).
- Boot from EPROM—The EPROM boot routine located in boot ROM memory space fetches a boot-stream-formatted program located at physical address 0x00 0000 of boot memory space, packing 8- or 16-bit external data into 24-bit internal data. The External Port Interface is configured for the default clock multiplier (32) and read waitstates (7).
- Boot from Host—The (8- or 16-bit) Host downloads a boot-stream-formatted program to internal or external memory. The Host's boot routine is located in internal ROM memory space and uses the top 16 locations of Page 0 program memory and the top 272 locations of Page 0 data memory.

  The internal boot ROM sets semaphore A (an IO register within the Host port) and then polls until the semaphore is reset. Once detected, the internal boot ROM will remap the interrupt vector table to Page 0 internal memory and jump to address 0x00 0000 internal memory. From the point of view of the host interface, an external host has full control of the DSP's memory map. The Host has the freedom to directly write internal memory, external memory, and internal I/O memory space. The DSP core execution is held off until the Host clears the semaphore register. This strategy allows the maximum flexibility for the Host to boot in the program and data code, by leaving it up to the programmer.
- Execute from memory external 8 bits (No Boot)—Execution starts from Page 1 of external memory space, packing either 8- or 16-bit external data into 24-bit internal data. The External Port Interface is configured for the default clock multiplier (128) and read waitstates (7).
- Boot from UART—Using an autobaud handshake sequence, a boot-stream-formatted program is downloaded by the Host. The Host agent selects a baud rate within the UART's clocking capabilities. After a hardware reset, the DSP's UART expects a 0xAA character (eight bits data, one start bit, one stop bit, no parity bit) on the RXD pin to determine the bit rate; and then replies with an OK string. Once the host receives this OK it downloads the boot stream without further handshake.The UART boot routine is located in internal ROM memory space and uses the top 16 locations of Page 0 program memory and the top 272 locations of Page 0 data memory.
- Boot from SPI, up to 4K bits—The SPI0 port uses the SPI0SEL1 (reconfigured PF2) output pin to select a single serial EEPROM device, submits a read command at address 0x00, and begins clocking consecutive data into internal or external memory. Use only SPI-compatible EEPROMs of ≤ 4K bit (12-bit address range). The SPI0 boot routine located in internal ROM memory space executes a boot-stream-formatted program, using the top 16 locations of Page 0 program memory and the top 272 locations of Page 0 data memory. The SPI boot configuration is SPIBAUD0=60 (decimal), CPHA=1, CPOL=1, 8-bit data, and MSB first.
- Boot from SPI, from >4K bits to 512K bits—The SPI0 port uses the SPI0SEL1 (re-configured PF2) output pin to select a single serial EEPROM device, submits a read command at address 0x00, and begins clocking consecutive data into internal or external memory. Use only SPI-compatible EEPROMs of ≥ 4K bit (16-bit address range). The SPI0 boot routine, located in internal ROM memory space, executes a boot-stream-formatted program, using the top 16 locations of Page 0 program memory and the top 272 locations of Page 0 data memory.

As indicated in Table 6, the OPMODE pin has a dual role, acting as a boot mode select during reset and determining SPORT or SPI operation at runtime. If the OPMODE pin at reset is the opposite of what is needed in an application during runtime, the application needs to set the OPMODE bit appropriately during runtime prior to using the corresponding peripheral.

Bus Request and Bus Grant

The ADSP-2191M can relinquish control of the data and address buses to an external device. When the external device requires access to the bus, it asserts the bus request ($\overline{BR}$) signal. The ($\overline{BR}$) signal is arbitrated with core and peripheral requests. External Bus requests have the lowest priority. If no other internal request is pending, the external bus request will be granted.

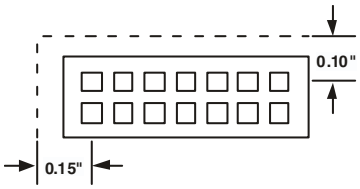

Figure 7. JTAG Pod Connector Keep-Out Area

Design-for-Emulation Circuit Information

For details on target board design issues including: single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

Additional Information

This data sheet provides a general overview of the ADSP-2191M architecture and functionality. For detailed information on the core architecture of the ADSP-219x family, refer to the *ADSP-219x/ADSP-2191 DSP Hardware Reference*. For details on the instruction set, refer to the *ADSP-219x Instruction Set Reference*.

PIN FUNCTION DESCRIPTIONS

ADSP-2191M pin definitions are listed in Table 7. All ADSP-2191M inputs are asynchronous and can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Tie or pull unused inputs to V_{DDEXT} or GND, except for ADDR21–0, DATA15–0, PF7-0, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{TRST}}$, BMODE0, BMODE1, OPMODE, BYPASS, TCK, TMS, TDI, and $\overline{\text{RESET}}$)—these pins can be left floating. These pins have a logic-level hold circuit that prevents input from floating internally.

The following symbols appear in the Type column of Table 7: G = Ground, I = Input, O = Output, P = Power Supply, and T = Three-State.

Table 7. Pin Function Descriptions

Pin	Type	Function
A21–0	O/T	External Port Address Bus
D7–0	I/O/T	External Port Data Bus, least significant 8 bits
D15	I/O/T	Data 15 (if 16-bit external bus)/Programmable Flags 15 (if 8-bit external bus)/SPI1 Slave
/PF15	I/O	Select output 7 (if 8-bit external bus, when SPI1 enabled)
/SPI1SEL7	I	
D14	I/O/T	Data 14 (if 16-bit external bus)/Programmable Flags 14 (if 8-bit external bus)/SPI0 Slave
/PF14	I/O	Select output 7 (if 8-bit external bus, when SPI0 enabled)
/SPI0SEL7	I	
D13	I/O/T	Data 13 (if 16-bit external bus)/Programmable Flags 13 (if 8-bit external bus)/SPI1 Slave
/PF12	I/O	Select output 6 (if 8-bit external bus, when SPI1 enabled)
/SPI1SEL6	I	
D12	I/O/T	Data 12 (if 16-bit external bus)/Programmable Flags 12 (if 8-bit external bus)/SPI0 Slave
/PF12	I/O	Select output 6 (if 8-bit external bus, when SPI0 enabled)
/SPI0SEL6	I	
D11	I/O/T	Data 11 (if 16-bit external bus)/Programmable Flags 11 (if 8-bit external bus)/SPI1 Slave
/PF11	I/O	Select output 5 (if 8-bit external bus, when SPI1 enabled)
/SPI1SEL5	I	
D10	I/O/T	Data 10 (if 16-bit external bus)/Programmable Flags 10 (if 8-bit external bus)/SPI0 Slave
/PF10	I/O	Select output 5 (if 8-bit external bus, when SPI0 enabled)
/SPI0SEL5	I	
D9	I/O/T	Data 9 (if 16-bit external bus)/Programmable Flags 9 (if 8-bit external bus)/SPI1 Slave Select
/PF9	I/O	output 4 (if 8-bit external bus, when SPI1 enabled)
/SPI1SEL4	I	
D8	I/O/T	Data 8 (if 16-bit external bus)/Programmable Flags 8 (if 8-bit external bus)/SPI0 Slave Select
/PF8	I/O	output 4 (if 8-bit external bus, when SPI0 enabled)
/SPI0SEL4	I	
PF7	I/O/T	Programmable Flags 7/SPI1 Slave Select output 3 (when SPI0 enabled)/Divisor Frequency
/SPI1SEL3	I	(divisor select for PLL input during boot)
/DF	I	
PF6	I/O/T	Programmable Flags 6/SPI0 Slave Select output 3 (when SPI0 enabled)/Multiplier Select 6
/SPI0SEL3	I	(during boot)
/MSEL6	I	

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		Test Conditions	K Grade (Commercial) Min	K Grade (Commercial) Max	B Grade (Industrial) Min	B Grade (Industrial) Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage		2.37	2.63	2.37	2.63	V
V_{DDEXT}	External (I/O) Supply Voltage		2.97	3.6	2.97	3.6	V
V_{IH}	High Level Input Voltage	@ V_{DDINT} = max, V_{DDEXT} = max	2.0	V_{DDEXT} + 0.3	2.0	V_{DDEXT} + 0.3	V
V_{IL}	Low Level Input Voltage	@ V_{DDINT} = min, V_{DDEXT} = min	–0.3	+0.8	–0.3	+0.8	V
T_{AMB}	Ambient Operating Temperature		0	70	–40	+85	°C

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K and B Grades Min	K and B Grades Typ	K and B Grades Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = min, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = min, I_{OL} = 2.0 mA			0.4	V
I_{IH}	High Level Input Current[2, 3]	@ V_{DDEXT} = max, V_{IN} = V_{DD} max			10	µA
I_{IL}	Low Level Input Current[3, 4]	@ V_{DDEXT} = max, V_{IN} = 0 V			10	µA
I_{IHP}	High Level Input Current[5]	@ V_{DDEXT} = max, V_{IN} = V_{DD} max	30		100	µA
I_{ILP}	Low Level Input Current[4]	@ V_{DDEXT} = max, V_{IN} = 0 V	20		70	µA
I_{OZH}	Three-State Leakage Current[5]	@ V_{DDEXT} = max, V_{IN} = V_{DD} max			10	µA
I_{OZL}	Three-State Leakage Current[6]	@ V_{DDEXT} = max, V_{IN} = 0 V			10	µA
C_{IN}	Input Capacitance[6, 7]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V			8	pF

Specifications subject to change without notice.

[1]Applies to output and bidirectional pins: DATA15–0, ADDR21–0, HAD15–0, $\overline{MS3–0}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$, CLKOUT, HACK, PF7–0, TMR2–0, $\overline{BGH}$, $\overline{BG}$, DT0, DT1, DT2/MISO0, TCLK0, TCLK1, TCLK2/SCK0, RCLK0, RCLK1, RCLK2/SCK1, TFS0, TFS1, TFS2/MOSI0, RFS0, RFS1, RFS2/MOSI1, $\overline{BMS}$, TDO, TXD, $\overline{EMU}$, DR2/MISO1.

[2]Applies to input pins: ACK, $\overline{BR}$, $\overline{HCMS}$, $\overline{HCIOMS}$, HA16, HALE, $\overline{HRD}$, $\overline{HWR}$, CLKIN, DR0, DR1, RXD, HACK_P.

[3]Applies to input pins with internal pull-ups: BMODE0, BMODE1, OPMODE, BYPASS, TCK, TMS, TDI, $\overline{RESET}$.

[4]Applies to input pin with internal pull-down: TRST.

[5]Applies to three-statable pins: DATA15–0, ADDR21–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PF7–0, $\overline{BMS}$, $\overline{IOMS}$, TFSx, RFSx, TDO, $\overline{EMU}$, TCLKx, RCLKx, DTx, HAD15–0, TMR2–0.

[6]Applies to all signal pins.

[7]Guaranteed, but not tested.

ABSOLUTE MAXIMUM RATINGS

V_{DDINT} Internal (Core) Supply Voltage[1] . . . –0.3 V to +3.0 V
V_{DDEXT} External (I/O) Supply Voltage . . . . –0.3 V to +4.6 V
V_{IL}–V_{IH} Input Voltage . . . . . –0.5 V to V_{DDEXT}+0.5 V
V_{OL}–V_{OH} Output Voltage Swing. . . –0.5 V to V_{DDEXT}+0.5 V
T_{STORE} Storage Temperature Range. . . . . .–65°C to +150°C
T_{LEAD} Lead Temperature of ST-144 (5 seconds) . . . . 185°C

[1]Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-2191M features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Power Dissipation

Using the operation-versus-current information in Table 8, designers can estimate the ADSP-2191M's internal power supply (V_{DDINT}) input current for a specific application, according to the formula for I_{DDINT} calculation beneath Table 8. For calculation of external supply current and total supply current, see Power Dissipation on Page 40.

Table 8. Operation Types Versus Input Current

	K-Grade I_{DDINT}(mA) CCLK = 160 MHz				B-Grade I_{DDINT}(mA)[1] CCLK = 140 MHz			
	Core		Peripheral		Core		Peripheral	
Activity	Typ[1]	Max[2]	Typ[1]	Max[2]	Typ[1]	Max[2]	Typ[1]	Max[2]
Power Down[3]	100 µA	600 µA	0	50 µA	100 µA	500 µA	0	50 µA
Idle 1[4]	1	2	5	8	1	2	4	7
Idle 2[5]	1	2	60	70	1	2	55	62
Typical[6]	184	210	60	70	165	185	55	62
Peak[7]	215	240	60	70	195	210	55	62

[1]Test conditions: V_{DDINT}= 2.50 V; HCLK (peripheral clock) frequency = CCLK/2 (core clock/2) frequency; T_{AMB} = 25°C.
[2]Test conditions: V_{DDINT}= 2.65 V; HCLK (peripheral clock) frequency = CCLK/2 (core clock/2) frequency; T_{AMB} = 25°C.
[3]PLL, Core, peripheral clocks, and CLKIN are disabled.
[4]PLL is enabled and Core and peripheral clocks are disabled.
[5]Core CLK is disabled and peripheral clock is enabled.
[6]All instructions execute from internal memory. 50% of the instructions are repeat MACs with dual operand addressing, with changing data fetched using a linear address sequence. 50% of the instructions are type 3 instructions.
[7]All instructions execute from internal memory. 100% of the instructions are MACs with dual operand addressing, with changing data fetched using a linear address sequence.

$$I_{DDINT} = (\%Typical \times I_{DDINT\text{-}TYPICAL}) + (\%Idle \times I_{DDINT\text{-}IDLE}) + (\%Power\ Down \times I_{DDINT\text{-}PWRDWN})$$

TIMING SPECIFICATIONS

This section contains timing information for the DSP's external signals. Use the exact information given. Do not attempt to derive parameters from the addition or subtraction of other information. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added meaningfully to derive longer times.

Switching characteristics specify how the processor changes its signals. No control is possible over this timing; circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics indicate what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Clock In and Clock Out Cycle Timing

Table 9 and Figure 8 describe clock and reset operations. Combinations of CLKIN and clock multipliers must not select core/peripheral clocks in excess of 160/80 MHz for commercial grade and 140/70 MHz for industrial grade, when the peripheral clock rate is one-half the core clock rate. If the peripheral clock rate is equal to the core clock rate, the maximum peripheral clock rate is 80 MHz for both commercial and industrial grade parts. The peripheral clock is supplied to the CLKOUT pins.

When changing from bypass mode to PLL mode, allow 512 HCLK cycles for the PLL to stabilize.

Table 9. Clock In and Clock Out Cycle Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{CKOD}	CLKOUT Delay from CLKIN	0	5.8	ns
t_{CKO}	CLKOUT Period[1]	12.5		ns
Timing Requirements				
t_{CK}	CLKIN Period[2, 3]	10	200	ns
t_{CKL}	CLKIN Low Pulse	4.5		ns
t_{CKH}	CLKIN High Pulse	4.5		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulsewidth Low	$200t_{CLKOUT}$		ns
t_{MSS}	MSELx/BYPASS Stable Before $\overline{\text{RESET}}$ Deasserted Setup	40		µs
t_{MSH}	MSELx/BYPASS Stable After $\overline{\text{RESET}}$ Deasserted Hold	1000		ns
t_{MSD}	MSELx/BYPASS Stable After $\overline{\text{RESET}}$ Asserted		200	ns
t_{PFD}	Flag Output Disable Time After $\overline{\text{RESET}}$ Asserted		10	ns

[1]CLKOUT jitter can be as great as 8 ns when CLKOUT frequency is less than 20 MHz. For frequencies greater than 20 MHz, jitter is less than 1 ns.
[2]In clock multiplier mode and MSEL6–0 set for 1:1 (or CLKIN = CCLK), $t_{CK} = t_{CCLK}$.
[3]In bypass mode, $t_{CK} = t_{CCLK}$.

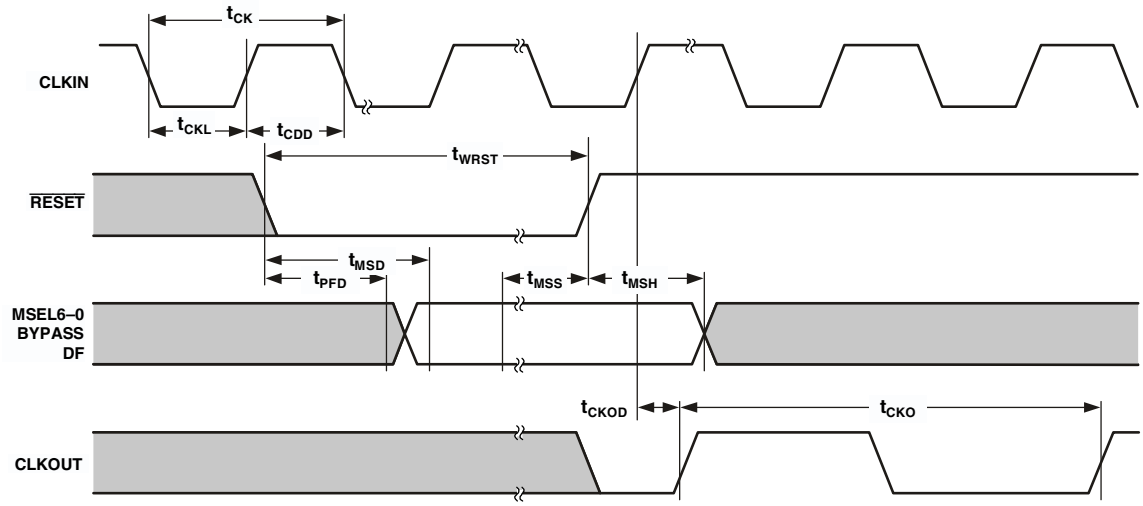

Figure 8. Clock In and Clock Out Cycle Timing

Host Port ALE Mode Write Cycle Timing

Table 15 and Figure 14 describe Host port write operations in Address Latch Enable (ALE) mode. For more information on ACK, Ready, ALE, and ACC mode selection, see the Host port modes description on Page 8.

Table 15. Host Port ALE Mode Write Cycle Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{WHKS1}	$\overline{HWR}$ Asserted to HACK Asserted (Setup, ACK Mode) First Byte	10	$5t_{HCLK}+t_{NH}$[1]	ns
t_{WHKS2}	$\overline{HWR}$ Asserted to HACK Asserted (Setup, ACK Mode)[2]		10	ns
t_{WHKH}	$\overline{HWR}$ Deasserted to HACK Deasserted (Hold, ACK Mode)		10	ns
t_{WHS}	$\overline{HWR}$ Asserted to HACK Asserted (Setup, Ready Mode)		10	ns
t_{WHH}	$\overline{HWR}$ Asserted to HACK Deasserted (Hold, Ready Mode) First Byte	0	$5t_{HCLK}+t_{NH}$[1]	ns
Timing Requirements				
t_{CSAL}	$\overline{HCMS}$ or $\overline{HCIOMS}$ Asserted to HALE Asserted	0		ns
t_{ALPW}	HALE Asserted Pulsewidth	4		ns
t_{ALCSW}	HALE Deasserted to $\overline{HCMS}$ or $\overline{HCIOMS}$ Deasserted	1		ns
t_{WCSW}	$\overline{HWR}$ Deasserted to $\overline{HCMS}$ or $\overline{HCIOMS}$ Deasserted	0		ns
t_{ALW}	HALE Deasserted to $\overline{HWR}$ Asserted	1		ns
t_{WCS}	$\overline{HWR}$ Deasserted (After Last Byte) to $\overline{HCMS}$ or $\overline{HCIOMS}$ Deasserted (Ready for Next Write)	0		ns
t_{HKWD}	HACK Asserted to $\overline{HWR}$ Deasserted (Hold, ACK Mode)	1.5		ns
t_{AALS}	Address Valid to HALE Deasserted (Setup)	2		ns
t_{ALAH}	HALE Deasserted to Address Invalid (Hold)	4		ns
t_{DWS}	Data Valid to $\overline{HWR}$ Deasserted (Setup)	4		ns
t_{WDH}	$\overline{HWR}$ Deasserted to Data Invalid (Hold)	1		ns

[1] t_{NH} are peripheral bus latencies ($n \times t_{HCLK}$); these are internal DSP latencies related to the number of peripheral DMAs attempting to access DSP memory at the same time.

[2] Measurement is for the second, third, or fourth byte of a host write transaction. The quantity of bytes to complete a host write transaction is dependent on the data bus size (8 or 16 bits) and the data type (16 or 24 bits).

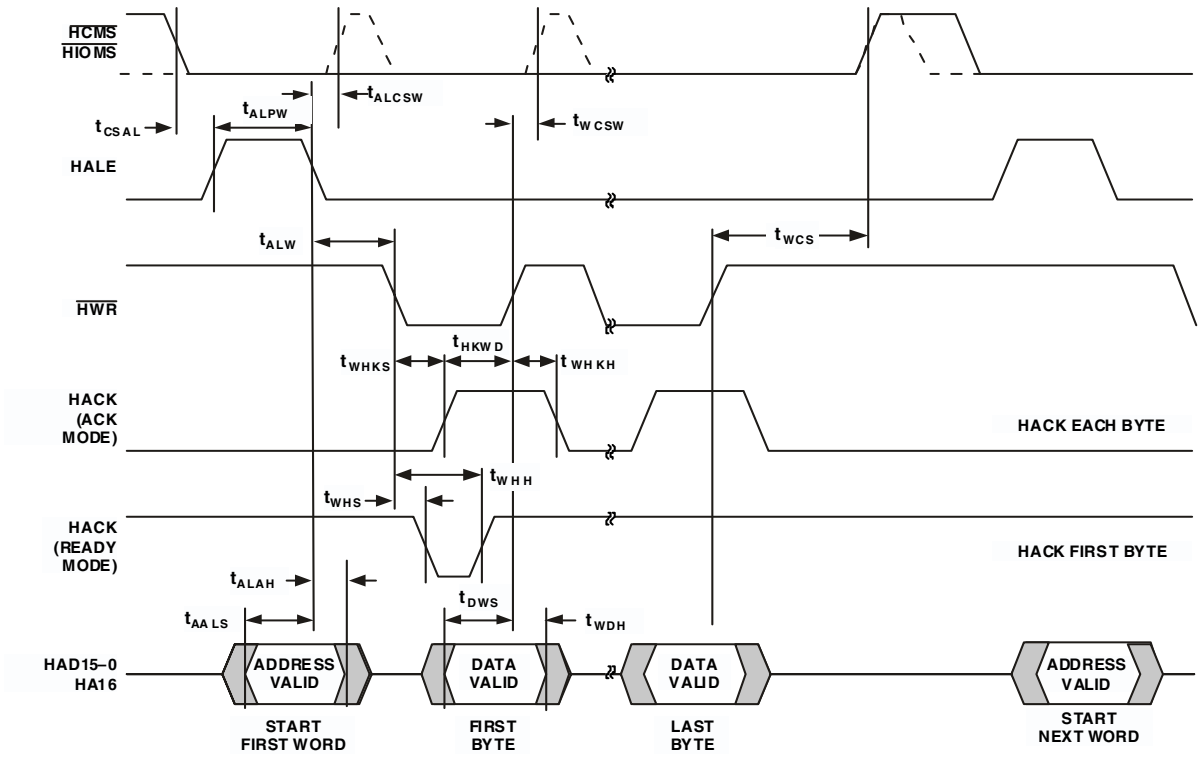

Figure 14. Host Port ALE Mode Write Cycle Timing

Host Port ACC Mode Write Cycle Timing

Table 16 and Figure 15 describe Host port write operations in Address Cycle Control (ACC) mode. For more information on ACK, Ready, ALE, and ACC mode selection, see the Host port modes description on Page 8.

Table 16. Host Port ACC Mode Write Cycle Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{WHKS1}	$\overline{HWR}$ Asserted to HACK Asserted (ACK Mode) First Byte	10	$5t_{HCLK}+t_{NH}$[1]	ns
t_{WHKS2}	$\overline{HWR}$ Asserted to HACK Asserted (Setup, ACK Mode)[2]		12	ns
t_{WHKH}	$\overline{HWR}$ Deasserted to HACK Deasserted (Hold, ACK Mode)		10	ns
t_{WHS}	$\overline{HWR}$ Asserted to HACK Asserted (Setup, Ready Mode)		10	ns
t_{WHH}	$\overline{HWR}$ Asserted to HACK Deasserted (Hold, Ready Mode) First Byte	0	$5t_{HCLK}+t_{NH}$[1]	ns
t_{WSHKS}	$\overline{HWR}$ Asserted to HACK Asserted (Setup) During Address Latch		10	ns
t_{WHHKH}	$\overline{HWR}$ Deasserted to HACK Deasserted (Hold) During Address Latch		10	ns
Timing Requirements				
t_{WAL}	$\overline{HWR}$ Asserted to HALE Deasserted (Delay)	1.5		ns
t_{CSAL}	$\overline{HCMS}$ or $\overline{HCIOMS}$ Asserted to HALE Asserted (Delay)	0		ns
t_{ALCS}	HALE Deasserted to Optional $\overline{HCMS}$ or $\overline{HCIOMS}$ Deasserted	1		ns
t_{WCSW}	$\overline{HWR}$ Deasserted to $\overline{HCMS}$ or $\overline{HCIOMS}$ Deasserted	0		ns
t_{ALW}	HALE Asserted to HWR Asserted	0.5		ns
t_{CSW}	$\overline{HCMS}$ or $\overline{HCIOMS}$ Asserted to $\overline{HWR}$ Asserted	0		ns
t_{WCS}	$\overline{HWR}$ Deasserted (After Last Byte) to $\overline{HCMS}$ or $\overline{HCIOMS}$ Deasserted (Ready for Next Write)	0		ns
t_{ALEW}	HALE Deasserted to HWR Asserted	1		ns
t_{HKWD}	HACK Asserted to $\overline{HWR}$ Deasserted (Hold, ACK Mode)	1.5		ns
t_{ADW}	Address Valid to $\overline{HWR}$ Asserted (Setup)	3		ns
t_{WAD}	$\overline{HWR}$ Deasserted to Address Invalid (Hold)	3		ns
t_{DWS}	Data Valid to $\overline{HWR}$ Deasserted (Setup)	2		ns
t_{WDH}	$\overline{HWR}$ Deasserted to Data Invalid (Hold)	2		ns
t_{HKWAL}	HACK Asserted to $\overline{HWR}$ Deasserted (Hold) During Address Latch[2]	2		ns

[1] t_{NH} are peripheral bus latencies ($n \times t_{HCLK}$); these are internal DSP latencies related to the number of peripheral DMAs attempting to access DSP memory at the same time.

[2] Measurement is for the second, third, or fourth byte of a host write transaction. The quantity of bytes to complete a host write transaction is dependent on the data bus size (8 or 16 bits) and the data type (16 or 24 bits).

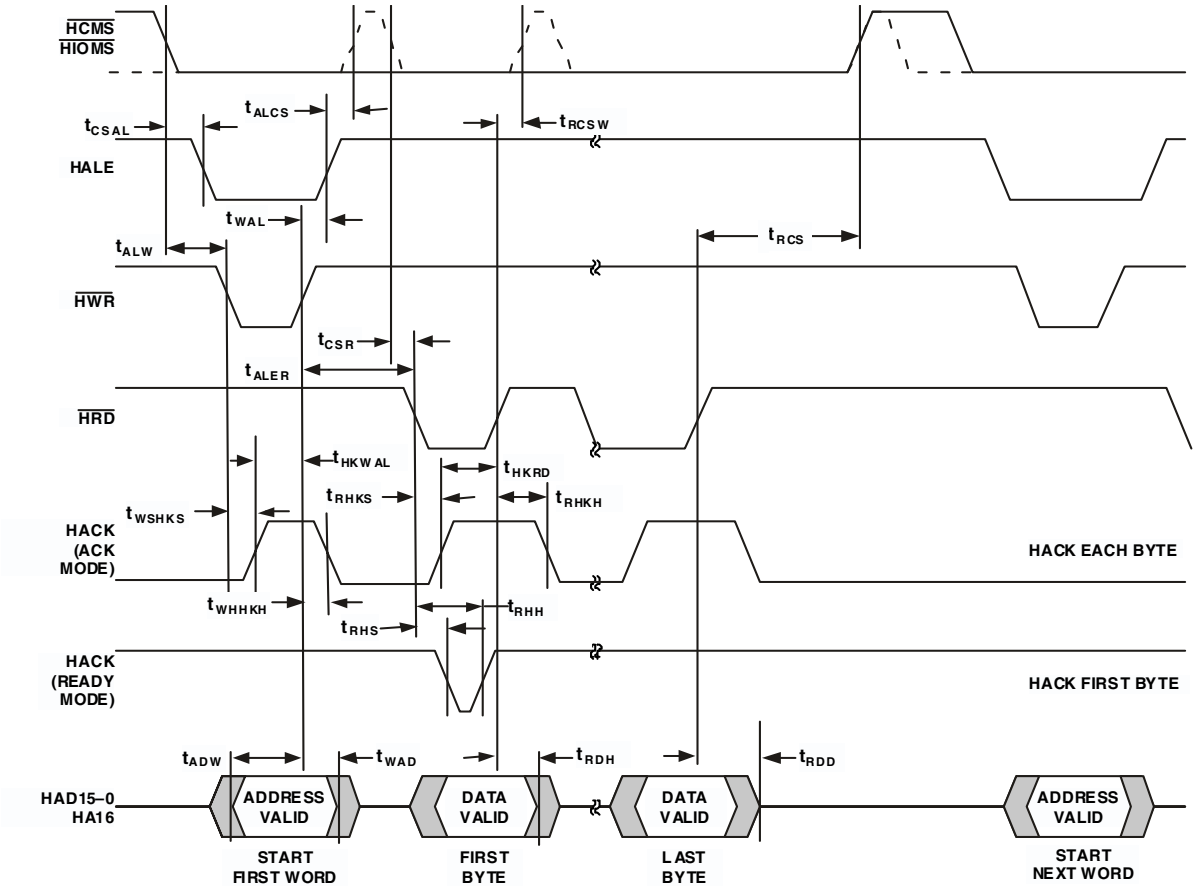

Figure 17. Host Port ACC Mode Read Cycle Timing

Serial Ports

Table 19 and Figure 18 describe SPORT transmit and receive operations, while Figure 19 and Figure 20 describe SPORT Frame Sync operations.

Table 19. Serial Ports[1, 2]

Parameter		Min	Max	Unit
External Clock Timing Requirements				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[3]	4		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[3]	4		ns
t_{SDRE}	Receive Data Setup Before RCLK[3]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[3]	4		ns
t_{SCLKW}	TCLK/RCLK Width	$0.5t_{HCLK}-1$		ns
t_{SCLK}	TCLK/RCLK Period	$2t_{HCLK}$		ns
Internal Clock Timing Requirements				
t_{SFSI}	TFS Setup Before TCLK[4]; RFS Setup Before RCLK[3]	4		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[3]	3		ns
t_{SDRI}	Receive Data Setup Before RCLK[3]	2		ns
t_{HDRI}	Receive Data Hold After RCLK[3]	5		ns
External or Internal Clock Switching Characteristics				
t_{DFSE}	TFS/RFS Delay After TCLK/RCLK (Internally Generated FS)[4]		14	ns
t_{HOFSE}	TFS/RFS Hold After TCLK/RCLK (Internally Generated FS)[4]	3		ns
External Clock Switching Characteristics				
t_{DDTE}	Transmit Data Delay After TCLK[4]		13.4	ns
t_{HDTE}	Transmit Data Hold After TCLK[4]	4		ns
Internal Clock Switching Characteristics				
t_{DDTI}	Transmit Data Delay After TCLK[4]		13.4	ns
t_{HDTI}	Transmit Data Hold After TCLK[4]	4		ns
t_{SCLKIW}	TCLK/RCLK Width	$0.5t_{HCLK}-3.5$	$0.5t_{HCLK}+2.5$	ns
Enable and Three-State[5] Switching Characteristics				
t_{DTENE}	Data Enable from External TCLK[4]	0	12.1	ns
t_{DDTTE}	Data Disable from External TCLK[4]		13	ns
t_{DTENI}	Data Enable from Internal TCLK[4]	0	13	ns
t_{DDTTI}	Data Disable from External TCLK[4]		12	ns
External Late Frame Sync Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFS with MCE=1, MFD=0[6, 7]		10.5	ns
$t_{DTENLFSE}$	Data Enable from Late FS or MCE=1, MFD=0[6, 7]	3.5		ns

[1]To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup-and-hold, 2) data delay and data setup-and-hold, and 3) SCLK width.
[2]Word selected timing for I^2S mode is the same as TFS/RFS timing (normal framing only).
[3]Referenced to sample edge.
[4]Referenced to drive edge.
[5]Only applies to SPORT0/1.
[6]MCE=1, TFS enable, and TFS valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.
[7]If external RFSD/TFS setup to RCLK/TCLK>$0.5t_{LSCK}$, $t_{DDTLSCK}$ and $t_{DTENLSCK}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

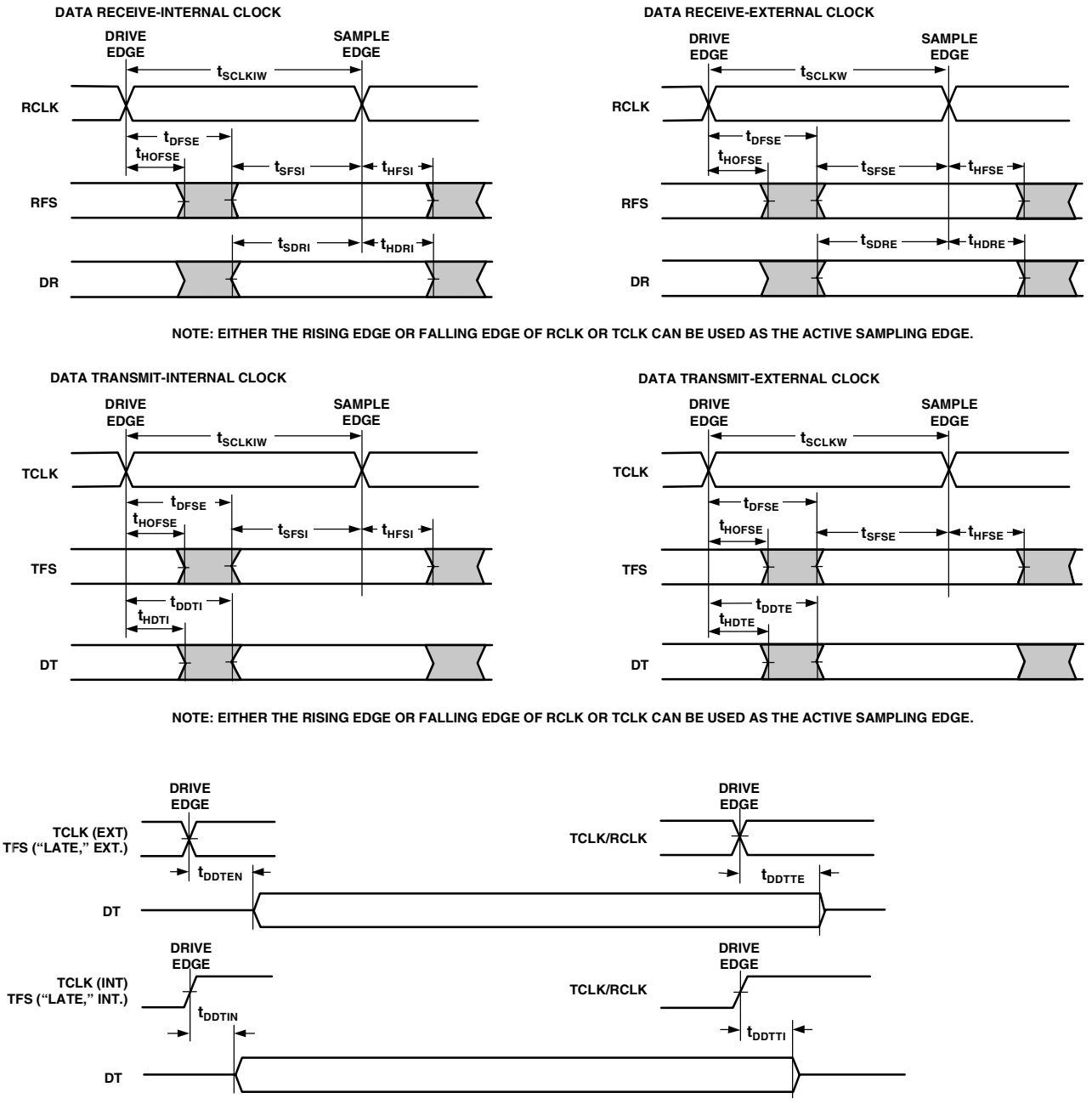

Figure 18. Serial Ports

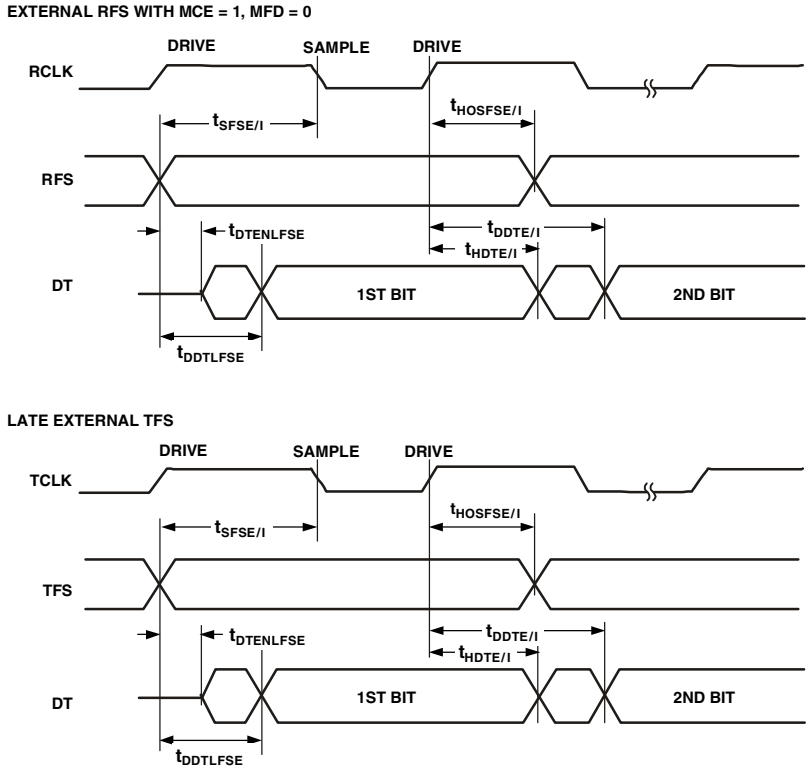

Figure 19. Serial Ports—External Late Frame Sync (Frame Sync Setup > 0.5t_{SCLK})

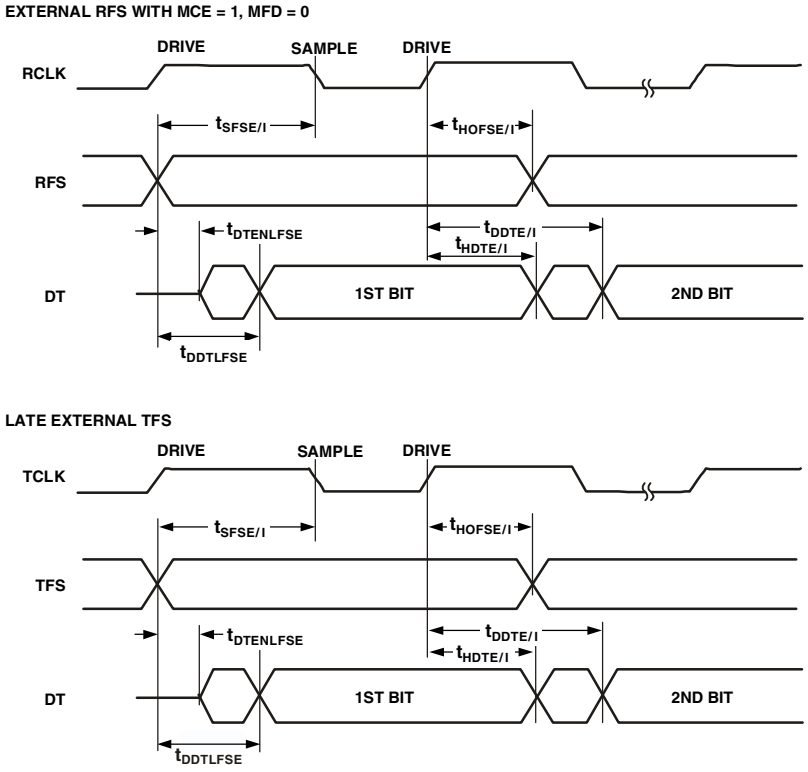

Figure 20. Serial Ports—External Late Frame Sync (Frame Sync Setup < 0.5t_{HCLK})

JTAG Test And Emulation Port Timing

Table 22 and Figure 24 describe JTAG port operations.

Table 22. JTAG Port Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		8	ns
t_{DSYS}	System Outputs Delay After TCK Low[1]	0	22	ns
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High		4	ns
t_{HTAP}	TDI, TMS Hold After TCK High		4	ns
t_{SSYS}	System Inputs Setup Before TCK Low[2]		4	ns
t_{HSYS}	System Inputs Hold After TCK Low[2]		5	ns
t_{TRSTW}	$\overline{TRST}$ Pulsewidth[3]	$4t_{TCK}$		ns

[1]System Outputs = DATA15–0, ADDR21–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, ACK, CLKOUT, $\overline{BG}$, PF7–0, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$.
[2]System Inputs = DATA15–0, ADDR21–0, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{BR}$, $\overline{BG}$, PF7–0, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, CLKIN, $\overline{RESET}$.
[3]50 MHz max.

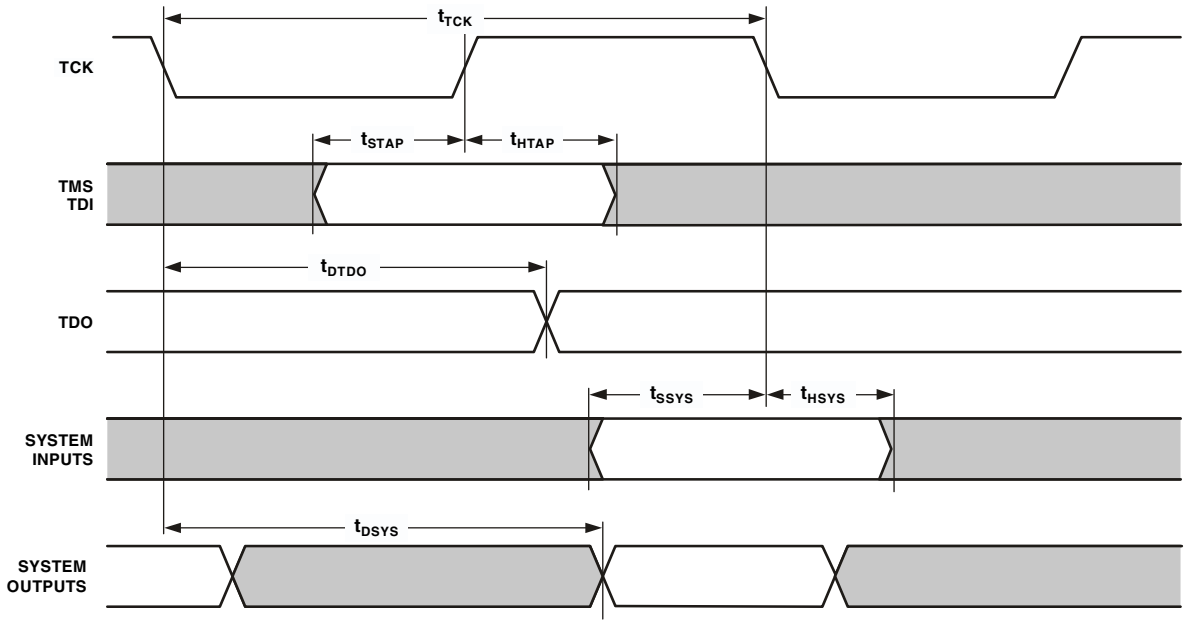

Figure 24. JTAG Port Timing

144-Lead LQFP Pinout

Table 25 lists the LQFP pinout by signal name. Table 26 lists the LQFP pinout by pin.

Table 25. 144-Lead LQFP Pins (Alphabetically by Signal)

Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.
A0	84	BYPASS	72	GND	33	$\overline{\text{HCMS}}$	27	TCLK1	65
A1	85	CLKIN	132	GND	54	$\overline{\text{HCIOMS}}$	28	TCLK2	47
A2	86	CLKOUT	130	GND	55	$\overline{\text{HRD}}$	31	TDI	75
A3	87	D0	123	GND	77	$\overline{\text{HWR}}$	32	TDO	74
A4	88	D1	124	GND	80	$\overline{\text{IOMS}}$	114	TFS0	59
A5	89	D2	125	GND	94	$\overline{\text{MS0}}$	115	TFS1	66
A6	91	D3	126	GND	105	$\overline{\text{MS1}}$	116	TFS2	48
A7	92	D4	128	GND	129	$\overline{\text{MS2}}$	117	TMR0	43
A8	93	D5	135	GND	134	$\overline{\text{MS3}}$	119	TMR1	44
A9	95	D6	136	HA16	23	OPMODE	83	TMR2	45
A10	96	D7	137	HACK	26	PF0	34	TMS	76
A11	97	D8	138	HACK_P	24	PF1	35	$\overline{\text{TRST}}$	79
A12	98	D9	139	HAD0	3	PF2	36	TXD	53
A13	99	D10	140	HAD1	4	PF3	37	V_{DDEXT}	13
A14	101	D11	141	HAD2	6	PF4	38	V_{DDEXT}	25
A15	102	D12	142	HAD3	7	PF5	39	V_{DDEXT}	40
A16	103	D13	144	HAD4	8	PF6	41	V_{DDEXT}	63
A17	104	D14	1	HAD5	9	PF7	42	V_{DDEXT}	90
A18	106	D15	2	HAD6	10	RCLK0	61	V_{DDEXT}	100
A19	107	DR0	60	HAD7	11	RCLK1	68	V_{DDEXT}	118
A20	108	DR1	67	HAD8	12	RCLK2	50	V_{DDEXT}	131
A21	109	DR2	49	HAD9	14	$\overline{\text{RD}}$	122	V_{DDEXT}	143
ACK	120	DT0	56	HAD10	15	$\overline{\text{RESET}}$	73	V_{DDINT}	19
$\overline{\text{BG}}$	111	DT1	64	HAD11	17	RFS0	62	V_{DDINT}	58
$\overline{\text{BGH}}$	110	DT2	46	HAD12	18	RFS1	69	V_{DDINT}	82
BMODE0	70	$\overline{\text{EMU}}$	81	HAD13	20	RFS2	51	V_{DDINT}	127
BMODE1	71	GND	5	HAD14	21	RXD	52	$\overline{\text{WR}}$	121
$\overline{\text{BMS}}$	113	GND	16	HAD15	22	TCK	78	XTAL	133
$\overline{\text{BR}}$	112	GND	29	HALE	30	TCLK0	57		

144-Lead Mini-BGA Pinout

Table 27 lists the mini-BGA pinout by signal name. Table 28 lists the mini-BGA pinout by ball number.

Table 27. 144-Lead Mini-BGA Pins (Alphabetically by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
A0	J11	BYPASS	M11	GND	F7	HALE	J1	TCLK0	J6
A1	H9	CLKIN	A5	GND	F8	$\overline{\text{HCIOMS}}$	J3	TCLK1	M9
A2	H10	CLKOUT	C6	GND	F9	$\overline{\text{HCMS}}$	H1	TCLK2	K5
A3	G12	D0	D7	GND	G4	$\overline{\text{HRD}}$	J2	TDI	K12
A4	H11	D1	A7	GND	G5	$\overline{\text{HWR}}$	K2	TDO	L11
A5	G10	D2	C7	GND	G6	$\overline{\text{IOMS}}$	E8	TFS0	M8
A6	F12	D3	A6	GND	H5	$\overline{\text{MS0}}$	D9	TFS1	J8
A7	G11	D4	B7	GND	L6	$\overline{\text{MS1}}$	A9	TFS2	M5
A8	F10	D5	A4	GND	M1	$\overline{\text{MS2}}$	C9	TMR0	K4
A9	F11	D6	C5	GND	M12	$\overline{\text{MS3}}$	D8	TMR1	L4
A10	E12	D7	B5	HACK	H3	OPMODE	H12	TMR2	J4
A11	E11	D8	D5	HACK_P	G1	PF0	K1	TMS	K10
A12	E10	D9	A3	HAD0	C1	PF1	L1	$\overline{\text{TRST}}$	J12
A13	E9	D10	C4	HAD1	B3	PF2	M2	TXD	M7
A14	D11	D11	B4	HAD2	C2	PF3	L2	V_{DDEXT}	E5
A15	D10	D12	C3	HAD3	D1	PF4	M3	V_{DDEXT}	E6
A16	D12	D13	A2	HAD4	D4	PF5	L3	V_{DDEXT}	F5
A17	C11	D14	B1	HAD5	D3	PF6	K3	V_{DDEXT}	F6
A18	C12	D15	B2	HAD6	D2	PF7	M4	V_{DDEXT}	G7
A19	B12	DR0	L7	HAD7	E1	RCLK0	K7	V_{DDEXT}	G8
A20	B11	DR1	K9	HAD8	E4	RCLK1	J9	V_{DDEXT}	H7
A21	A11	DR2	L5	HAD9	E2	RCLK2	J5	V_{DDEXT}	H8
ACK	A8	DT0	H6	HAD10	F1	$\overline{\text{RD}}$	B8	V_{DDINT}	D6
$\overline{\text{BG}}$	C10	DT1	L8	HAD11	E3	$\overline{\text{RESET}}$	L12	V_{DDINT}	F4
$\overline{\text{BGH}}$	B10	DT2	H4	HAD12	F2	RFS0	K8	V_{DDINT}	G9
BMODE0	L10	$\overline{\text{EMU}}$	J10	HAD13	G2	RFS1	M10	V_{DDINT}	J7
BMODE1	L9	GND	A1	HAD14	F3	RFS2	M6	$\overline{\text{WR}}$	C8
$\overline{\text{BMS}}$	A10	GND	A12	HAD15	G3	RXD	K6	XTAL	B6
$\overline{\text{BR}}$	B9	GND	E7	HA16	H2	TCK	K11		

Table 28. 144-Lead Mini-BGA Pins (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	C6	CLKOUT	E11	A11	H4	DT2	K9	DR1
A2	D13	C7	D2	E12	A10	H5	GND	K10	TMS
A3	D9	C8	$\overline{WR}$	F1	HAD10	H6	DT0	K11	TCK
A4	D5	C9	$\overline{MS2}$	F2	HAD12	H7	V_{DDEXT}	K12	TDI
A5	CLKIN	C10	$\overline{BG}$	F3	HAD14	H8	V_{DDEXT}	L1	PF1
A6	D3	C11	A17	F4	V_{DDINT}	H9	A1	L2	PF3
A7	D1	C12	A18	F5	V_{DDEXT}	H10	A2	L3	PF5
A8	ACK	D1	HAD3	F6	V_{DDEXT}	H11	A4	L4	TMR1
A9	$\overline{MS1}$	D2	HAD6	F7	GND	H12	OPMODE	L5	DR2
A10	$\overline{BMS}$	D3	HAD5	F8	GND	J1	HALE	L6	GND
A11	A21	D4	HAD4	F9	GND	J2	$\overline{HRD}$	L7	DR0
A12	GND	D5	D8	F10	A8	J3	$\overline{HCIOMS}$	L8	DT1
B1	D14	D6	V_{DDINT}	F11	A9	J4	TMR2	L9	BMODE1
B2	D15	D7	D0	F12	A6	J5	RCLK2	L10	BMODE0
B3	HAD1	D8	$\overline{MS3}$	G1	HACK_P	J6	TCLK0	L11	TDO
B4	D11	D9	$\overline{MS0}$	G2	HAD13	J7	V_{DDINT}	L12	$\overline{RESET}$
B5	D7	D10	A15	G3	HAD15	J8	TFS1	M1	GND
B6	XTAL	D11	A14	G4	GND	J9	RCLK1	M2	PF2
B7	D4	D12	A16	G5	GND	J10	$\overline{EMU}$	M3	PF4
B8	$\overline{RD}$	E1	HAD7	G6	GND	J11	A0	M4	PF7
B9	$\overline{BR}$	E2	HAD9	G7	V_{DDEXT}	J12	$\overline{TRST}$	M5	TFS2
B10	$\overline{BGH}$	E3	HAD11	G8	V_{DDEXT}	K1	PF0	M6	RFS2
B11	A20	E4	HAD8	G9	V_{DDINT}	K2	$\overline{HWR}$	M7	TXD
B12	A19	E5	V_{DDEXT}	G10	A5	K3	PF6	M8	TFS0
C1	HAD0	E6	V_{DDEXT}	G11	A7	K4	TMR0	M9	TCLK1
C2	HAD2	E7	GND	G12	A3	K5	TCLK2	M10	RFS1
C3	D12	E8	$\overline{IOMS}$	H1	$\overline{HCMS}$	K6	RXD	M11	BYPASS
C4	D10	E9	A13	H2	HA16	K7	RCLK0	M12	GND
C5	D6	E10	A12	H3	HACK	K8	RFS0		