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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	- ·
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1507-i-ss

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3.3.2 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.3.3 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

3.3.3.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.6.2** "Linear Data Memory" for more information.

3.3.4 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-2: BANKED MEMORY PARTITIONING

7-bit Bank Offset	Memory Region
00h	Core Registers
0Bh	(12 bytes)
0Ch	Special Function Registers
1Fh	(20 bytes maximum)
6Fh	General Purpose RAM (80 bytes maximum)
70h	Common RAM
7Fh	(16 bytes)

3.4 PCL and PCLATH

The Program Counter (PC) is 15 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<14:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 3-3 shows the five situations for the loading of the PC.





3.4.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<14:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper seven bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 15 bits of the program counter will change to the values contained in the PCLATH register.

3.4.2 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to Application Note AN556, *"Implementing a Table Read"* (DS00556).

3.4.3 COMPUTED FUNCTION CALLS

A computed function CALL allows programs to maintain tables of functions and provide another way to execute state machines or look-up tables. When performing a table read using a computed function CALL, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

If using the CALL instruction, the PCH<2:0> and PCL registers are loaded with the operand of the CALL instruction. PCH<6:3> is loaded with PCLATH<6:3>.

The CALLW instruction enables computed calls by combining PCLATH and W to form the destination address. A computed CALLW is accomplished by loading the W register with the desired address and executing CALLW. The PCL register is loaded with the value of W and PCH is loaded with PCLATH.

3.4.4 BRANCHING

The branching instructions add an offset to the PC. This allows relocatable code and code that crosses page boundaries. There are two forms of branching, BRW and BRA. The PC will have incremented to fetch the next instruction in both cases. When using either branching instruction, a PCL memory boundary may be crossed.

If using BRW, load the W register with the desired unsigned address and execute BRW. The entire PC will be loaded with the address PC + 1 + W.

If using BRA, the entire PC will be loaded with PC + 1 +, the signed value of the operand of the BRA instruction.





3.5.2 OVERFLOW/UNDERFLOW RESET

If the STVREN bit in Configuration Words is programmed to '1', the device will be reset if the stack is PUSHed beyond the sixteenth level or POPed beyond the first level, setting the appropriate bits (STKOVF or STKUNF, respectively) in the PCON register.

3.6 Indirect Addressing

The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the File Select Registers (FSR). If the FSRn address specifies one of the two INDFn registers, the read will return '0' and the write will not occur (though Status bits may be affected). The FSRn register value is created by the pair FSRnH and FSRnL.

The FSR registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- Traditional Data Memory
- Linear Data Memory
- Program Flash Memory

5.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bits of the OSCCON register. The following clock sources can be selected using the SCS bits:

- Default system oscillator determined by FOSC bits in Configuration Words
- Internal Oscillator Block (INTOSC)

5.3.1 SYSTEM CLOCK SELECT (SCS) BITS

The System Clock Select (SCS) bits of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bits of the OSCCON register = 00, the system clock source is determined by value of the FOSC<1:0> bits in the Configuration Words.
- When the SCS bits of the OSCCON register = 01, the system clock source is the secondary oscillator.
- When the SCS bits of the OSCCON register = 1x, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<3:0>

TABLE 5-2: OSCILLATOR SWITCHING DELAYS

bits of the OSCCON register. After a Reset, the SCS bits of the OSCCON register are always cleared.

When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 5-2.

5.3.2 CLOCK SWITCHING BEFORE SLEEP

When clock switching from an old clock to a new clock is requested just prior to entering Sleep mode, it is necessary to confirm that the switch is complete before the SLEEP instruction is executed. Failure to do so may result in an incomplete switch and consequential loss of the system clock altogether. Clock switching is confirmed by monitoring the clock status bits in the OSCSTAT register. Switch confirmation can be accomplished by sensing that the ready bit for the new clock is set or the ready bit for the old clock is cleared. For example, when switching between the internal oscillator with the PLL and the internal oscillator without the PLL, monitor the PLLR bit. When PLLR is set, the switch to 32 MHz operation is complete. Conversely, when PPLR is cleared, the switch from 32 MHz operation to the selected internal clock is complete.

Switch From	Switch To	Oscillator Delay		
	LFINTOSC	1 cycle of each clock source		
Any clock source	HFINTOSC	2 μs (approx.)		
	ECH, ECM, ECL	2 cycles		

8.3 Register Definitions: Voltage Regulator Control

REGISTER 8-1: VREGCON: VOLTAGE REGULATOR CONTROL REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-1/1
	—	—	—	—	—	VREGPM	Reserved
bit 7							bit 0
I a manual.							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 1	VREGPM: Voltage Regulator Power Mode Selection bit
	1 = Low-Power Sleep mode enabled in Sleep ⁽²⁾

- Draws lowest current in Sleep, slower wake-up
 - 0 = Normal Power mode enabled in Sleep⁽²⁾
 Draws higher current in Sleep, faster wake-up
- bit 0 **Reserved:** Read as '1'. Maintain this bit set.

Note 1: PIC16F1507 only.

2: See Section 25.0 "Electrical Specifications".

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	64
IOCAF	—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	110
IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	110
IOCAP	—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	110
IOCBF	IOCBF7	IOCBF6	IOCBF5	IOCBF4	—	—	—	—	111
IOCBN	IOCBN7	IOCBN6	IOCBN5	IOCBN4	_	_	_	_	111
IOCBP	IOCBP7	IOCBP6	IOCBP5	IOCBP4	_	_	_	_	111
PIE1	TMR1GIE	ADIE	_	_	_	_	TMR2IE	TMR1IE	65
PIE2	—	—	—	—	—	NCO1IE	—	—	66
PIE3	—	—	—	—	—	—	CLC2IE	CLC1IE	67
PIR1	TMR1GIF	ADIF	—	—	—	—	TMR2IF	TMR1IF	68
PIR2	—	—	—	—	—	NCO1IF	—	—	69
PIR3	—	_	_	_	_	—	CLC2IF	CLC1IF	70
STATUS	—	—	—	TO	PD	Z	DC	С	17
WDTCON	—	—		V	VDTPS<4:0	>		SWDTEN	77

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Legend: — = unimplemented, read as '0'. Shaded cells are not used in Power-Down mode.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	—		IRCF<3:0>				SCS<1:0>		49
PCON	STKOVF	STKUNF	_	RWDT	RMCLR	RI	POR	BOR	57
STATUS	—	—	-	TO	PD	Z	DC	С	17
WDTCON	_	_		WDTPS<4:0>					

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Watchdog Timer.

TABLE 9-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
	13:8	—	—	—	—	CLKOUTEN	BORE	N<1:0>	_	20
CONFIGT	7:0	CP	MCLRE	PWRTE	WDTE<1:0>		_	FOSC	<1:0>	38

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Watchdog Timer.





15.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive

FIGURE 15-1: ADC BLOCK DIAGRAM

approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 15-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.



ADC Clock	Period (TAD)		Device Frequency (Fosc)					
ADC Clock Source	ADCS<2:0	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz		
Fosc/2	000	100 ns	125 ns	250 ns	500 ns	2.0 μs		
Fosc/4	100	200 ns	250 ns	500 ns	1.0 μs	4.0 μs		
Fosc/8	001	400 ns	500 ns	1.0 μs	2.0 μs	8.0 μs		
Fosc/16	101	800 ns	1.0 μs	2.0 μs	4.0 μs	16.0 μs		
Fosc/32	010	1.6 μs	2.0 μs	4.0 μs	8.0 μs	32.0 μs		
Fosc/64	110	3.2 μs	4.0 μs	8.0 μs	16.0 μs	64.0 μs		
FRC	x11	1.0-6.0 μs	1.0-6.0 μs	1.0-6.0 μs	1.0-6.0 μs	1.0-6.0 μs		

TABLE 15-1: ADC CLOCK PERIOD (TAD) Vs. DEVICE OPERATING FREQUENCIES

Legend: Shaded cells are outside of recommended range.

Note: The TAD period when using the FRC clock source can fall within a specified range, (see TAD parameter). The TAD period when using the FOSC-based clock source can be configured for a more precise TAD period. However, the FRC clock source must be used when conversions are to be performed with the device in Sleep mode.



FIGURE 15-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES

16.2 Register Definitions: Option Register

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1		
WPUEN	INTEDG	TMR0CS	TMR0SE	PSA		PS<2:0>			
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	e bit	U = Unimpler	mented bit, read	d as '0'			
u = Bit is unch	nanged	x = Bit is unl	known	-n/n = Value a	at POR and BC	R/Value at all c	other Resets		
'1' = Bit is set		ʻ0' = Bit is cl	eared						
bit 7	WPUEN: We	ak Pull-Up En	able bit						
	1 = All weak	pull-ups are di	sabled (excep	t MCLR, if it is	enabled)				
	0 = Weak pu	II-ups are enal	bled by individu	ial WPUx latch	values				
bit 6	INTEDG: Inte	errupt Edge Se	elect bit						
	1 = Interrupt	on rising edge	of INI pin						
hit 5		on laining cugo	urco Soloct bit						
bit 5	1 = Transition	n on TOCKI nir							
	0 = Internal ii	nstruction cycl	e clock (Fosc/	4)					
bit 4	TMR0SE: Timer0 Source Edge Select bit								
	1 = Incremen	nt on high-to-lo	w transition or	1 TOCKI pin					
	0 = Incremen	nt on low-to-hig	gh transition or	1 TOCKI pin					
bit 3	PSA: Presca	ler Assignmer	it bit						
	1 = Prescale	r is not assign	ed to the Time	r0 module					
	0 = Prescale	r is assigned to	o the Timer0 m	odule					
bit 2-0	PS<2:0>: Pre	escaler Rate S	elect bits						
	Bit	Value Timer) Rate						
	(000 1:	2						
	(001 1:	4						
	(ช 16						
		100 1:	32						
		101 1 :	64						

REGISTER 16-1: OPTION_REG: OPTION REGISTER

TABLE 16-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

1:128

1:256

110

111

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON2		TRIGSI	EL<3:0>		—		—	_	125
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	64
OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA		PS<2:0>		133
TMR0	Holding Register for the 8-bit Timer0 Count					131*			
TRISA	—	—	TRISA5	TRISA4	_(1)	TRISA2	TRISA1	TRISA0	98

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the Timer0 module. * Page provides register information.

Note 1: Unimplemented, read as '1'.



TMR1GE	
T1GPOL	
T1GSPM	
T1GGO/ Set by software DONE Counting enabled on rising edge of T1C	Cleared by hardware on falling edge of T1GVAL
t1g_in	
T1GVAL	
Timer1 N N +	N + 2
TMR1GIF Cleared by software	Cleared by Set by hardware on falling edge of T1GVAL

19.1 PWMx Pin Configuration

All PWM outputs are multiplexed with the PORT data latch. The user must configure the pins as outputs by clearing the associated TRIS bits.

Note:	Clearing the PWMxOE bit will relinquish
	control of the PWMx pin.

19.1.1 FUNDAMENTAL OPERATION

The PWM module produces a 10-bit resolution output. Timer2 and PR2 set the period of the PWM. The PWMxDCL and PWMxDCH registers configure the duty cycle. The period is common to all PWM modules, whereas the duty cycle is independently controlled.

Note:	The Timer2 postscaler is not used in the
	determination of the PWM frequency. The
	postscaler could be used to have a servo
	update rate at a different frequency than
	the PWM output.

All PWM outputs associated with Timer2 are set when TMR2 is cleared. Each PWMx is cleared when TMR2 is equal to the value specified in the corresponding PWMxDCH (8 MSb) and PWMxDCL<7:6> (2 LSb) registers. When the value is greater than or equal to PR2, the PWM output is never cleared (100% duty cycle).

Note:	The PWMxDCH and PWMxDCL registers							
	are double buffered. The buffers are							
	updated when Timer2 matches PR2. Care							
	should be taken to update both registers							
	before the timer match occurs.							

19.1.2 PWM OUTPUT POLARITY

The output polarity is inverted by setting the PWMxPOL bit of the PWMxCON register.

19.1.3 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 19-1.

EQUATION 19-1: PWM PERIOD

 $PWM Period = [(PR2) + 1] \bullet 4 \bullet Tosc \bullet$ (TMR2 Prescale Value)

Note: Tosc = 1/Fosc

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The PWM output is active. (Exception: When the PWM duty cycle = 0%, the PWM output will remain inactive.)
- The PWMxDCH and PWMxDCL register values are latched into the buffers.

Note:	The Timer2 postscaler has no effect on
	the PWM operation.

19.1.4 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to the PWMxDCH and PWMxDCL register pair. The PWMxDCH register contains the eight MSbs and the PWMxDCL<7:6>, the two LSbs. The PWMxDCH and PWMxDCL registers can be written to at any time.

Equation 19-2 is used to calculate the PWM pulse width.

Equation 19-3 is used to calculate the PWM duty cycle ratio.

EQUATION 19-2: PULSE WIDTH

 $Pulse Width = (PWMxDCH:PWMxDCL<7:6>) \bullet$

TOSC • (TMR2 Prescale Value)

Note: Tosc = 1/Fosc

EQUATION 19-3: DUTY CYCLE RATIO

$$Duty Cycle Ratio = \frac{(PWMxDCH:PWMxDCL<7:6>)}{4(PR2+1)}$$

The 8-bit timer TMR2 register is concatenated with the two Least Significant bits of 1/Fosc, adjusted by the Timer2 prescaler to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

Figure 19-2 shows a waveform of the PWM signal when the duty cycle is set for the smallest possible pulse.

FIGURE 19-2: PWM OUTPUT



22.0 COMPLEMENTARY WAVEFORM GENERATOR (CWG) MODULE

The Complementary Waveform Generator (CWG) produces a complementary waveform with dead-band delay from a selection of input sources.

The CWG module has the following features:

- Selectable dead-band clock source control
- · Selectable input sources
- · Output enable control
- · Output polarity control
- Dead-band control with independent 6-bit rising and falling edge dead-band counters
- Auto-shutdown control with:
- Selectable shutdown sources
- Auto-restart enable
- Auto-shutdown pin override control

22.1 Fundamental Operation

The CWG generates two output waveforms from the selected input source.

The off-to-on transition of each output can be delayed from the on-to-off transition of the other output, thereby, creating a time delay immediately where neither output is driven. This is referred to as dead time and is covered in **Section 22.5 "Dead-Band Control"**. A typical operating waveform, with dead band, generated from a single input signal is shown in Figure 22-2.

It may be necessary to guard against the possibility of circuit faults or a feedback event arriving too late or not at all. In this case, the active drive must be terminated before the Fault condition causes damage. This is referred to as auto-shutdown and is covered in **Section 22.9 "Auto-Shutdown Control"**.

22.2 Clock Source

The CWG module allows the following clock sources to be selected:

- Fosc (system clock)
- HFINTOSC (16 MHz only)

The clock sources are selected using the G1CS0 bit of the CWGxCON0 register (Register 22-1).

22.3 Selectable Input Sources

The CWG generates the output waveforms from the input sources in Table 22-1.

TABLE 22-1: SELECTABLE INPUT SOURCES

Source Peripheral	Signal Name
PWM1	PWM1_out
PWM2	PWM2_out
PWM3	PWM3_out
PWM4	PWM4_out
NCO1	NCO1_out
CLC1	LC1_out

The input sources are selected using the GxIS<2:0> bits in the CWGxCON1 register (Register 22-2).

22.4 Output Control

Immediately after the CWG module is enabled, the complementary drive is configured with both CWGxA and CWGxB drives cleared.

22.4.1 OUTPUT ENABLES

Each CWG output pin has individual output enable control. Output enables are selected with the GxOEA and GxOEB bits of the CWGxCON0 register. When an output enable control is cleared, the module asserts no control over the pin. When an output enable is set, the override value or active PWM waveform is applied to the pin per the port priority selection. The output pin enables are dependent on the module enable bit, GxEN. When GxEN is cleared, CWG output enables and CWG drive levels have no effect.

22.4.2 POLARITY CONTROL

The polarity of each CWG output can be selected independently. When the output polarity bit is set, the corresponding output is active-high. Clearing the output polarity bit configures the corresponding output as active-low. However, polarity does not affect the override levels. Output polarity is selected with the GxPOLA and GxPOLB bits of the CWGxCON0 register.

LSLF	Logical Left Shift				
Syntax:	[<i>label</i>]LSLF f{,d}				
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$				
Operation:	$(f<7>) \rightarrow C$ $(f<6:0>) \rightarrow dest<7:1>$ $0 \rightarrow dest<0>$				
Status Affected:	C, Z				
Description:	The contents of register 'f' are shifted one bit to the left through the Carry flag. A '0' is shifted into the LSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.				
	C ← register f ← 0				

LSRF	Logical Right Shift				
Syntax:	[<i>label</i>]LSRF f{,d}				
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$				
Operation:	$\begin{array}{l} 0 \rightarrow dest < 7 > \\ (f < 7:1 >) \rightarrow dest < 6:0 >, \\ (f < 0 >) \rightarrow C, \end{array}$				
Status Affected:	C, Z				
Description:	The contents of register 'f' are shifted one bit to the right through the Carry flag. A '0' is shifted into the MSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.				
	0 → register f → C				

MOVF	Move f
Syntax:	[<i>label</i>] MOVF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	$(f) \rightarrow (dest)$
Status Affected:	Z
Description:	The contents of register f is moved to a destination dependent upon the status of d. If $d = 0$, destination is W register. If $d = 1$, the destination is file register f itself. $d = 1$ is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
Example:	MOVF FSR, 0
	After Instruction

Instruction W = value in FSR register Z = 1

PIC16LF1507 PIC16F1507		Standard Operating Conditions (unless otherwise stated)						
Param. Device					Unite	Conditions		
No.	Characteristics	win.	турт	wax.	Units	Vdd	Note	
D019A		-	1030	1500	μA	3.0	Fosc = 20 MHz, External Clock (ECH), High-Power mode	
D019A		_	1060	1600	μA	3.0	Fosc = 20 MHz,	
		—	1220	1800	μA	5.0	External Clock (ECH), High-Power mode	
D019B		—	6	16	μA	1.8	Fosc = 32 kHz,	
		—	8	22	μA	3.0	External Clock (ECL), Low-Power mode	
D019B		—	13	28	μA	2.3	Fosc = 32 kHz,	
		—	15	31	μA	3.0	External Clock (ECL),	
		—	16	36	μA	5.0	Low-Power mode	
D019C		—	19	35	μA	1.8	Fosc = 500 kHz,	
		— 32		55	μA	3.0	External Clock (ECL), Low-Power mode	
D019C		_	31	52	μA	2.3	Fosc = 500 kHz,	
		_	38	65	μA	3.0	External Clock (ECL),	
		—	44	74	μA	5.0		

TABLE 25-2: SUPPLY CURRENT (IDD)^(1,2) (CONTINUED)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to Vss; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.











FIGURE 26-35: VOH vs. IOH OVER TEMPERATURE, VDD = 1.8V, PIC16LF1507 ONLY









FIGURE 26-50: LFINTOSC FREQUENCY OVER VDD AND TEMPERATURE, PIC16F1507 ONLY





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VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	е	1.27 BSC		
Overall Height	Α	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	12.80 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	С	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

For the most current package drawings, please see the Microchip Packaging Specification located at

Notes:

Note:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-094C Sheet 2 of 2