# Renesas Electronics America Inc - R5F107ACGSP#X0 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

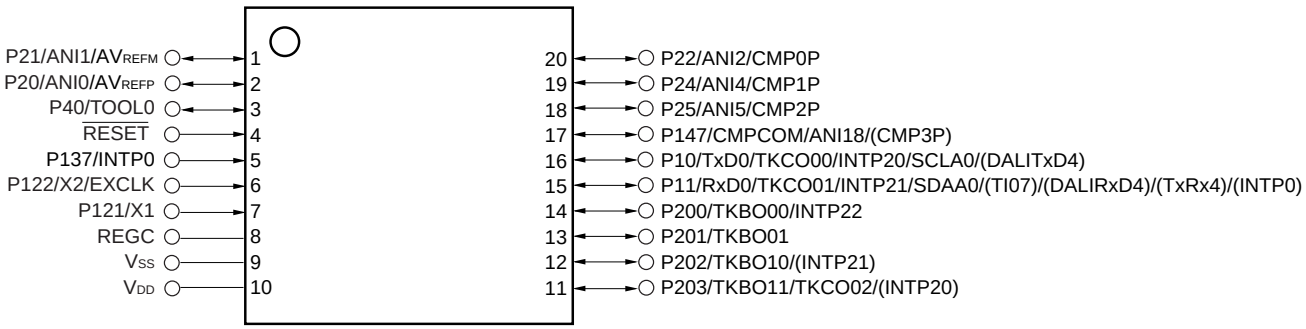
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 11x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 30-LSSOP (0.240", 6.10mm Width) |
| Supplier Device Package | 30-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f107acgsp-x0 |

## 1.3 Pin Configuration (Top View)

### 1.3.1 20-pin products

- 20-pin plastic LSSOP (4.4 x 6.5)




**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

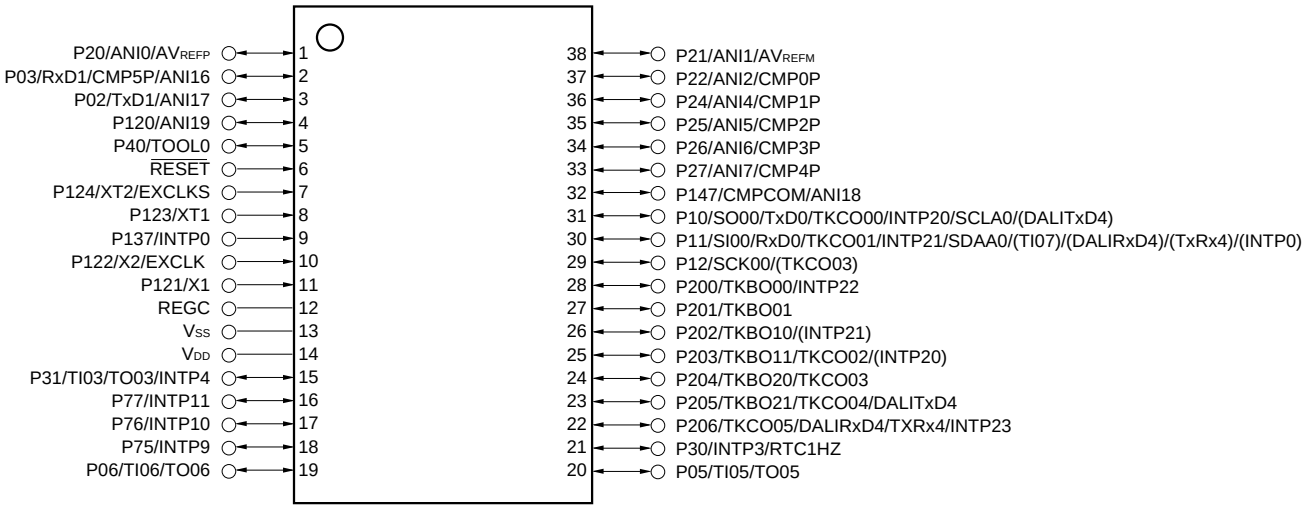
**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1)** and **Figure 15-20 Format of Input Switch Control Register (ISC) in the RL78/I1A User's Manual**.

**3.** The shared function CMP3P can be assigned to P147 by setting the CMPSEL0 bit in the comparator input switch control register (CMPSEL).

### 1.3.3 38-pin products

- 38-pin plastic SSOP (7.62 mm (300))




**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

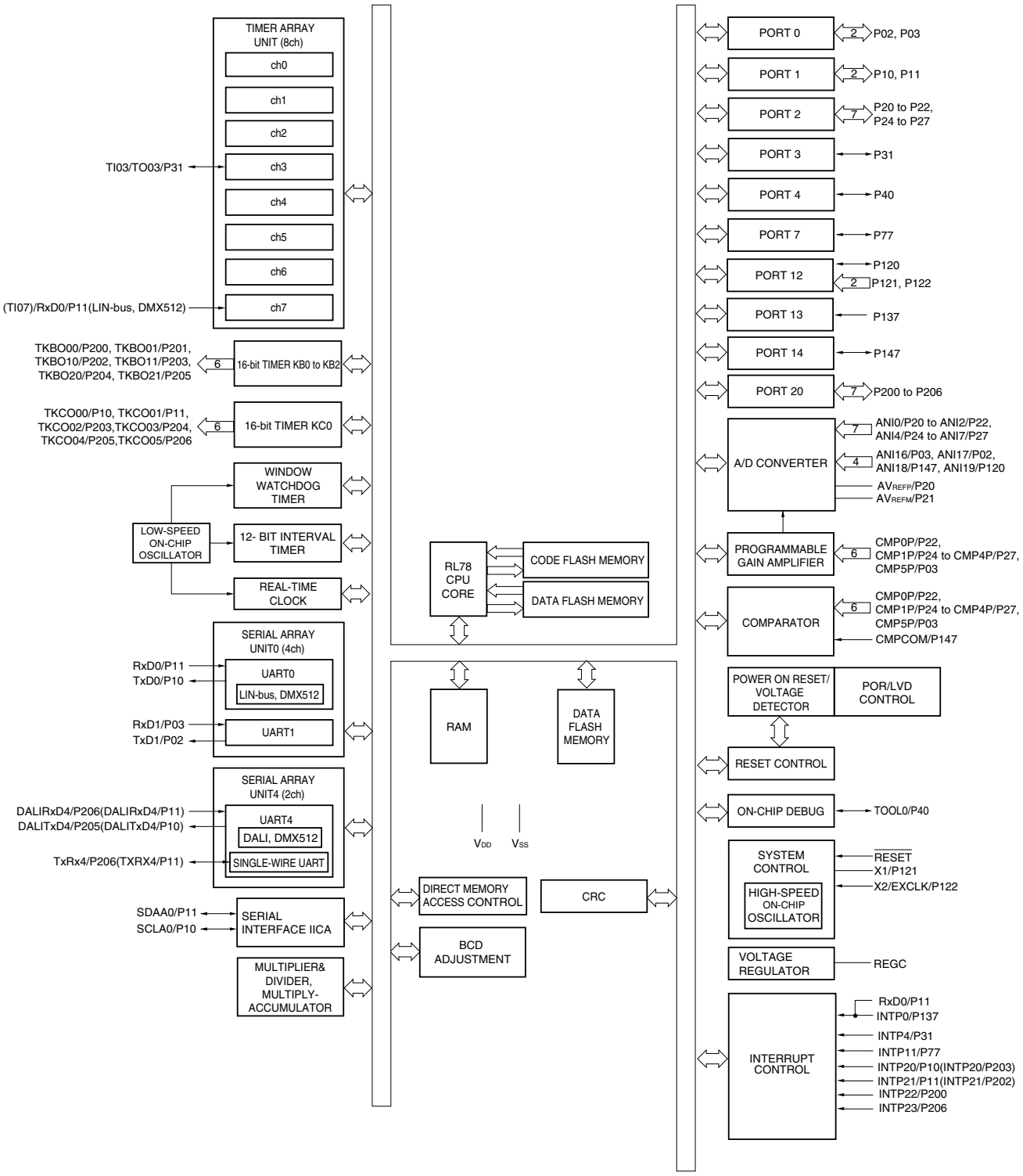
**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1)** and **Figure 15-20 Format of Input Switch Control Register (ISC) in the RL78/I1A User's Manual**.

## 1.4 Pin Identification

| | |
|---|---|
| ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19: | Analog Input |
| $AV_{REFM}$: | Analog Reference Voltage Minus |
| $AV_{REFP}$: | Analog Reference Voltage Plus |
| CMP0P to CMP5P: | Comparator Analog Input |
| CMPCOM: | Comparator External Reference Voltage |
| EXCLK: | External Clock Input (Main System Clock) |
| EXCLKS: | External Clock Input (Subsystem Clock) |
| INTP0, INTP3, INTP4, INTP9, INTP10, INTP11, INTP20 to INTP23: | Interrupt Request from Peripheral |
| P02, P03, P05, P06: | Port 0 |
| P10 to P12: | Port 1 |
| P20 to P22, P24 to P27: | Port 2 |
| P30, P31: | Port 3 |
| P40: | Port 4 |
| P75 to P77: | Port 7 |
| P120 to P124: | Port 12 |
| P137: | Port 13 |
| P147: | Port 14 |
| P200 to P206: | Port 20 |
| REGC: | Regulator Capacitance |
| RESET: | Reset |
| RTC1HZ: | Real-time Clock Correction Clock (1 Hz) Output |
| RxD0, RxD1, DALIRxD4: | Receive Data |
| SCK00: | Serial Clock Input/Output |
| SCLA0: | Serial Clock Input/Output |
| SDAA0: | Serial Data Input/Output |
| SI00: | Serial Data Input |
| SO00: | Serial Data Output |
| TI03, TI05, TI06, TI07: | Timer Input |
| TO03, TO05, TO06, TKBO00, TKBO01 to TKBO20, TKBO21, TKCO00 to TKCO05: | Timer Output |
| TOOL0: | Data Input/Output for Tool |
| TxRx4: | Serial Data Input/Output for Single Wired UART |
| TxD0, TxD1 DALITxD4: | Transmit Data |
| $V_{DD}$: | Power Supply |
| $V_{SS}$: | Ground |
| X1, X2: | Crystal Oscillator (Main System Clock) |
| XT1, XT2: | Crystal Oscillator (Subsystem Clock) |

### 1.5.2 30-pin products




**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1)** and **Figure 15-20 Format of Input Switch Control Register (ISC) in the RL78/I1A User's Manual**.

(2/3)

| Item | | | 20-pin | 30-pin | 38-pin |
|---|---|---|---|---|---|
| | | | R5F1076C | R5F107AC, R5F107AE | R5F107DE |
| Timer | Watchdog timer | | 1 channel | | |
| | Real-time clock (RTC) | | 1 channel[Notes 1, 2] | | |
| | 12-bit interval timer (IT) | | 1 channel | | |
| | RTC output | | – | | 1<br>1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) |
| 8/10-bit resolution A/D converter | | | 6 channels | 11 channels | 11 channels |
| Comparator | | | 4 channels | 6 channels | 6 channels |
| Programmable gain amplifier | | | 1 channel | | |
| | | Input[Note 3] | 4 channels | 6 channels | 6 channels |
| Serial interface | | | [20-pin] [Note 5]<br>• UART (Supporting LIN-bus and DMX512): 1 channel<br>• UART (Supporting DALI communication): 1 channel<br>[30-pin products]<br>• UART (Supporting LIN-bus and DMX512): 1 channel<br>• UART: 1 channel<br>• UART (Supporting DALI communication): 1 channel<br>[38-pin products]<br>• CSI: 1 channel/UART (Supporting LIN-bus and DMX512): 1 channel<br>• UART: 1 channel<br>• UART (Supporting DALI communication): 1 channel | | |
| | $I^2C$ bus | | 1 channel | 1 channel | 1 channel |
| Multiplier and divider/multiply-accumulator | | | • 16 bits × 16 bits = 32 bits (Unsigned or signed)<br>• 32 bits ÷ 32 bits = 32 bits (Unsigned)<br>• 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) | | |
| DMA controller | | | 2 channels | | |
| Vectored interrupt sources | Internal | | 27 | 30 | 30 |
| | External | | 7 | 10 | 11 |
| Reset | | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution[Note 4]<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | |

**Notes 1.** The subsystem clock ($f_{SUB}$) can be selected as the operating clock only for 38-pin products.

**2.** The 20- and 30-pin products can only be used as the constant-period interrupt function.

**3.** The comparator input is alternatively used with analog input pin (ANI pin).

**4.** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

**5.** The 20 pin products can only be used 1 UART simultaneously due to sharing of the same I/O pins.

# 2. ELECTRICAL SPECIFICATIONS (G: Industrial applications, $T_A$ = –40 to +105°C)

In this chapter, shows the electrical spesificatons of the target products.

Target products (G: Industrial applications): $T_A$ = – 40 to + 105°C
R5F107xxGxx

**Cautions 1. The RL78/I1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 Functions for each product in the RL78/I1A User's Manual.**

**Absolute Maximum Ratings ($T_A$ = 25°C) (2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | −40 | mA |
| | | Total of all pins −170 mA | P02, P03, P40, P120 | −70 | mA |
| | | | P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 | −100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P22, P24 to P27 | −0.5 | mA |
| | | Total of all pins | | −2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | 40 | mA |
| | | Total of all pins 170 mA | P02, P03, P40, P120 | 70 | mA |
| | | | P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P22, P24 to P27 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | −40 to +105 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | −65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +105°C[Note 6], 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time [Note 5] | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | | | $t_{KCY2}$/2 | | $t_{KCY2}$/2 | | ns |
| SIp setup time (to SCKp↑)[Note 1] | $t_{SIK2}$ | | | 1/$f_{MCK}$+20 | | 1/$f_{MCK}$+30 | | ns |
| SIp hold time (from SCKp↑)[Note 2] | $t_{KSI2}$ | | | 1/$f_{MCK}$+31 | | 1/$f_{MCK}$+31 | | ns |
| Delay time from SCKp↓ to SOp output[Note 3] | $t_{KSO2}$ | C = 30 pF[Note 4] | | | 2/$f_{MCK}$+ 44 | | 2/$f_{MCK}$+ 110 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SOp output lines.

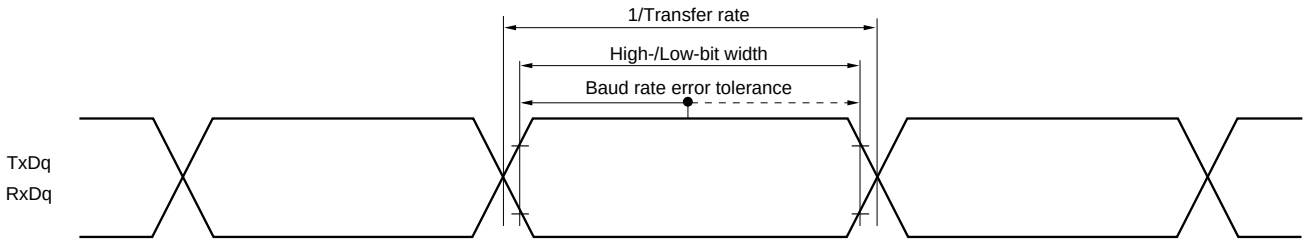
**5.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**6.** Operating conditions of LS (low-speed main) mode is $T_A$ = –40 to +85 °C.

**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remarks 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))



**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +105°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (–) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution | | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| Zero-scale error[Notes 1, 2] | $E_{ZS}$ | 10-bit resolution | | | | ±0.60 | %FSR |
| Full-scale error[Notes 1, 2] | $E_{FS}$ | 10-bit resolution | | | | ±0.60 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution | | | | ±4.0 | LSB |
| Differential linearity error[Note 1] | DLE | 10-bit resolution | | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI2, ANI4 to ANI7 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI19 | | 0 | | $V_{DD}$ | V |
| | | Internal reference voltage (HS (high-speed main) mode) | | $V_{BGR}$[Note 3] | | | V |
| | | Temperature sensor output voltage (HS (high-speed main) mode) | | $V_{TMPS25}$[Note 3] | | | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** See **2.6.2 Temperature sensor/internal reference voltage characteristics**.

## 2.6.6 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode**

**($T_A$ = –40 to +105°C, $V_{PDR} \le V_{DD} \le$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | Supply voltage level | $V_{LVD0}$ | Power supply rise time | 3.97 | 4.06 | 4.14 | V |
| | | | Power supply fall time | 3.89 | 3.98 | 4.06 | V |
| | | $V_{LVD1}$ | Power supply rise time | 3.67 | 3.75 | 3.82 | V |
| | | | Power supply fall time | 3.59 | 3.67 | 3.74 | V |
| | | $V_{LVD2}$ | Power supply rise time | 3.06 | 3.13 | 3.19 | V |
| | | | Power supply fall time | 2.99 | 3.06 | 3.12 | V |
| | | $V_{LVD3}$ | Power supply rise time | 2.95 | 3.02 | 3.08 | V |
| | | | Power supply fall time | 2.89 | 2.96 | 3.02 | V |
| | | $V_{LVD4}$ | Power supply rise time | 2.85 | 2.92 | 2.97 | V |
| | | | Power supply fall time | 2.79 | 2.86 | 2.91 | V |
| | | $V_{LVD5}$ | Power supply rise time | 2.75 | 2.81 | 2.87 | V |
| | | | Power supply fall time | 2.70 | 2.75 | 2.81 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | μs |
| Detection delay time | | | | | | 300 | μs |

**LVD Detection Voltage of Interrupt & Reset Mode**

**($T_A$ = –40 to +105°C, $V_{PDR} \le V_{DD} \le$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage: 2.7 V | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVD1}$ | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.85 | 2.92 | 2.97 | V |
| | | | Falling interrupt voltage | 2.79 | 2.86 | 2.91 | V |
| | $V_{LVD2}$ | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.95 | 3.02 | 3.08 | V |
| | | | Falling interrupt voltage | 2.89 | 2.96 | 3.02 | V |
| | $V_{LVD3}$ | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.97 | 4.06 | 4.14 | V |
| | | | Falling interrupt voltage | 3.89 | 3.98 | 4.06 | V |

## 2.6.7 Supply voltage rise inclination characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage rise | $SV_{DD}$ | | | | 54 | V/ms |

**Caution Keep the internal reset status by using the LVD circuit or an external reset signal until $V_{DD}$ rises to within the operating voltage range shown in 32.4 AC Characteristics.**

## 2.8 Flash Memory Programming Characteristics

**($T_A$ = –40 to +105°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CPU/peripheral hardware clock frequency | $f_{CLK}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | 32 | MHz |
| Number of code flash rewrites Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years, $T_A$ = 85°C Note 3 | 1,000 | | | Times |
| Number of data flash rewrites Notes 1, 2, 3 | | Retained for 1 year, $T_A$ = 25°C Note 3 | | 1,000,000 | | |
| | | Retained for 5 years, $T_A$ = 85°C Note 3 | 100,000 | | | |
| | | Retained for 20 years, $T_A$ = 85°C Note 3 | 10,000 | | | |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library

**3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

**($T_A$ = –40 to +105°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115.2 k | | 1 M | bps |

## 3.3 DC Characteristics

### 3.3.1 Pin characteristics

**($T_A$ = –40 to +125°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high[Note 1] | $I_{OH1}$ | Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | –3.0[Note 2] | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | –1.0 | mA |
| | | Total of P02, P03, P40, P120 (When duty ≤ 70%[Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | –9.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | –3.0 | mA |
| | | Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty ≤ 70%[Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | –21.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | –6.0 | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | –21.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | –9.0 | mA |
| | $I_{OH2}$ | Per pin for P20 to P22, P24 to P27 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | –0.1[Note 2] | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | –0.4 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ pin to an output pin.

**2.** However, do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Caution P02, P10 to P12 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +125°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –3.0 mA | $V_{DD}$ – 0.7 | | | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –1.0 mA | $V_{DD}$ – 0.5 | | | V |
| | $V_{OH2}$ | P20 to P22, P24 to P27 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH2}$ = –100 μA | $V_{DD}$ – 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 4.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P22, P24 to P27 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL2}$ = 400 μA | | | 0.4 | V |

**Caution P02, P10 to P12 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 20 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**($T_A$ = –40 to +125°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.50 | 2.0 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.50 | 2.0 | mA |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.40 | 2.2 | mA |
| | | | | | Resonator connection | | 0.50 | 2.3 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.40 | 2.2 | mA |
| | | | | | Resonator connection | | 0.50 | 2.3 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.24 | 1.22 | mA |
| | | | | | Resonator connection | | 0.30 | 1.28 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.24 | 1.22 | mA |
| | | | | | Resonator connection | | 0.30 | 1.28 | mA |
| | | | HS (high-speed main) mode Note 7 | $f_{IH}$ = 4 MHz Note 4 $f_{PLL}$ = 64 MHz, $f_{CLK}$ = 16 MHz | $V_{DD}$ = 5.0 V | | 0.95 | 3.7 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.95 | 3.7 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = –40°C | Square wave input | | 0.28 | 0.70 | μA |
| | | | | | Resonator connection | | 0.47 | 0.89 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +25°C | Square wave input | | 0.33 | 0.70 | μA |
| | | | | | Resonator connection | | 0.52 | 0.89 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +50°C | Square wave input | | 0.41 | 1.90 | μA |
| | | | | | Resonator connection | | 0.60 | 2.09 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +70°C | Square wave input | | 0.54 | 2.80 | μA |
| | | | | | Resonator connection | | 0.73 | 2.99 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +85°C | Square wave input | | 1.27 | 6.10 | μA |
| | | | | | Resonator connection | | 1.46 | 6.29 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +105°C | Square wave input | | 3.04 | 15.5 | μA |
| | | | | | Resonator connection | | 3.23 | 15.7 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5 $T_A$ = +125°C | Square wave input | | 7.20 | 45.2 | μA |
| | | | | | Resonator connection | | 7.53 | 45.5 | μA |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = –40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | μA |
| | | | $T_A$ = +50°C | | | | 0.27 | 1.70 | μA |
| | | | $T_A$ = +70°C | | | | 0.44 | 2.60 | μA |
| | | | $T_A$ = +85°C | | | | 1.17 | 5.90 | μA |
| | | | $T_A$ = +105°C | | | | 2.94 | 15.3 | μA |
| | | | $T_A$ = +125°C | | | | 7.14 | 45.1 | μA |

(**Notes** and **Remarks** are listed on the next page.)

## 3.5.2 Serial interface IICA

### (1) $I^2C$ standard mode

**($T_A$ = –40 to +125°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Standard mode: $f_{CLK}$ ≥ 1 MHz | 0 | 100 | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | | 4.7 | | μs |
| Hold time[Note 1] | $t_{HD:STA}$ | | 4.0 | | μs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | | 4.7 | | μs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | | 4.0 | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | | 250 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | | 0 | 3.45 | μs |
| Setup time of stop condition | $t_{SU:STO}$ | | 4.0 | | μs |
| Bus-free time | $t_{BUF}$ | | 4.7 | | μs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ

### (2) $I^2C$ fast mode

**($T_A$ = –40 to +125°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | fast mode: $f_{CLK}$ ≥ 3.5 MHz | 0 | 400 | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | | 0.6 | | μs |
| Hold time[Note 1] | $t_{HD:STA}$ | | 0.6 | | μs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | | 1.3 | | μs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | | 0.6 | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | | 100 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | | 0 | 0.9 | μs |
| Setup time of stop condition | $t_{SU:STO}$ | | 0.6 | | μs |
| Bus-free time | $t_{BUF}$ | | 1.3 | | μs |

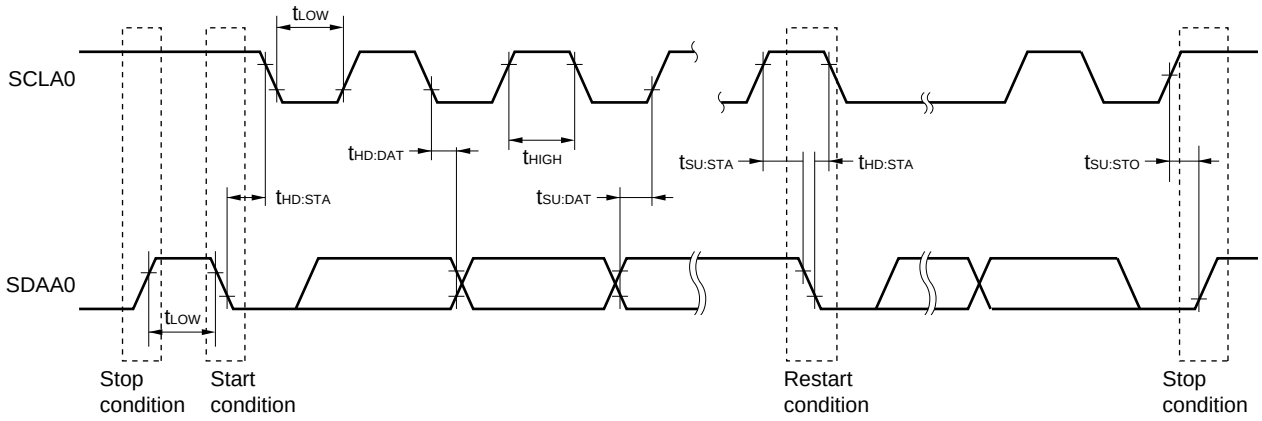
**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**



## 3.6 Analog Characteristics

### 3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
|---|---|---|---|
| | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (–) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$<br>Reference voltage (–) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$<br>Reference voltage (–) = $AV_{REFM}$ |
| ANI0 to ANI2, ANI4 to ANI7 | See **3.6.1 (1)**. | See **3.6.1 (3)**. | See **3.6.1 (4)**. |
| ANI16 to ANI19 | See **3.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | See **3.6.1 (1)**. | | – |

## 3.6.3 Programmable gain amplifier

**($T_A$ = –40 to +125°C, 2.7 V ≤ $AV_{REFP}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IOPGA}$ | | | | | ±5 | ±10 | mV |
| Input voltage range | $V_{IPGA}$ | | | | 0 | | 0.9$V_{DD}$/gain | V |
| Gain error[Note 1] | | 4, 8 times | | | | | ±1 | % |
| | | 16 times | | | | | ±1.5 | % |
| | | 32 times | | | | | ±2 | % |
| Slew rate[Note 1] | $SR_{RPGA}$ | Rising edge | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 4, 8 times | 4 | | | V/μs |
| | | | | 16, 32 times | 1.4 | | | V/μs |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | 4, 8 times | 1.8 | | | V/μs |
| | | | | 16, 32 times | 0.5 | | | V/μs |
| | $SR_{FPGA}$ | Falling edge | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 4, 8 times | 3.2 | | | V/μs |
| | | | | 16, 32 times | 1.4 | | | V/μs |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | 4, 8 times | 1.2 | | | V/μs |
| | | | | 16, 32 times | 0.5 | | | V/μs |
| Operation stabilization wait time[Note 2] | $t_{PGA}$ | 4, 8 times | | | 5 | | | μs |
| | | 16, 32 times | | | 10 | | | μs |

**Notes 1.** When $V_{IPGA}$ = 0.1$V_{DD}$/gain to 0.9$V_{DD}$/gain.

**2.** Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

**Remark** These characteristics apply when $AV_{REFM}$ is selected as GND of the PGA by using the CVRVS1 bit.

## 3.8 Flash Memory Programming Characteristics

**($T_A$ = –40 to +105°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CPU/peripheral hardware clock frequency | $f_{CLK}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | 32 | MHz |
| Number of code flash rewrites Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years, $T_A$ = 85°C Note 3, 4 | 1,000 | | | Times |
| Number of data flash rewrites Notes 1, 2, 3 | | Retained for 1 year, $T_A$ = 25°C Note 3, 4 | | 1,000,000 | | |
| | | Retained for 5 years, $T_A$ = 85°C Note 3, 4 | 100,000 | | | |
| | | Retained for 20 years, $T_A$ = 85°C Note 3, 4 | 10,000 | | | |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library

**3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4. These are the average temperature of during the retainment.

## 3.9 Dedicated Flash Memory Programmer Communication (UART)

**$T_A$ = –40 to +105°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115.2 k | | 1 M | bps |