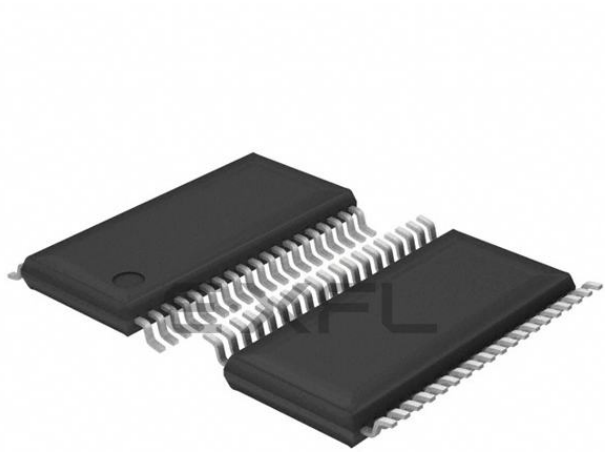


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

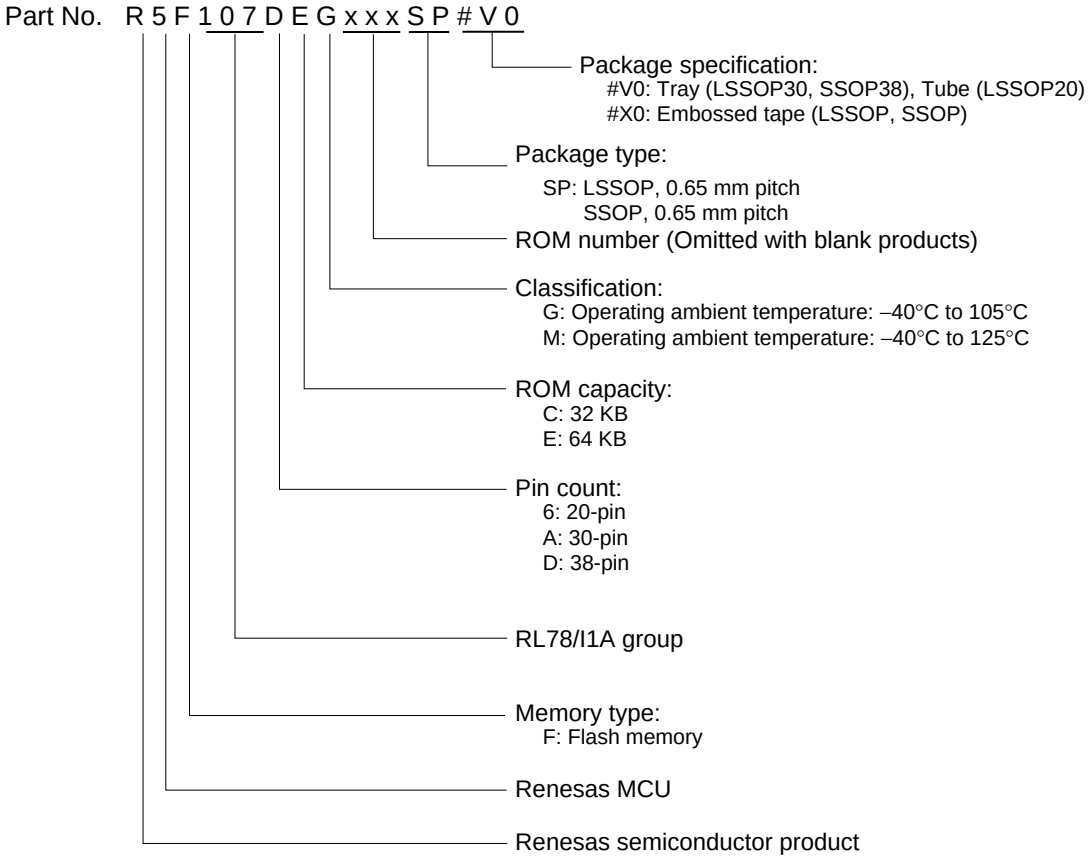
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	38-SSOP (0.240", 6.10mm Width)
Supplier Device Package	38-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f107degsp-x0

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/I1A



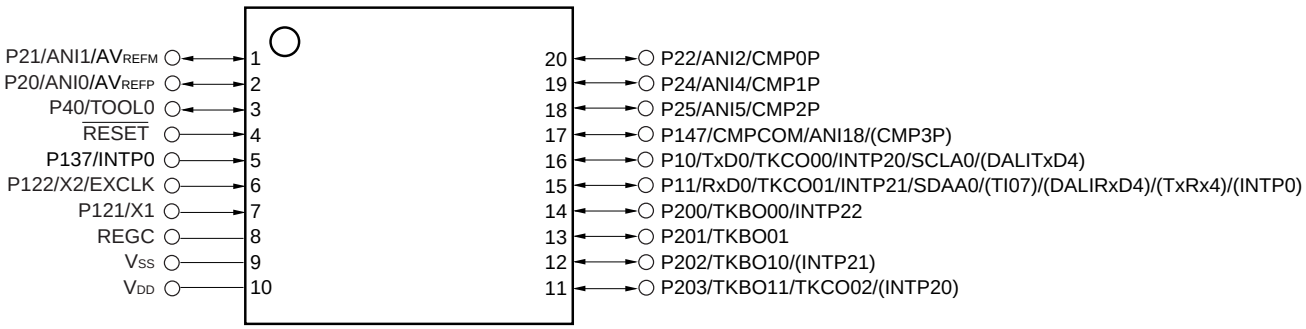
Pin count	Package	Operating Ambient Temperature	Part Number
20 pin	20-pin plastic LSSOP (4.4 × 6.5)	T_A = –40 to +105°C	R5F1076CGSP#V0, R5F1076CGSP#X0
		T_A = –40 to +125°C	R5F1076CMSP#V0, R5F1076CMSP#X0
30 pin	30-pin plastic LSSOP (7.62 mm (300))	T_A = –40 to +105°C	R5F107ACGSP#V0, R5F107AEGSP#V0, R5F107ACGSP#X0, R5F107AEGSP#X0
		T_A = –40 to +125°C	R5F107ACMSP#V0, R5F107AEMSP#V0, R5F107ACMSP#X0, R5F107AEMSP#X0
38 pin	38-pin plastic SSOP (7.62 mm (300))	T_A = –40 to +105°C	R5F107DEGSP#V0, R5F107DEGSP#X0
		T_A = –40 to +125°C	R5F107DEMSP#V0, R5F107DEMSP#X0

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 20-pin products

- 20-pin plastic LSSOP (4.4 x 6.5)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

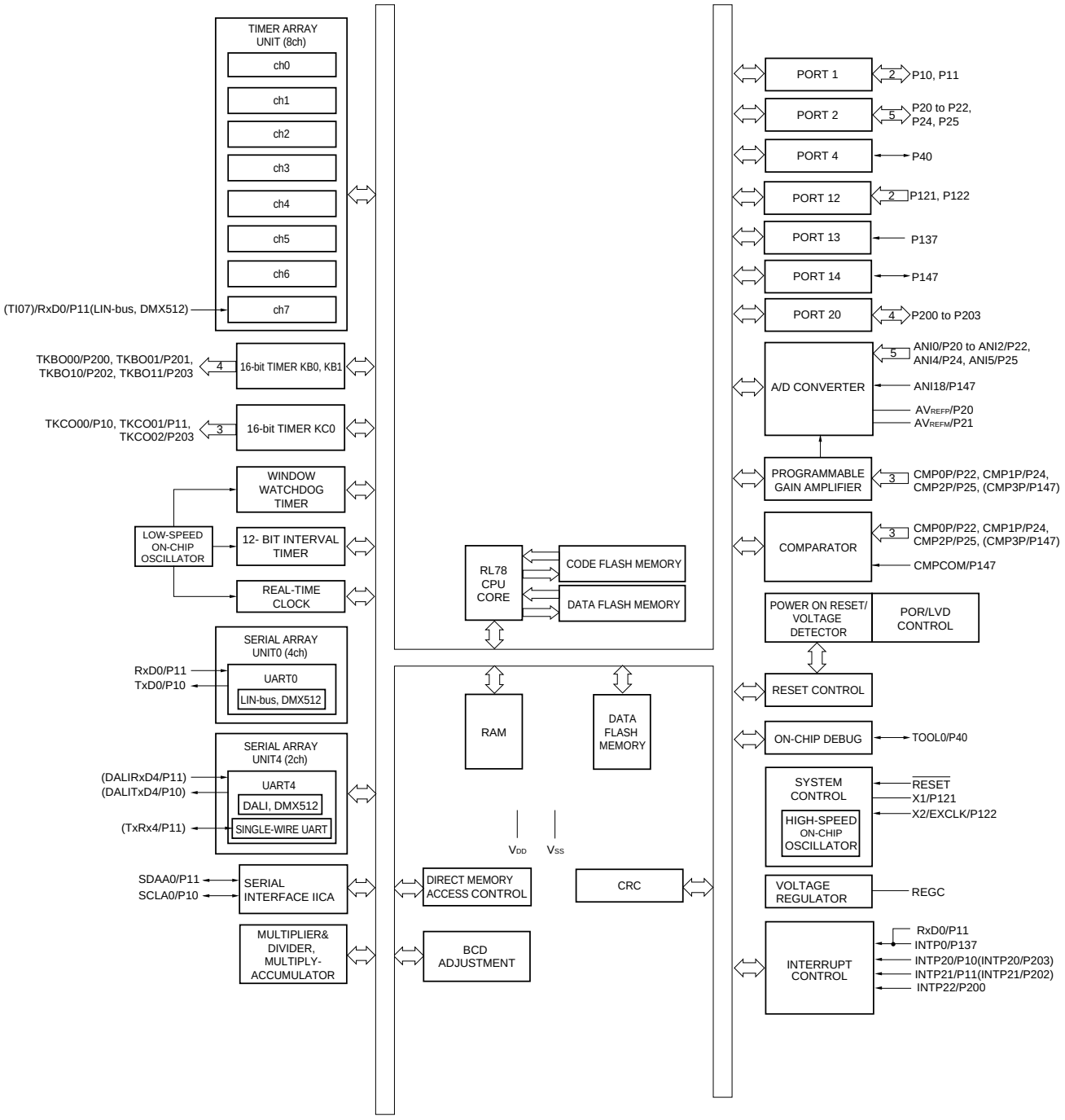
Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1)** and **Figure 15-20 Format of Input Switch Control Register (ISC) in the RL78/I1A User's Manual**.

3. The shared function CMP3P can be assigned to P147 by setting the CMPSEL0 bit in the comparator input switch control register (CMPSEL).

1.5 Block Diagram

1.5.1 20-pin products



Remarks 1. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1)** and **Figure 15-20 Format of Input Switch Control Register (ISC) in the RL78/I1A User's Manual**.

2. The shared function CMP3P can be assigned to P147 by setting the CMPSEL0 bit in the comparator input switch control register (CMPSEL).

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz

LS (low-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVD} Notes 1, 7				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 8				2.50	12.2	mA
Programmable gain amplifier operating current	I_{PGA} Note 9		AV_{REFP} = V_{DD} = 5.0 V		0.21	0.31	mA
			AV_{REFP} = V_{DD} = 3.0 V		0.18	0.29	mA
Comparator operating current	I_{CMP} Note 10	When one comparator channel is operating	AV_{REFP} = V_{DD} = 5.0 V		41.4	62	μA
			AV_{REFP} = V_{DD} = 3.0 V		37.2	59	μA
	I_{VREF}	When one internal reference voltage circuit is operating	AV_{REFP} = V_{DD} = 5.0 V		14.8	26	μA
			AV_{REFP} = V_{DD} = 3.0 V		8.9	20	μA
Programmable gain amplifier/ comparator reference current source	I_{IREF} Note 11		AV_{REFP} = V_{DD} = 5.0 V		3.2	5.1	μA
			AV_{REFP} = V_{DD} = 3.0 V		2.9	4.9	μA
BGO operating current	I_{BGO} Note 12				2.50	12.2	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 13		0.50	1.1	mA
			The A/D conversion operations are performed, Standard mode, AV_{REFP} = V_{DD} = 5.0 V		2.0	3.04	mA
		CSI/UART operation			0.70	1.54	mA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Current flowing to the V_{DD}.

2. When the high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the XT1 oscillator and f_{IL} operating current). The current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

8. Current flowing during self-programming operation.

9. Current flowing only to the programmable gain amplifier. The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{PGA}, when the programmable gain amplifier is operating in operating mode or in HALT mode.

10. Current flowing only to the comparator. The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{CMP}, when the comparator is operating.

11. This is the current required to flow to V_{DD} pin of the current circuit that is used as the programmable gain amplifier and the comparator.

12. Current flowing only during data flash rewrite.

13. See **21.3.3 SNOOZE mode in the RL78/I1A User's Manual** for shift time to the SNOOZE mode .

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

5. Example of calculating current value when using programmable gain amplifier and comparator.

Examples 1) TYP. operating current value when three comparator channels, one internal reference voltage generator, and PGA are operating (when AV_{REFP} = V_{DD} = 5.0 V)

I_{CMP} × 3 + I_{VREF} + I_{PGA} + I_{IREF}

= 41.4 [μA] × 3 + 14.8 [μA] × 1 + 210 [μA] + 3.2 [μA]

= 352.2 [μA]

Examples 2) TYP. operating current value when using two comparator channels, without using internal reference voltage generator (when AV_{REFP} = V_{DD} = 5.0 V)

I_{CMP} × 2 + I_{IREF}

= 41.4 [μA] × 2 + 3.2 [μA]

= 86.0 [μA]

2.4 AC Characteristics

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode		0.03125		1	μs
			LS (low-speed main) mode	T_A = –40 to +85°C	0.125		1	μs
		Subsystem clock (f_{SUB}) operation			28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode		0.03125		1	μs
			LS (low-speed main) mode	T_A = –40 to +85°C	0.125		1	μs
External system clock frequency	f_{EX}				1.0		20.0	MHz
	f_{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}				24			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI03, TI05, TI06, TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				2/f_{MCK}+10			ns
TO03, TO05, TO06, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TKCO00 to TKCO05 output frequency (When duty = 50%)	f_{TO}	HS (high-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			8	MHz
				2.7 V ≤ V_{DD} < 4.0 V			4	MHz
		LS (low-speed main) mode, T_A = –40 to +85°C		4.0 V ≤ V_{DD} ≤ 5.5 V			4	MHz
				2.7 V ≤ V_{DD} < 4.0 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP3, INTP4, INTP9 to INTP11, INTP20 to INTP23			1			μs
$\overline{RESET}$ low-level width	t_{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

2.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +105°C [Note 3], 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	0	100	0	100	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		4.7		μs
Hold time[Note 1]	$t_{HD:STA}$		4.0		4.0		μs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		4.7		μs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		4.0		μs
Data setup time (reception)	$t_{SU:DAT}$		250		250		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	3.45	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		4.0		μs
Bus-free time	t_{BUF}		4.7		4.7		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

3. Operating conditions of LS (low-speed main) mode is T_A = –40 to +85 °C.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

2.6.3 Programmable gain amplifier

(T_A = –40 to +105°C, 2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOPGA}					±5	±10	mV
Input voltage range	V_{IPGA}				0		0.9V_{DD}/gain	V
Gain error[Note 1]		4, 8 times					±1	%
		16 times					±1.5	%
		32 times					±2	%
Slew rate[Note 1]	SR_{RPGA}	Rising edge	4.0 V ≤ V_{DD} ≤ 5.5 V	4, 8 times	4			V/μs
				16, 32 times	1.4			V/μs
			2.7 V ≤ V_{DD} < 4.0 V	4, 8 times	1.8			V/μs
				16, 32 times	0.5			V/μs
	SR_{FPGA}	Falling edge	4.0 V ≤ V_{DD} ≤ 5.5 V	4, 8 times	3.2			V/μs
				16, 32 times	1.4			V/μs
			2.7 V ≤ V_{DD} < 4.0 V	4, 8 times	1.2			V/μs
				16, 32 times	0.5			V/μs
Operation stabilization wait time[Note 2]	t_{PGA}	4, 8 times			5			μs
		16, 32 times			10			μs

Notes 1. When V_{IPGA} = 0.1V_{DD}/gain to 0.9V_{DD}/gain.

2. Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

Remark These characteristics apply when AV_{REFM} is selected as GND of the PGA by using the CVRVS1 bit.

2.8 Flash Memory Programming Characteristics

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	2.7 V ≤ V_{DD} ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years, T_A = 85°C Note 3	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year, T_A = 25°C Note 3		1,000,000		
		Retained for 5 years, T_A = 85°C Note 3	100,000			
		Retained for 20 years, T_A = 85°C Note 3	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

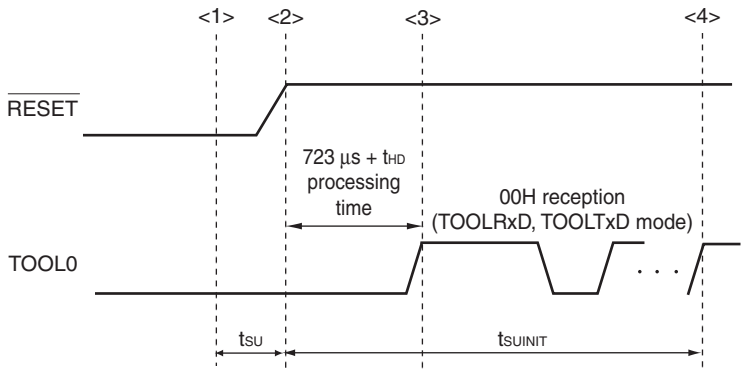
(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115.2 k		1 M	bps

2.10 Timing of Entry to Flash Memory Programming Modes

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the pin reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Complete the baud rate setting by UART reception.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends

t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	4.0 V ≤ V_{DD} ≤ 5.5 V			–3.0[Note 2]	mA
			2.7 V ≤ V_{DD} < 4.0 V			–1.0	mA
		Total of P02, P03, P40, P120 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			–9.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–3.0	mA
		Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			–21.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–6.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			–21.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–9.0	mA
	I_{OH2}	Per pin for P20 to P22, P24 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V			–0.1[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.7 V ≤ V_{DD} ≤ 5.5 V			–0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P02, P10 to P12 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, $\overline{\text{RESET}}$	Normal input buffer	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P03, P10, P11	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.1		V_{DD}	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 2.7 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
Input voltage, low	V_{IL1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, $\overline{\text{RESET}}$	Normal input buffer	0		0.2V_{DD}	V
	V_{IL2}	P03, P10, P11	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 2.7 V ≤ V_{DD} < 3.3 V	0		0.32	V

Caution The maximum value of V_{IH} of pins P02, P10 to P12 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.50	2.0	mA
					V_{DD} = 3.0 V		0.50	2.0	mA
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.40	2.2	mA
					Resonator connection		0.50	2.3	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.40	2.2	mA
					Resonator connection		0.50	2.3	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.24	1.22	mA
					Resonator connection		0.30	1.28	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.24	1.22	mA
					Resonator connection		0.30	1.28	mA
			HS (high-speed main) mode Note 7	f_{IH} = 4 MHz Note 4 f_{PLL} = 64 MHz, f_{CLK} = 16 MHz	V_{DD} = 5.0 V		0.95	3.7	mA
					V_{DD} = 3.0 V		0.95	3.7	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = –40°C	Square wave input		0.28	0.70	μA
					Resonator connection		0.47	0.89	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.33	0.70	μA
					Resonator connection		0.52	0.89	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.41	1.90	μA
					Resonator connection		0.60	2.09	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.54	2.80	μA
					Resonator connection		0.73	2.99	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		1.27	6.10	μA
					Resonator connection		1.46	6.29	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +105°C	Square wave input		3.04	15.5	μA
					Resonator connection		3.23	15.7	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +125°C	Square wave input		7.20	45.2	μA
					Resonator connection		7.53	45.5	μA
	I_{DD3} Note 6	STOP mode Note 8	T_A = –40°C				0.18	0.50	μA
			T_A = +25°C				0.23	0.50	μA
			T_A = +50°C				0.27	1.70	μA
			T_A = +70°C				0.44	2.60	μA
			T_A = +85°C				1.17	5.90	μA
			T_A = +105°C				2.94	15.3	μA
			T_A = +125°C				7.14	45.1	μA

(**Notes** and **Remarks** are listed on the next page.)

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V	250		ns
			2.7 V ≤ V_{DD} ≤ 5.5 V	500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 20$		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 40$		ns
SIp setup time (to SCKp↑)Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		80		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		80		ns
SIp hold time (from SCKp↑)Note 2	t_{KSI1}			40		ns
Delay time from SCKp↓ to SOp outputNote 3	t_{KSO1}	C = 30 pFNote 4			80	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

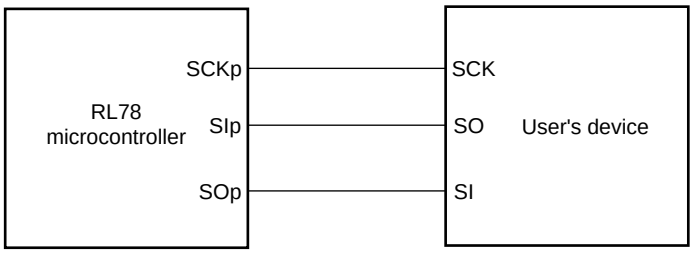
Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

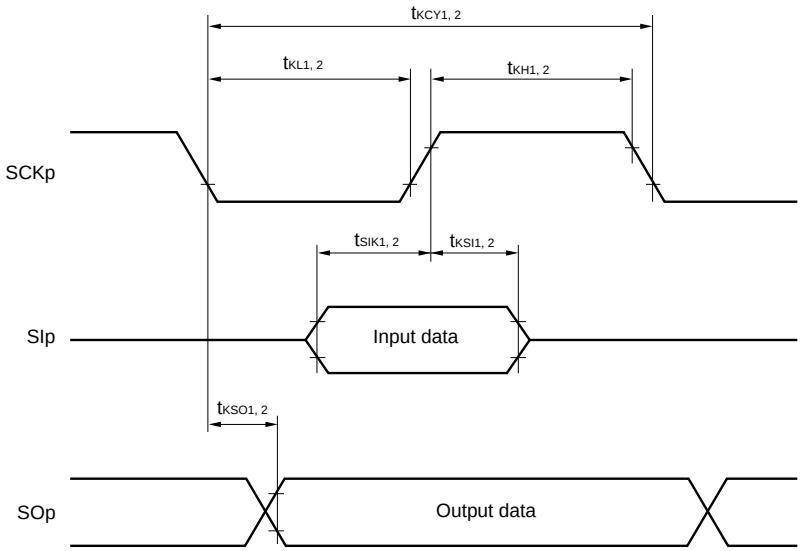
2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

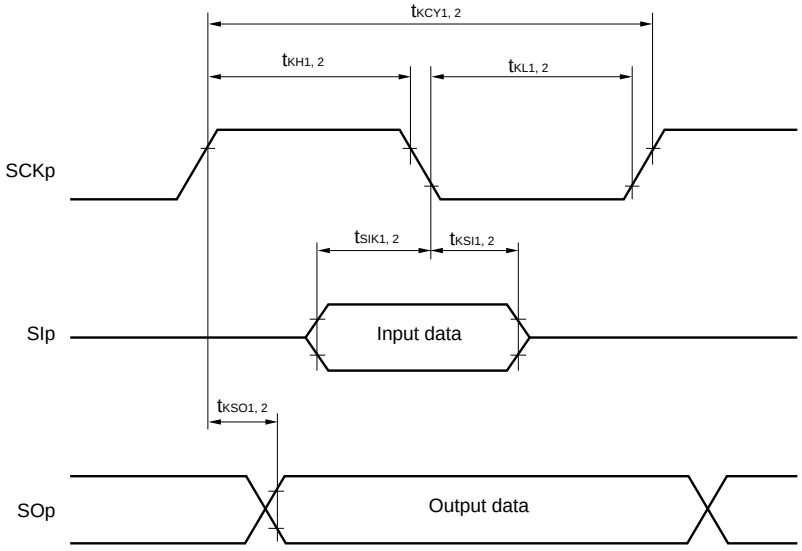
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00)

2. m: Unit number, n: Channel number (mn = 00)

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI2, ANI4 to ANI7, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +125°C, 2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} Note 3			1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2, ANI4 to ANI7	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.8		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD} Note 3				±0.25	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution AV_{REFP} = V_{DD} Note 3				±0.25	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV_{REFP} = V_{DD} Note 3				±2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV_{REFP} = V_{DD} Note 3				±1.5	LSB
Analog input voltage	V_{AIN}	ANI2, ANI4 to ANI7		0		AV_{REFP}	V
		Internal reference voltage (HS (high-speed main) mode)		V_{BGR} Note 4			V
		Temperature sensor output voltage (HS (high-speed main) mode)		V_{TMPS25} Note 4			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

4. See **3.6.2 Temperature sensor/internal reference voltage characteristics**.

3.6.3 Programmable gain amplifier

(T_A = –40 to +125°C, 2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOPGA}					±5	±10	mV
Input voltage range	V_{IPGA}				0		0.9V_{DD}/gain	V
Gain error[Note 1]		4, 8 times					±1	%
		16 times					±1.5	%
		32 times					±2	%
Slew rate[Note 1]	SR_{RPGA}	Rising edge	4.0 V ≤ V_{DD} ≤ 5.5 V	4, 8 times	4			V/μs
				16, 32 times	1.4			V/μs
			2.7 V ≤ V_{DD} < 4.0 V	4, 8 times	1.8			V/μs
				16, 32 times	0.5			V/μs
	SR_{FPGA}	Falling edge	4.0 V ≤ V_{DD} ≤ 5.5 V	4, 8 times	3.2			V/μs
				16, 32 times	1.4			V/μs
			2.7 V ≤ V_{DD} < 4.0 V	4, 8 times	1.2			V/μs
				16, 32 times	0.5			V/μs
Operation stabilization wait time[Note 2]	t_{PGA}	4, 8 times			5			μs
		16, 32 times			10			μs

Notes 1. When V_{IPGA} = 0.1V_{DD}/gain to 0.9V_{DD}/gain.

2. Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

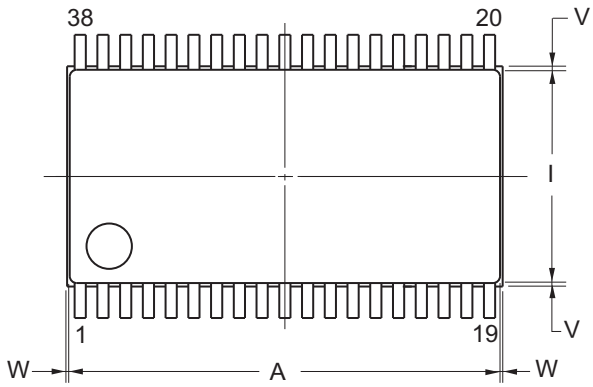
Remark These characteristics apply when AV_{REFM} is selected as GND of the PGA by using the CVRVS1 bit.

4. PACKAGE DRAWINGS

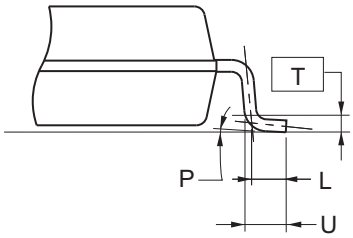
4.1 20-pin Products

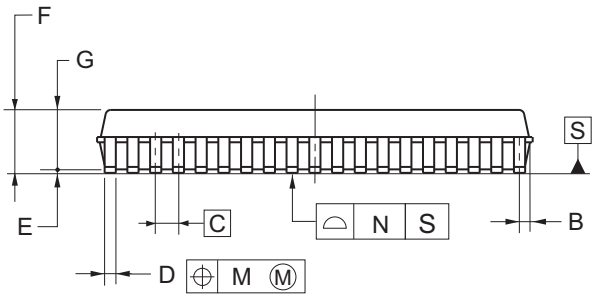
R5F1076CGSP#V0, R5F1076CGSP#X0, R5F1076CMSP#V0, R5F1076CMSP#X0

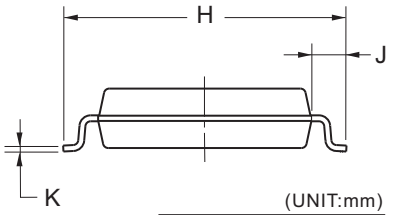
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-SSOP38-0300-0.65	PRSP0038JA-A	P38MC-65-2A4-2	0.3



detail of lead end







(UNIT:mm)

ITEM	DIMENSIONS
A	12.30±0.10
B	0.30
C	0.65 (T.P.)
D	$0.32^{+0.08}_{-0.07}$
E	0.125±0.075
F	2.00 MAX.
G	1.70±0.10
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.17^{+0.08}_{-0.07}$
L	0.50
M	0.10
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

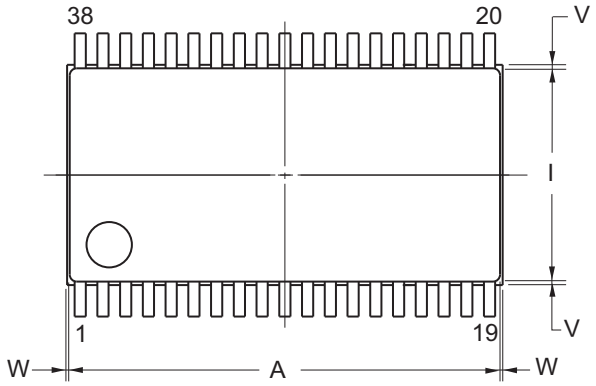
NOTE

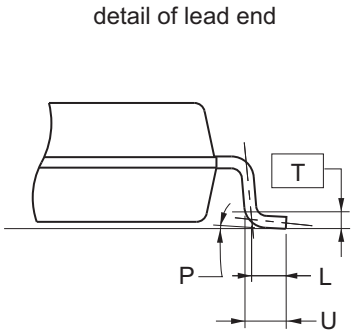
Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

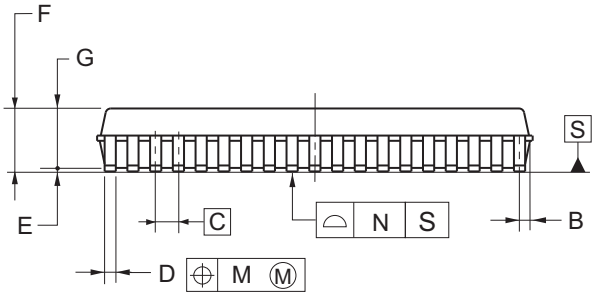
4.3 38-pin Products

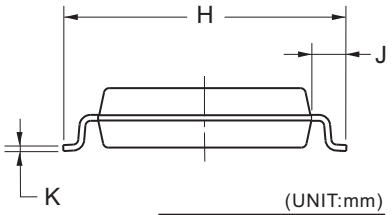
R5F107DEGSP#V0, R5F107DEGSP#X0, R5F107DEMSP#V0, R5F107DEMSP#X0

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-SSOP38-0300-0.65	PRSP0038JA-A	P38MC-65-2A4-2	0.3









(UNIT:mm)

ITEM	DIMENSIONS
A	12.30±0.10
B	0.30
C	0.65 (T.P.)
D	$0.32^{+0.08}_{-0.07}$
E	0.125±0.075
F	2.00 MAX.
G	1.70±0.10
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.17^{+0.08}_{-0.07}$
L	0.50
M	0.10
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.