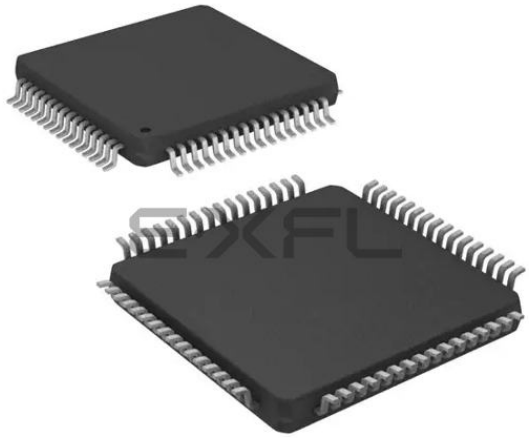

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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TABLE 1-1: DEVICE FEATURES FOR THE PIC18F85J90 FAMILY (64-PIN DEVICES)

Features	PIC18F63J90	PIC18F64J90	PIC18F65J90
Operating Frequency	DC – 40 MHz		
Program Memory (Bytes)	8K	16K	32K
Program Memory (Instructions)	4096	8192	16384
Data Memory (Bytes)	1024	1024	2048
Interrupt Sources	27		
I/O Ports	Ports A, B, C, D, E, F, G		
LCD Driver (available pixels to drive)	132 (33 SEGs x 4 COMs)		
Timers	4		
Capture/Compare/PWM Modules	2		
Serial Communications	MSSP, Addressable USART, Enhanced USART		
10-Bit Analog-to-Digital Module	12 Input Channels		
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set enabled		
Packages	64-pin TQFP		

TABLE 1-2: DEVICE FEATURES FOR THE PIC18F85J90 FAMILY (80-PIN DEVICES)

Features	PIC18F83J90	PIC18F84J90	PIC18F85J90
Operating Frequency	DC – 40 MHz		
Program Memory (Bytes)	8K	16K	32K
Program Memory (Instructions)	4096	8192	16384
Data Memory (Bytes)	1024	1024	2048
Interrupt Sources	27		
I/O Ports	Ports A, B, C, D, E, F, G, H, J		
LCD Driver (available pixels to drive)	192 (48 SEGs x 4 COMs)		
Timers	4		
Capture/Compare/PWM Modules	2		
Serial Communications	MSSP, Addressable USART, Enhanced USART		
10-Bit Analog-to-Digital Module	12 Input Channels		
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set enabled		
Packages	80-pin TQFP		

Note: The Timer1 oscillator should already be running prior to entering SEC_RUN mode. If the T1OSCEN bit is not set when the SCS<1:0> bits are set to '01', entry to SEC_RUN mode will not occur. If the Timer1 oscillator is enabled, but not yet running, device clocks will be delayed until the oscillator has started. In such situations, initial oscillator operation is far from stable and unpredictable operation may result.

On transitions from SEC_RUN mode to PRI_RUN mode, the peripherals and CPU continue to be clocked from the Timer1 oscillator while the primary clock is started. When the primary clock becomes ready, a clock switch back to the primary clock occurs (see Figure 4-2). When the clock switch is complete, the T1RUN bit is cleared, the OSTS bit is set and the primary clock is providing the clock. The IDLEN and SCS bits are not affected by the wake-up; the Timer1 oscillator continues to run.

FIGURE 4-1: TRANSITION TIMING FOR ENTRY TO SEC_RUN MODE

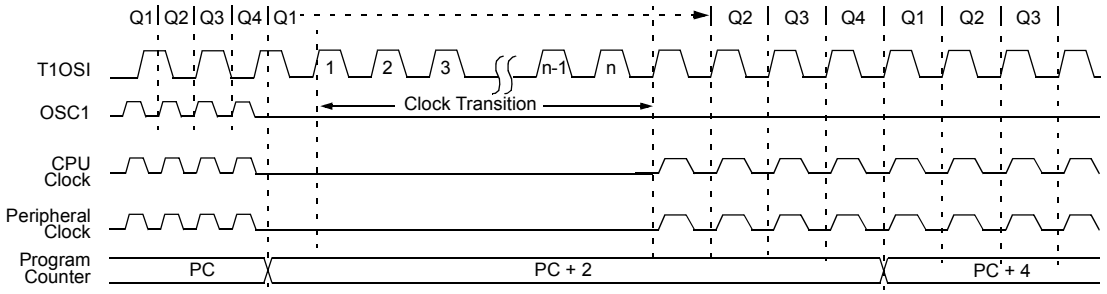
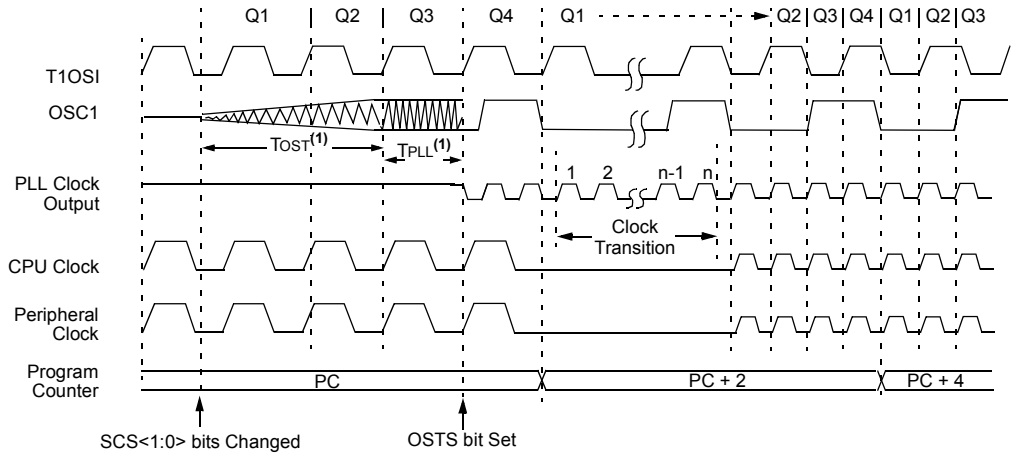


FIGURE 4-2: TRANSITION TIMING FROM SEC_RUN MODE TO PRI_RUN MODE (HSPLL)



Note 1: TOST = 1024 TOSC; TPLL = 2 ms (approx). These intervals are not shown to scale.

A CM Reset behaves similarly to a Master Clear Reset, RESET instruction, WDT time-out or Stack Event Resets. As with all hard and power Reset events, the device Configuration Words are reloaded from the Flash Configuration Words in program memory as the device restarts.

5.6 Power-up Timer (PWRT)

PIC18F85J90 family devices incorporate an on-chip Power-up Timer (PWRT) to help regulate the Power-on Reset process. The PWRT is always enabled. The main function is to ensure that the device voltage is stable before code is executed.

The Power-up Timer (PWRT) of the PIC18F85J90 family devices is an 11-bit counter which uses the INTRC source as the clock input. This yields an approximate time interval of 2048 x 32 μs = 65.6 ms. While the PWRT is counting, the device is held in Reset.

The power-up time delay depends on the INTRC clock and will vary from chip-to-chip due to temperature and process variation. See DC parameter 33 for details.

5.6.1 TIME-OUT SEQUENCE

If enabled, the PWRT time-out is invoked after the POR pulse has cleared. The total time-out will vary based on the status of the PWRT. Figure 5-3, Figure 5-4, Figure 5-5 and Figure 5-6 all depict time-out sequences on power-up with the Power-up Timer enabled.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the PWRT will expire. Bringing $\overline{\text{MCLR}}$ high will begin execution immediately (Figure 5-5). This is useful for testing purposes, or to synchronize more than one PIC18FXXXX device operating in parallel.

FIGURE 5-3: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD}, V_{DD} RISE < T_{PWRT})

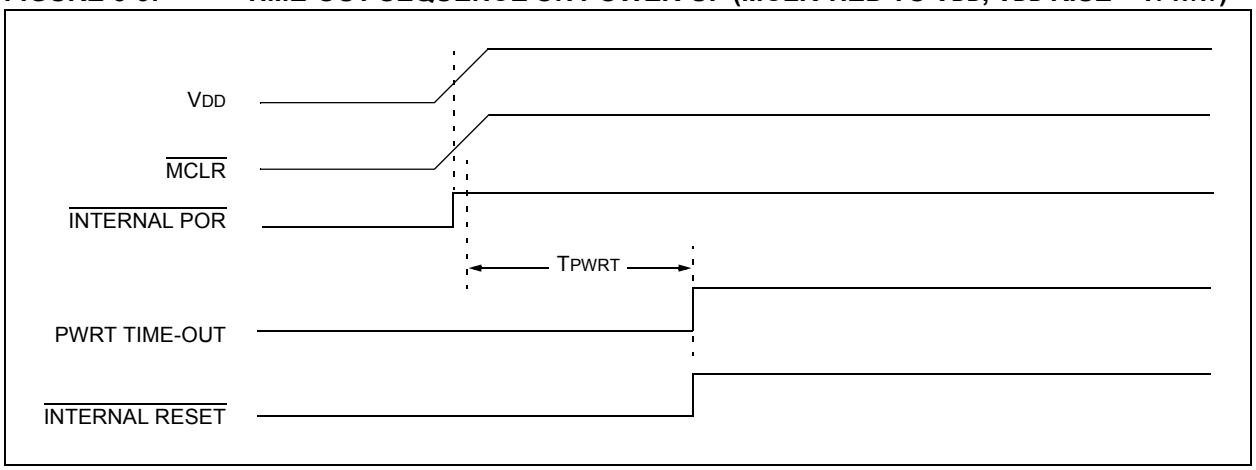


FIGURE 5-4: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1

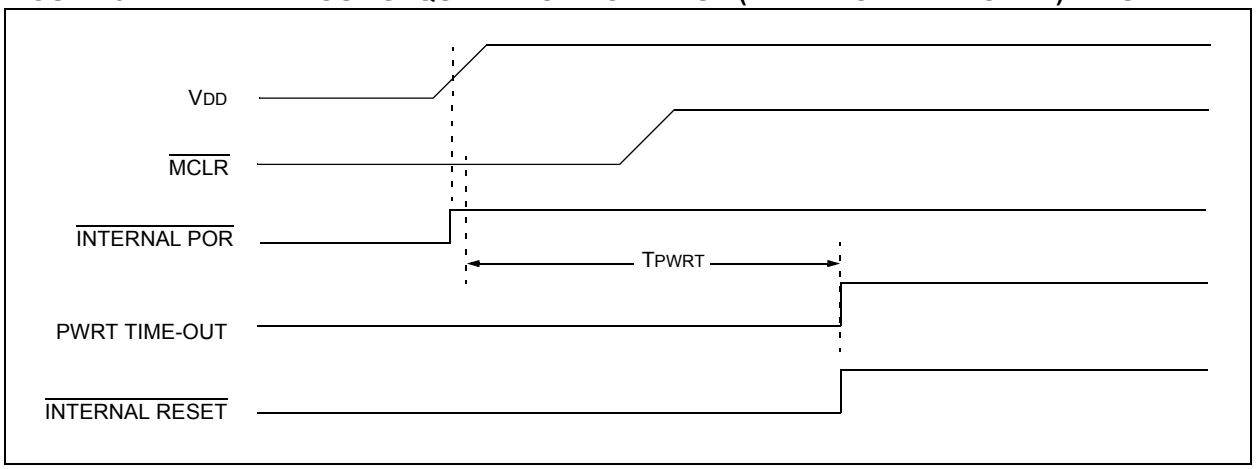


TABLE 10-18: PORTH FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RH0/SEG47	RH0	0	O	DIG	LATH<0> data output.
		1	I	ST	PORTH<0> data input.
	SEG47	x	O	ANA	LCD Segment 47 output; disables all other pin functions.
RH1/SEG46	RH1	0	O	DIG	LATH<1> data output.
		1	I	ST	PORTH<1> data input.
	SEG46	x	O	ANA	LCD Segment 46 output; disables all other pin functions.
RH2/SEG45	RH2	0	O	DIG	LATH<2> data output.
		1	I	ST	PORTH<2> data input.
	SEG45	x	O	ANA	LCD Segment 45 output; disables all other pin functions.
RH3/SEG44	RH3	0	O	DIG	LATH<3> data output.
		1	I	ST	PORTH<3> data input.
	SEG44	x	O	ANA	LCD Segment 44 output; disables all other pin functions.
RH4/SEG40	RH4	0	O	DIG	LATH<4> data output.
		1	I	ST	PORTH<4> data input.
	SEG40	x	O	ANA	LCD Segment 40 output; disables all other pin functions.
RH5/SEG41	RH5	0	O	DIG	LATH<5> data output.
		1	I	ST	PORTH<5> data input.
	SEG41	x	O	ANA	LCD Segment 41 output; disables all other pin functions.
RH6/SEG42	RH6	0	O	DIG	LATH<6> data output.
		1	I	ST	PORTH<6> data input.
	SEG42	x	O	ANA	LCD Segment 42 output; disables all other pin functions.
RH7/SEG43	RH7	0	O	DIG	LATH<7> data output.
		1	I	ST	PORTH<7> data input.
	SEG43	x	O	ANA	LCD Segment 43 output; disables all other pin functions.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input,
x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

TABLE 10-19: SUMMARY OF REGISTERS ASSOCIATED WITH PORTH

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTH	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	60
LATH	LATH7	LATH6	LATH5	LATH4	LATH3	LATH2	LATH1	LATH0	60
TRISH	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	60
LCDSE5	SE47	SE46	SE45	SE44	SE43	SE42	SE41	SE40	59

13.2 Timer2 Interrupt

Timer2 can also generate an optional device interrupt. The Timer2 output signal (TMR2 to PR2 match) provides the input for the 4-bit output counter/postscaler. This counter generates the TMR2 match interrupt flag which is latched in TMR2IF (PIR1<1>). The interrupt is enabled by setting the TMR2 Match Interrupt Enable bit, TMR2IE (PIE1<1>).

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, T2OUTPS<3:0> (T2CON<6:3>).

13.3 Timer2 Output

The unscaled output of TMR2 is available primarily to the CCP modules, where it is used as a time base for operations in PWM mode.

Timer2 can be optionally used as the shift clock source for the MSSP module operating in SPI mode. Additional information is provided in **Section 17.0 "Master Synchronous Serial Port (MSSP) Module"**.

FIGURE 13-1: TIMER2 BLOCK DIAGRAM

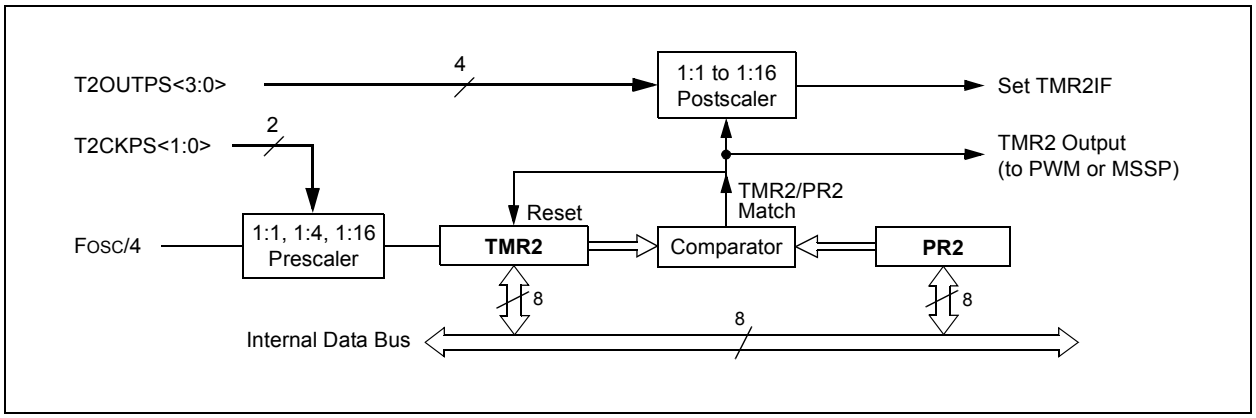


TABLE 13-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	57
PIR1	—	ADIF	RC1IF	TX1IF	SSPIF	—	TMR2IF	TMR1IF	60
PIE1	—	ADIE	RC1IE	TX1IE	SSPIE	—	TMR2IE	TMR1IE	60
IPR1	—	ADIP	RC1IP	TX1IP	SSPIP	—	TMR2IP	TMR1IP	60
TMR2	Timer2 Register								58
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	58
PR2	Timer2 Period Register								58

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

14.2 Timer3 16-Bit Read/Write Mode

Timer3 can be configured for 16-bit reads and writes (see Figure 14-2). When the RD16 control bit (T3CON<7>) is set, the address for TMR3H is mapped to a buffer register for the high byte of Timer3. A read from TMR3L will load the contents of the high byte of Timer3 into the Timer3 High Byte Buffer register. This provides the user with the ability to accurately read all 16 bits of Timer1 without having to determine whether a read of the high byte, followed by a read of the low byte, has become invalid due to a rollover between reads.

A write to the high byte of Timer3 must also take place through the TMR3H Buffer register. The Timer3 high byte is updated with the contents of TMR3H when a write occurs to TMR3L. This allows a user to write all 16 bits to both the high and low bytes of Timer3 at once.

The high byte of Timer3 is not directly readable or writable in this mode. All reads and writes must take place through the Timer3 High Byte Buffer register.

Writes to TMR3H do not clear the Timer3 prescaler. The prescaler is only cleared on writes to TMR3L.

14.3 Using the Timer1 Oscillator as the Timer3 Clock Source

The Timer1 internal oscillator may be used as the clock source for Timer3. The Timer1 oscillator is enabled by setting the T1OSCEN (T1CON<3>) bit. To use it as the Timer3 clock source, the TMR3CS bit must also be set. As previously noted, this also configures Timer3 to increment on every rising edge of the oscillator source.

The Timer1 oscillator is described in **Section 12.0 "Timer1 Module"**.

14.4 Timer3 Interrupt

The TMR3 register pair (TMR3H:TMR3L) increments from 0000h to FFFFh and overflows to 0000h. The Timer3 interrupt, if enabled, is generated on overflow and is latched in interrupt flag bit, TMR3IF (PIR2<1>). This interrupt can be enabled or disabled by setting or clearing the Timer3 Interrupt Enable bit, TMR3IE (PIE2<1>).

14.5 Resetting Timer3 Using the CCP Special Event Trigger

If CCP1 or CCP2 is configured to use Timer3 and to generate a Special Event Trigger in Compare mode (CCPxM<3:0> = 1011), this signal will reset Timer3. The trigger from CCP2 will also start an A/D conversion if the A/D module is enabled (see **Section 15.3.4 "Special Event Trigger"** for more information).

The module must be configured as either a timer or synchronous counter to take advantage of this feature. When used this way, the CCPRxH:CCPRxL register pair effectively becomes a period register for Timer3.

If Timer3 is running in Asynchronous Counter mode, the Reset operation may not work.

In the event that a write to Timer3 coincides with a Special Event Trigger from a CCP module, the write will take precedence.

Note:	The Special Event Triggers from the CCPx module will not set the TMR3IF interrupt flag bit (PIR2<1>).

TABLE 14-1: REGISTERS ASSOCIATED WITH TIMER3 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	57
PIR2	OSCFIF	CMIF	—	—	BCLIF	LVDIF	TMR3IF	—	60
PIE2	OSCFIE	CMIE	—	—	BCLIE	LVDIE	TMR3IE	—	60
IPR2	OSCFIP	CMIP	—	—	BCLIP	LVDIP	TMR3IP	—	60
TMR3L	Timer3 Register Low Byte								59
TMR3H	Timer3 Register High Byte								59
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	58
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	$\overline{\text{T3SYNC}}$	TMR3CS	TMR3ON	59

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Timer3 module.

TABLE 15-2: INTERACTIONS BETWEEN CCP1 AND CCP2 FOR TIMER RESOURCES

CCP1 Mode	CCP2 Mode	Interaction
Capture	Capture	Each module can use TMR1 or TMR3 as the time base. The time base can be different for each CCP.
Capture	Compare	CCP2 can be configured for the Special Event Trigger to reset TMR1 or TMR3 (depending upon which time base is used). Automatic A/D conversions on a trigger event can also be done. Operation of CCP1 could be affected if it is using the same timer as a time base.
Compare	Capture	CCP1 can be configured for the Special Event Trigger to reset TMR1 or TMR3 (depending upon which time base is used). Operation of CCP2 could be affected if it is using the same timer as a time base.
Compare	Compare	Either module can be configured for the Special Event Trigger to reset the time base. Automatic A/D conversions on CCP2 trigger event can be done. Conflicts may occur if both modules are using the same time base.
Capture	PWM	None
Compare	PWM	None
PWM	Capture	None
PWM	Compare	None
PWM	PWM	Both PWMs will have the same frequency and update rate (TMR2 interrupt).

15.2 Capture Mode

In Capture mode, the CCPR2H:CCPR2L register pair captures the 16-bit value of the TMR1 or TMR3 register when an event occurs on the CCP2 pin (RC1 or RE7, depending on device configuration). An event is defined as one of the following:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

The event is selected by the mode select bits, CCP2M<3:0> (CCP2CON<3:0>). When a capture is made, the interrupt request flag bit, CCP2IF (PIR3<2>), is set; it must be cleared in software. If another capture occurs before the value in register, CCPR2, is read, the old captured value is overwritten by the new captured value.

15.2.1 CCP PIN CONFIGURATION

In Capture mode, the appropriate CCPx pin should be configured as an input by setting the corresponding TRIS direction bit.

Note:	If RC1/CCP2 or RE7/CCP2 is configured as an output, a write to the port can cause a capture condition.

15.2.2 TIMER1/TIMER3 MODE SELECTION

The timers that are to be used with the capture feature (Timer1 and/or Timer3) must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation may not work. The timer to be used with each CCP module is selected in the T3CON register (see **Section 15.1.1 "CCP Modules and Timer Resources"**).

15.2.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP2IE bit (PIE3<2>) clear to avoid false interrupts and should clear the flag bit, CCP2IF, following any such change in operating mode.

15.2.4 CCP PRESCALER

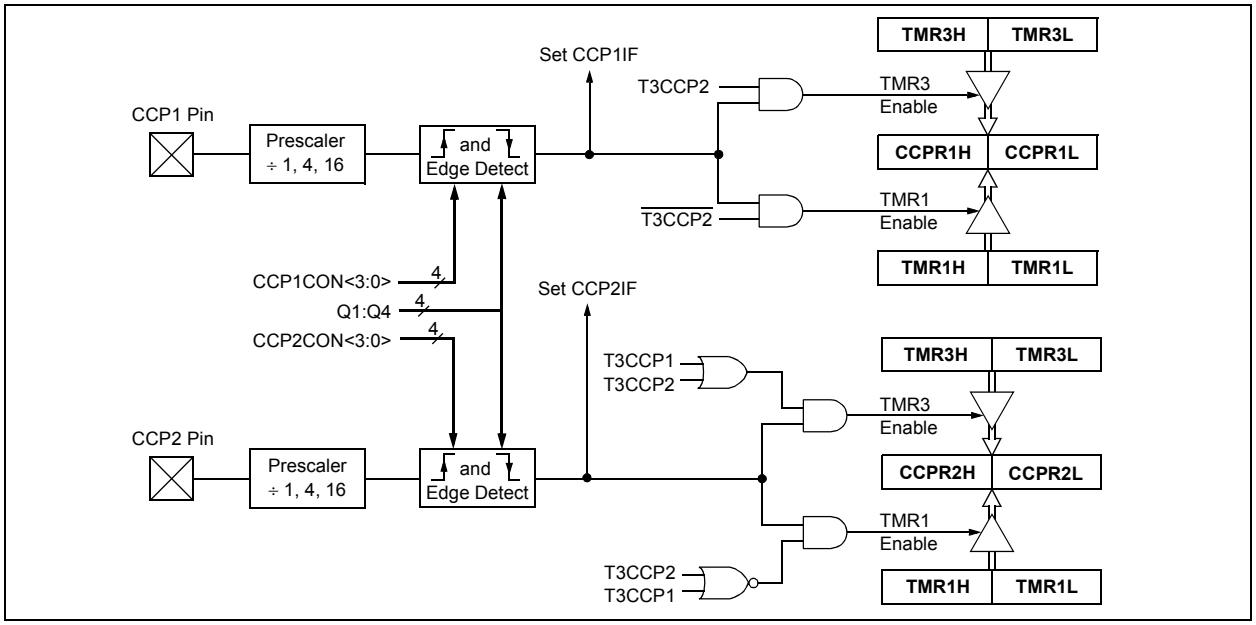
There are four prescaler settings in Capture mode. They are specified as part of the operating mode selected by the mode select bits (CCP2M<3:0>). Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared; therefore, the first capture may be from a non-zero prescaler. Example 15-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 15-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF   CCP2CON      ; Turn CCP module off
MOVLW  NEW_CAPT_PS  ; Load WREG with the
                    ; new prescaler mode
                    ; value and CCP ON
MOVWF  CCP2CON      ; Load CCP2CON with
                    ; this value
```

FIGURE 15-2: CAPTURE MODE OPERATION BLOCK DIAGRAM



16.7 LCD Frame Frequency

The rate at which the COM and SEG outputs changes is called the LCD frame frequency. Frame frequency is set by the LP<3:0> bits (LCDPS<3:0>), and is also affected by the Multiplex mode being used. The relationship between the Multiplex mode, LP bits setting and frame rate is shown in Table 16-4 and Table 16-5.

TABLE 16-4: FRAME FREQUENCY FORMULAS

Multiplex Mode	Frame Frequency (Hz)
Static	Clock source/(4 x 1 x (LP3:LP0 + 1))
1/2	Clock source/(2 x 2 x (LP3:LP0 + 1))
1/3	Clock source/(1 x 3 x (LP3:LP0 + 1))
1/4	Clock source/(1 x 4 x (LP3:LP0 + 1))

TABLE 16-5: APPROXIMATE FRAME FREQUENCY (IN Hz) FOR LP PRESCALER SETTINGS

LP<3:0>	Multiplex Mode			
	Static	1/2	1/3	1/4
1	125	125	167	125
2	83	83	111	83
3	62	62	83	62
4	50	50	67	50
5	42	42	56	42
6	36	36	48	36
7	31	31	42	31

16.8 LCD Waveform Generation

LCD waveform generation is based on the principle that the net AC voltage across the dark pixel should be maximized and the net AC voltage across the clear pixel should be minimized. The net DC voltage across any pixel should be zero.

The COM signal represents the time slice for each common, while the SEG contains the pixel data. The pixel signal (COM-SEG) will have no DC component and it can take only one of the two rms values. The higher rms value will create a dark pixel and a lower rms value will create a clear pixel.

As the number of commons increases, the delta between the two rms values decreases. The delta represents the maximum contrast that the display can have.

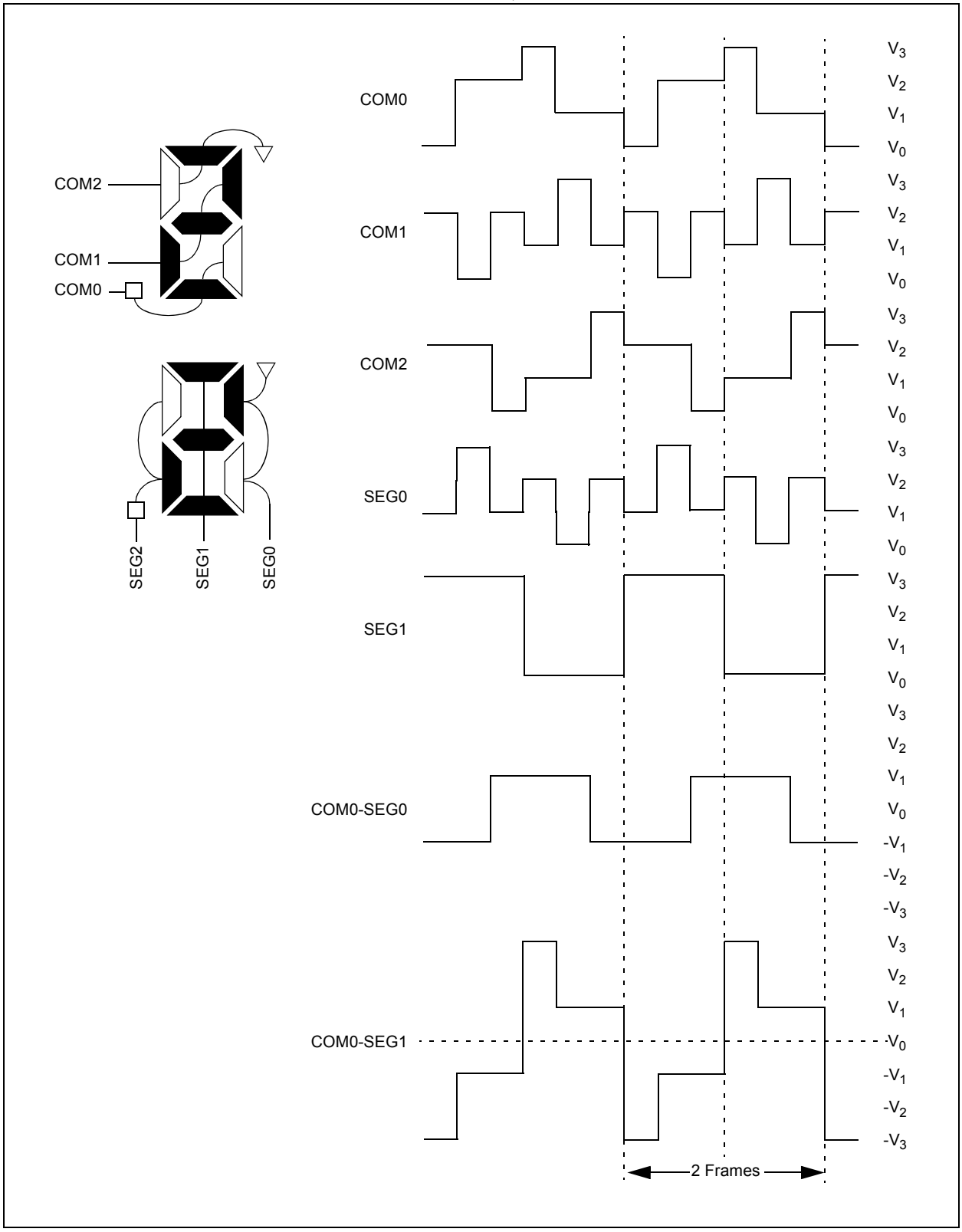
The LCDs can be driven by two types of waveform: Type-A and Type-B. In the Type-A waveform, the phase changes within each common type, whereas in the Type-B waveform, the phase changes on each frame boundary. Thus, the Type-A waveform maintains 0 VDC over a single frame, whereas the Type-B waveform takes two frames.

Note 1: If the power-managed Sleep mode is invoked while the LCD Sleep bit is set (LCDCON<6> is '1'), take care to execute Sleep only when the VDC on all the pixels is '0'.

2: When the LCD clock source is the system clock, the LCD module will go to Sleep if the microcontroller goes into Sleep mode, regardless of the setting of the SPLEN bit. Thus, always take care to see that the VDC on all pixels is '0' whenever Sleep mode is invoked.

Figure 16-6 through Figure 16-16 provide waveforms for static, half multiplex, one-third multiplex and quarter multiplex drives for Type-A and Type-B waveforms.

FIGURE 16-14: TYPE-B WAVEFORMS IN 1/3 MUX, 1/3 BIAS DRIVE



17.4.3.2 Address Masking

Masking an address bit causes that bit to become a "don't care". When one address bit is masked, two addresses will be Acknowledged and cause an interrupt. It is possible to mask more than one address bit at a time, which makes it possible to Acknowledge up to 31 addresses in 7-bit mode and up to 63 addresses in 10-bit mode (see Example 17-2).

The I^2C Slave behaves the same way whether address masking is used or not. However, when address masking is used, the I^2C slave can Acknowledge multiple addresses and cause interrupts. When this occurs, it is necessary to determine which address caused the interrupt by checking SSPBUF.

In 7-Bit Address mode, address mask bits, ADMSK<5:1> (SSPCON<5:1>), mask the corresponding address bits in the SSPADD register. For any ADMSK bits that are set (ADMSK<n> = 1), the corresponding address bit is ignored (SSPADD<n> = x). For the module to issue an address Acknowledge, it is sufficient to match only on addresses that do not have an active address mask.

In 10-Bit Address mode, the ADMSK<5:2> bits mask the corresponding address bits in the SSPADD register. In addition, ADMSK1 simultaneously masks the two LSbs of the address (SSPADD<1:0>). For any ADMSK bits that are active (ADMSK<n> = 1), the corresponding address bit is ignored (SSPADD<n> = x). Also note, that although in 10-Bit Addressing mode, the upper address bits reuse part of the SSPADD register bits. The address mask bits do not interact with those bits; they only affect the lower address bits.

Note 1: ADMSK1 masks the two Least Significant bits of the address.

2: The two Most Significant bits of the address are not affected by address masking.

EXAMPLE 17-2: ADDRESS MASKING EXAMPLES

7-Bit Addressing:

SSPADD<7:1> = A0h (1010000) (SSPADD<0> is assumed to be '0')

ADMSK<5:1> = 00111

Addresses Acknowledged: A0h, A2h, A4h, A6h, A8h, AAh, ACh, AEh

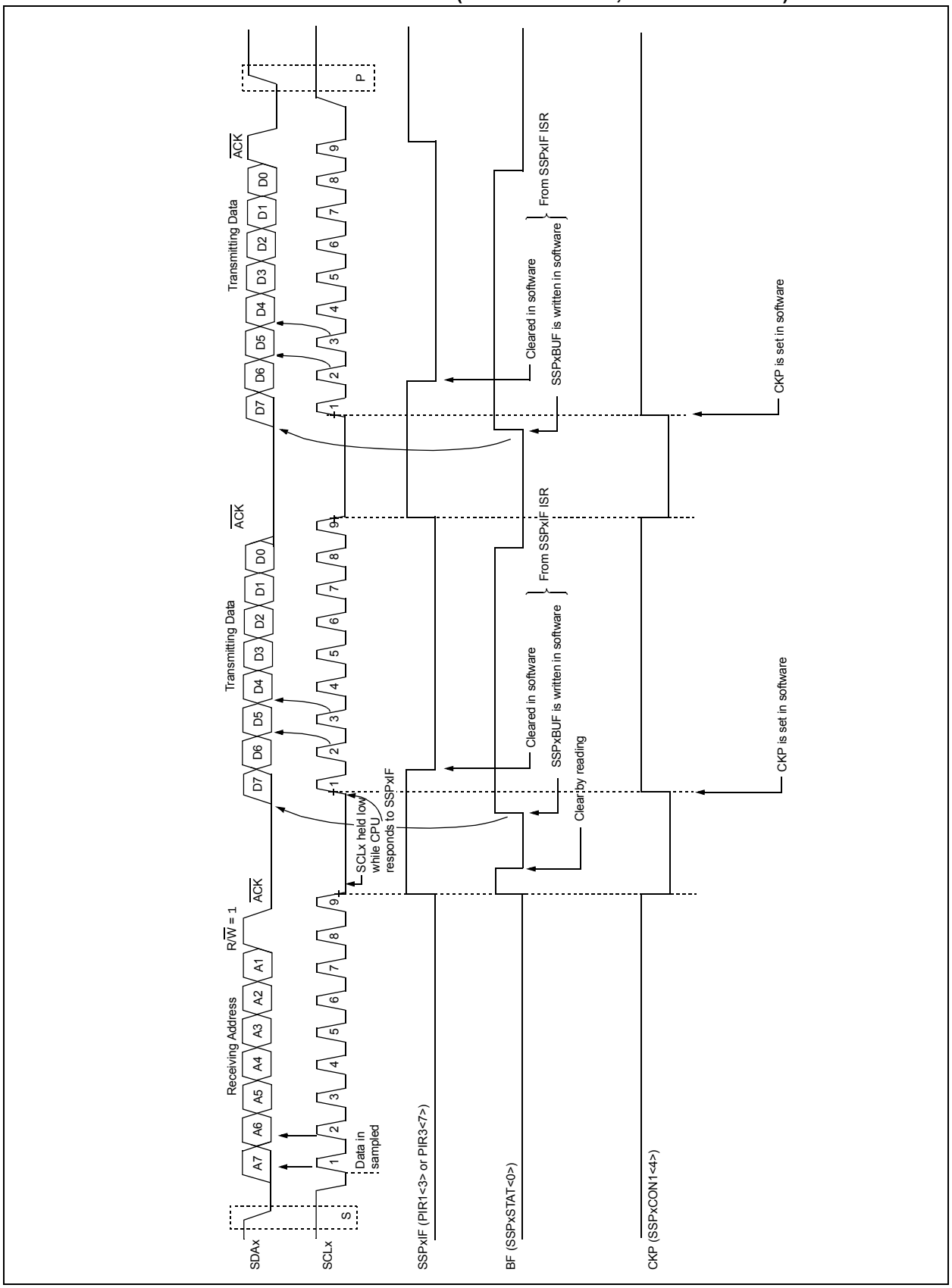
10-Bit Addressing:

SSPADD<7:0> = A0h (10100000) (the two MSbs of the address are ignored in this example, since they are not affected by masking)

ADMSK<5:1> = 00111

Addresses Acknowledged: A0h, A1h, A2h, A3h, A4h, A5h, A6h, A7h, A8h, A9h, AAh, ABh, ACh, ADh, AEh, AFh

FIGURE 17-10: I²C™ SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESS)



17.4.17.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level.

b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user deasserts SDA and the pin is allowed to float high, the BRG is loaded with SSPADD<6:0> and counts down to 0. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', see Figure 17-31). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high-to-low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition (see Figure 17-32).

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

FIGURE 17-31: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

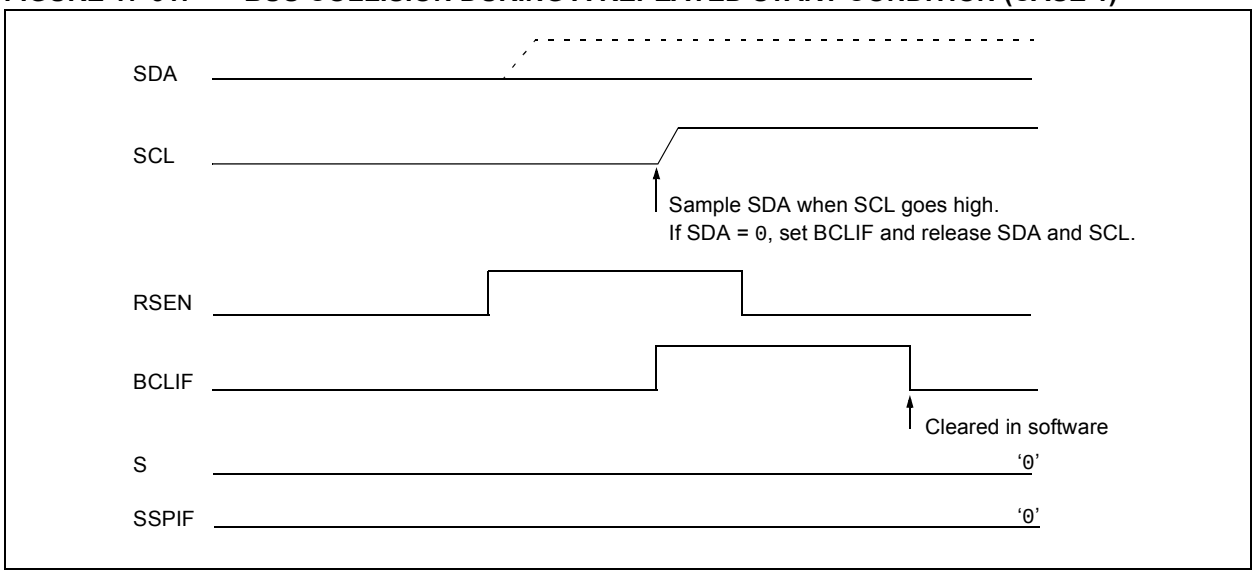


FIGURE 17-32: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)

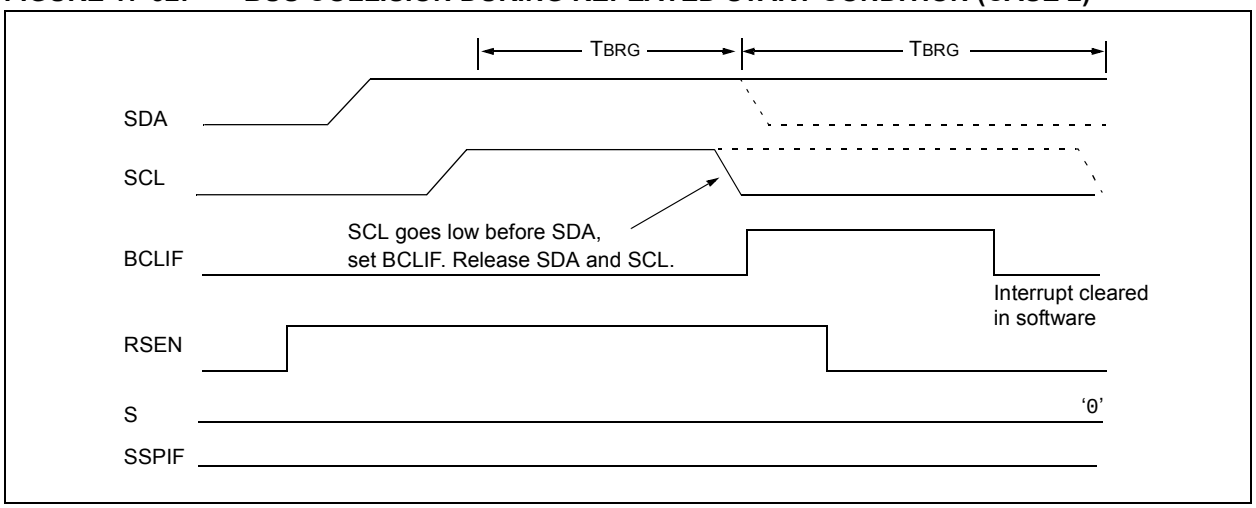


FIGURE 18-12: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)

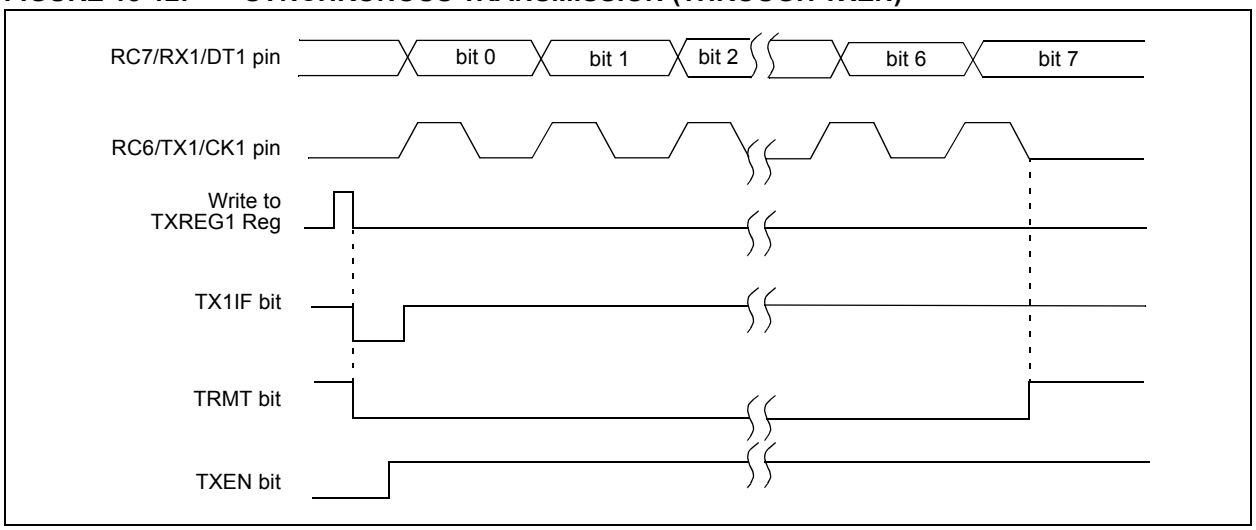


TABLE 18-7: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	57
PIR1	—	ADIF	RC1IF	TX1IF	SSPIF	—	TMR2IF	TMR1IF	60
PIE1	—	ADIE	RC1IE	TX1IE	SSPIE	—	TMR2IE	TMR1IE	60
IPR1	—	ADIP	RC1IP	TX1IP	SSPIP	—	TMR2IP	TMR1IP	60
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	59
TXREG1	EUSART Transmit Register								59
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	59
BAUDCON1	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	61
SPBRGH1	EUSART Baud Rate Generator Register High Byte								61
SPBRG1	EUSART Baud Rate Generator Register Low Byte								59
LATG	U2OD	U1OD	—	LATG4	LATG3	LATG2	LATG1	LATG0	60

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous master transmission.

XORWF **Exclusive OR W with f**

Syntax: XORWF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (W) .XOR. (f) → dest

Status Affected: N, Z

Encoding:

0001	10da	ffff	ffff

Description: Exclusive OR the contents of W with register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in the register 'f'.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 24.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `XORWF REG, 1, 0`

Before Instruction
REG = AFh
W = B5h
After Instruction
REG = 1Ah
W = B5h

TABLE 26-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	100	1K	—	E/W	-40°C to +85°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132	VPEW	Voltage for Self-Timed Erase or Write:					
		VDD	2.35	—	3.6	V	ENVREG tied to VDD
		VDDCORE	2.25	—	2.7	V	ENVREG tied to VSS
D133A	TIW	Self-Timed Write Cycle Time	—	2.8	—	ms	
D133B	TIE	Self-Timed Block Erased Cycle Time	—	33	—	ms	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	3	7	mA	
D1xxx	TWE	Writes per Erase Cycle	—	—	1		Per one physical word address

† Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 26-2: COMPARATOR SPECIFICATIONS

Operating Conditions: 3.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	±5.0	±25	mV	
D301	VICM	Input Common Mode Voltage	0	—	AVDD – 1.5	V	
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	
D303	TRESP	Response Time(1)	—	150	400	ns	
D304	TMC2OV	Comparator Mode Change to Output Valid*	—	—	10	μs	
D305	VIRV	Internal Reference Voltage	—	1.2	—	V	

Note 1: Response time measured with one comparator input at (AVDD – 1.5)/2, while the other input transitions from VSS to VDD.

26.4 AC (Timing) Characteristics

26.4.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKO	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T13CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

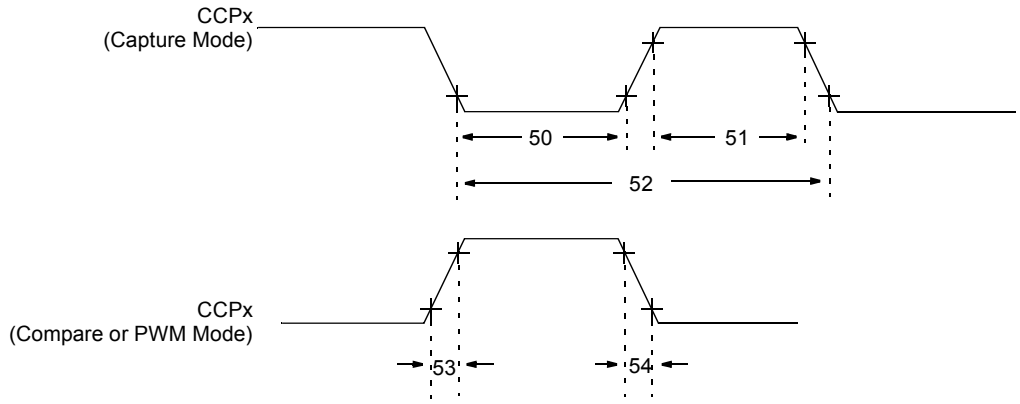
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-Impedance)	V	Valid
L	Low	Z	High-Impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	Stop condition
STA	Start condition		

FIGURE 26-8: CAPTURE/COMPARE/PWM TIMINGS (CCP1, CCP2 MODULES)



Note: Refer to Figure 26-3 for load conditions.

TABLE 26-13: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1, CCP2 MODULES)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
50	TccL	CCPx Input Low Time	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
51	TccH	CCPx Input High Time	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
52	TccP	CCPx Input Period		$\frac{3\ T_{CY} + 40}{N}$	—	ns	N = prescale value (1, 4 or 16)
53	TccR	CCPx Output Fall Time		—	25	ns	
54	TccF	CCPx Output Fall Time		—	25	ns	

V

W

X