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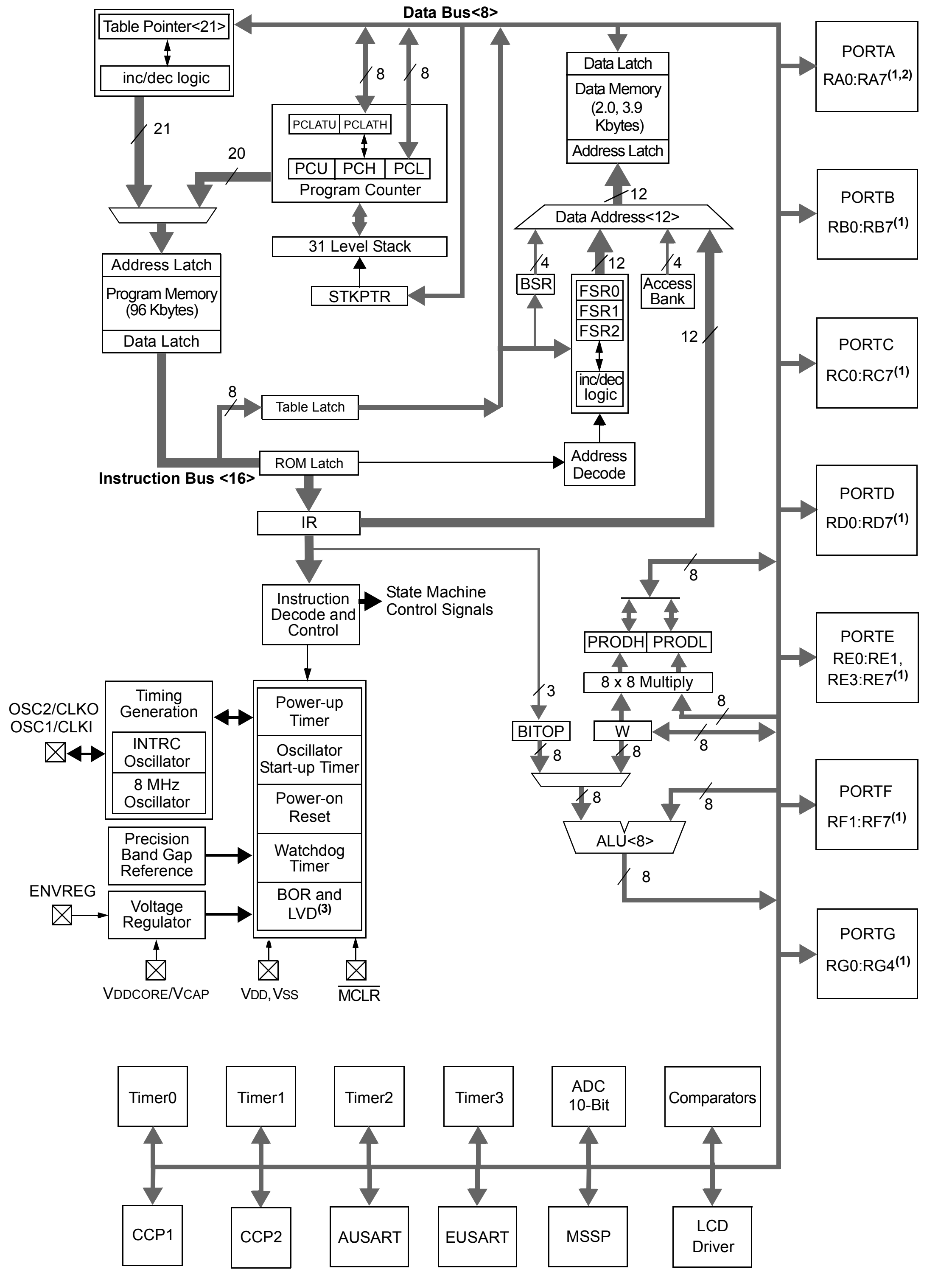
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f83j90-i-pt

FIGURE 1-1: PIC18F6XJ90 (64-PIN) BLOCK DIAGRAM



Note 1: See Table 1-3 for I/O port pin descriptions.

2: RA6 and RA7 are only available as digital I/O in select oscillator modes. See **Section 3.0 “Oscillator Configurations”** for more information

3: Brown-out Reset and Low-Voltage Detect functions are provided when the on-board voltage regulator is enabled.

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets CM Resets	Wake-up via WDT or Interrupt
PORTE	PIC18F6XJ90	PIC18F8XJ90	xxxx x-xx	uuuu u-uu	uuuu u-uu
PORTD	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTB	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA(5)	PIC18F6XJ90	PIC18F8XJ90	xx0x 0000(5)	uu0u 0000(5)	uuuu uuuu(5)
SPBRGH1	PIC18F6XJ90	PIC18F8XJ90	0000 0000	0000 0000	uuuu uuuu
BAUDCON1	PIC18F6XJ90	PIC18F8XJ90	0100 0-00	0100 0-00	uuuu u-uu
LCDDATA23	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA22	PIC18F6XJ90	PIC18F8XJ90	---- ---x	---- ---u	---- ---u
LCDDATA22	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA21	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA20	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA19	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA18	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA17	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA16	PIC18F6XJ90	PIC18F8XJ90	---- ---x	---- ---u	---- ---u
LCDDATA16	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA15	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA14	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA13	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA12	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA11	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA10	PIC18F6XJ90	PIC18F8XJ90	---- ---x	---- ---u	---- ---u
LCDDATA10	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA9	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA8	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA7	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA6	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA5	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1L	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	PIC18F6XJ90	PIC18F8XJ90	--00 0000	--00 0000	--uu uuuu
CCPR2H	PIC18F6XJ90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read as '0'.

EXAMPLE 7-3: WRITING TO FLASH PROGRAM MEMORY

```
                        MOVLW   CODE_ADDR_UPPER         ; Load TBLPTR with the base address
                        MOVWF   TBLPTRU                 ; of the memory block, minus 1
                        MOVLW   CODE_ADDR_HIGH
                        MOVWF   TBLPTRH
                        MOVLW   CODE_ADDR_LOW
                        MOVWF   TBLPTRL
ERASE_BLOCK
                        BSF     EECON1, WREN            ; enable write to memory
                        BSF     EECON1, FREE            ; enable Erase operation
                        BCF     INTCON, GIE             ; disable interrupts
                        MOVLW   55h
                        MOVWF   EECON2                  ; write 55h
                        MOVLW   0AAh
                        MOVWF   EECON2                  ; write 0AAh
                        BSF     EECON1, WR              ; start erase (CPU stall)
                        BSF     INTCON, GIE             ; re-enable interrupts
                        MOVLW   D'16'
                        MOVWF   WRITE_COUNTER           ; Need to write 16 blocks of 64 to write
                                                        ; one erase block of 1024
RESTART_BUFFER
                        MOVLW   D'64'
                        MOVWF   COUNTER
                        MOVLW   BUFFER_ADDR_HIGH        ; point to buffer
                        MOVWF   FSR0H
                        MOVLW   BUFFER_ADDR_LOW
                        MOVWF   FSR0L
FILL_BUFFER
                        ...                             ; read the new data from I2C, SPI,
                                                        ; PSP, USART, etc.
WRITE_BUFFER
                        MOVLW   D’64                    ; number of bytes in holding register
                        MOVWF   COUNTER
WRITE_BYTE_TO_HREGS
                        MOVFF   POSTINC0, WREG          ; get low byte of buffer data
                        MOVWF   TABLAT                  ; present data to table latch
                        TBLWT+*                         ; write data, perform a short write
                                                        ; to internal TBLWT holding register.
                        DECFSZ  COUNTER                 ; loop until buffers are full
                        BRA     WRITE_BYTE_TO_HREGS
PROGRAM_MEMORY
                        BSF     EECON1, WREN            ; enable write to memory
                        BCF     INTCON, GIE             ; disable interrupts
                        MOVLW   55h
    Required            MOVWF   EECON2                  ; write 55h
    Sequence            MOVLW   0AAh
                        MOVWF   EECON2                  ; write 0AAh
                        BSF     EECON1, WR              ; start program (CPU stall)
                        BSF     INTCON, GIE             ; re-enable interrupts
                        BCF     EECON1, WREN            ; disable write to memory

                        DECFSZ  WRITE_COUNTER           ; done with one write cycle
                        BRA     RESTART_BUFFER          ; if not done replacing the erase block
```


REGISTER 9-5: PIR2: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 2

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0
OSCFIF	CMIF	—	—	BCLIF	LVDIF	TMR3IF	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **OSCFIF:** Oscillator Fail Interrupt Flag bit
1 = Device oscillator failed, clock input has changed to INTOSC (must be cleared in software)
0 = Device clock operating

bit 6 **CMIF:** Comparator Interrupt Flag bit
1 = Comparator input has changed (must be cleared in software)
0 = Comparator input has not changed

bit 5-4 **Unimplemented:** Read as ‘0’

bit 3 **BCLIF:** Bus Collision Interrupt Flag bit
1 = A bus collision occurred (must be cleared in software)
0 = No bus collision occurred

bit 2 **LVDIF:** Low-Voltage Detect Interrupt Flag bit
1 = A low-voltage condition occurred (must be cleared in software)
0 = The device voltage is above the regulator’s low-voltage trip point

bit 1 **TMR3IF:** TMR3 Overflow Interrupt Flag bit
1 = TMR3 register overflowed (must be cleared in software)
0 = TMR3 register did not overflow

bit 0 **Unimplemented:** Read as ‘0’

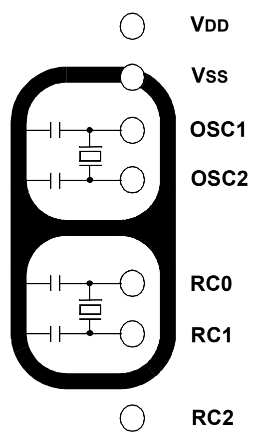
12.3.2 TIMER1 OSCILLATOR LAYOUT CONSIDERATIONS

The Timer1 oscillator circuit draws very little power during operation. Due to the low-power nature of the oscillator, it may also be sensitive to rapidly changing signals in close proximity.

The oscillator circuit, shown in Figure 12-3, should be located as close as possible to the microcontroller. There should be no circuits passing within the oscillator circuit boundaries other than VSS or VDD.

If a high-speed circuit must be located near the oscillator (such as the CCP1 pin in Output Compare or PWM mode, or the primary oscillator using the OSC2 pin), a grounded guard ring around the oscillator circuit, as shown in Figure 12-4, may be helpful when used on a single-sided PCB or in addition to a ground plane.

FIGURE 12-4: OSCILLATOR CIRCUIT WITH GROUNDED GUARD RING



Note: Not drawn to scale.

12.4 Timer1 Interrupt

The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The Timer1 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled or disabled by setting or clearing the Timer1 Interrupt Enable bit, TMR1IE (PIE1<0>).

12.5 Resetting Timer1 Using the CCP Special Event Trigger

If CCP1 or CCP2 is configured to use Timer1 and to generate a Special Event Trigger in Compare mode (CCPxM<3:0> = `1011`), this signal will reset Timer3. The trigger from CCP2 will also start an A/D conversion if the A/D module is enabled (see **Section 15.3.4 “Special Event Trigger”** for more information).

The module must be configured as either a timer or a synchronous counter to take advantage of this feature. When used this way, the CCPRxH:CCPRxL register pair effectively becomes a period register for Timer1.

If Timer1 is running in Asynchronous Counter mode, this Reset operation may not work.

In the event that a write to Timer1 coincides with a Special Event Trigger, the write operation will take precedence.

Note:	The Special Event Triggers from the CCPx module will not set the TMR1IF interrupt flag bit (PIR1<0>).

12.6 Using Timer1 as a Real-Time Clock

Adding an external LP oscillator to Timer1 (such as the one described in **Section 12.3 “Timer1 Oscillator”**) gives users the option to include RTC functionality to their applications. This is accomplished with an inexpensive watch crystal to provide an accurate time base and several lines of application code to calculate the time. When operating in Sleep mode and using a battery or supercapacitor as a power source, it can completely eliminate the need for a separate RTC device and battery backup.

The application code routine, `RTCisr`, shown in Example 12-1, demonstrates a simple method to increment a counter at one-second intervals using an Interrupt Service Routine. Incrementing the TMR1 register pair to overflow triggers the interrupt and calls the routine which increments the seconds counter by one. Additional counters for minutes and hours are incremented as the previous counter overflows.

Since the register pair is 16 bits wide, counting up to overflow the register directly from a 32.768 kHz clock would take 2 seconds. To force the overflow at the required one-second intervals, it is necessary to preload it. The simplest method is to set the MSb of TMR1H with a `BSF` instruction. Note that the TMR1L register is never preloaded or altered; doing so may introduce cumulative error over many cycles.

For this method to be accurate, Timer1 must operate in Asynchronous mode and the Timer1 overflow interrupt must be enabled (PIE1<0> = `1`) as shown in the routine, `RTCinit`. The Timer1 oscillator must also be enabled and running at all times.

16.3.3 BIAS CONFIGURATIONS

PIC18F85J90 family devices have four distinct circuit configurations for LCD bias generation:

- M0: Regulator with Boost
- M1: Regulator without Boost
- M2: Resistor Ladder with Software Contrast
- M3: Resistor Ladder with Hardware Contrast

16.3.3.1 M0 (Regulator with Boost)

In M0 operation, the LCD charge pump feature is enabled. This allows the regulator to generate voltages up to +3.6V to the LCD (as measured at LCDBIAS3).

M0 uses a flyback capacitor connected between VLCAP1 and VLCAP2, as well as filter capacitors on LCDBIAS0 through LCDBIAS3, to obtain the required voltage boost (Figure 16-3).

Note:	When the device is put to Sleep while operating in M0 or M1 mode, make sure that the Bias capacitors are fully discharged to get the lowest Sleep current.

The output voltage (VBIAS) is the difference of potential between LCDBIAS3 and LCDBIAS0. It is set by the BIAS<2:0> bits which adjust the offset between LCDBIAS0 and VSS. The flyback capacitor (CFLY) acts as a charge storage element for large LCD loads. This mode is useful in those cases where the voltage requirements of the LCD are higher than the microcontroller's VDD. It also permits software control of the display's contrast by adjustment of bias voltage by changing the value of the BIAS bits.

M0 supports Static and 1/3 Bias types. Generation of the voltage levels for 1/3 Bias is handled automatically, but must be configured in software.

M0 is enabled by selecting a valid regulator clock source (CKSEL<1:0> set to any value except '00') and setting the CPEN bit. If static Bias type is required, the MODE13 bit must be cleared.

16.3.3.2 M1 (Regulator without Boost)

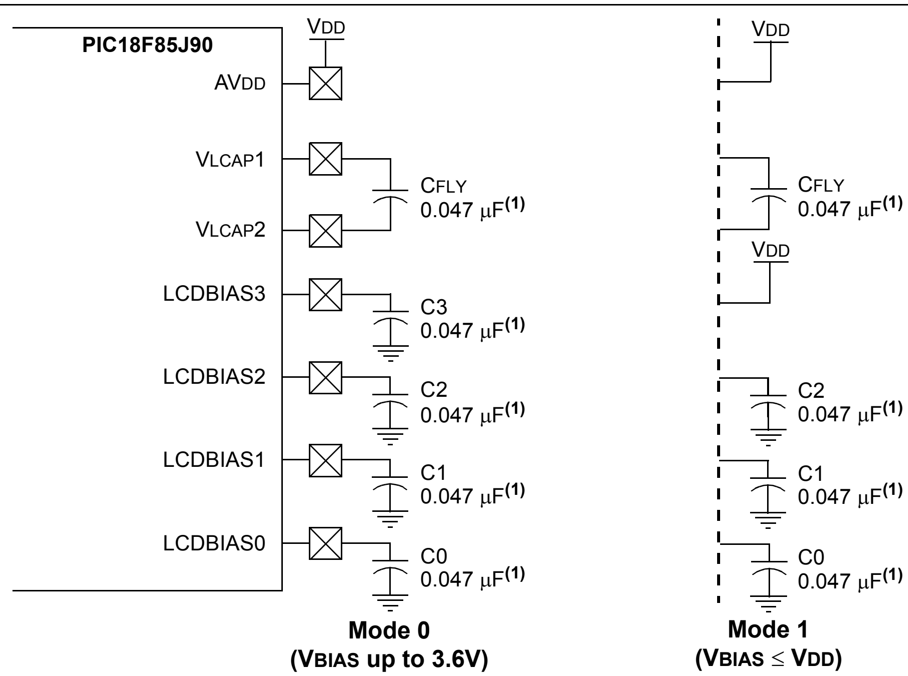
M1 operation is similar to M0, but does not use the LCD charge pump. It can provide VBIAS up to the voltage level supplied directly to LCDBIAS3. It can be used in cases where VDD for the application is expected to never drop below a level that can provide adequate contrast for the LCD. The connection of external components is very similar to M0, except that LCDBIAS3 must be tied directly to VDD (Figure 16-3).

The BIAS<2:0> bits can still be used to adjust contrast in software by changing VBIAS. As with M0, changing these bits changes the offset between LCDBIAS0 and VSS. In M1, this is reflected in the change between the LCDBIAS0 and the voltage tied to LCDBIAS3. Thus, if VDD should change, VBIAS will also change; where in M0, the level of VBIAS is constant.

Like M0, M1 supports Static and 1/3 Bias types. Generation of the voltage levels for 1/3 Bias is handled automatically but must be configured in software.

M1 is enabled by selecting a valid regulator clock source (CKSEL<1:0> set to any value except '00') and clearing the CPEN bit. If 1/3 Bias type is required, the MODE13 bit should also be set.

FIGURE 16-3: LCD REGULATOR CONNECTIONS FOR M0 AND M1 CONFIGURATIONS



Note 1: These values are provided for design guidance only; they should be optimized for the application by the designer based on the actual LCD specifications.

FIGURE 17-16: I²C™ SLAVE MODE TIMING WITH SEN = 1 (RECEPTION, 10-BIT ADDRESS)

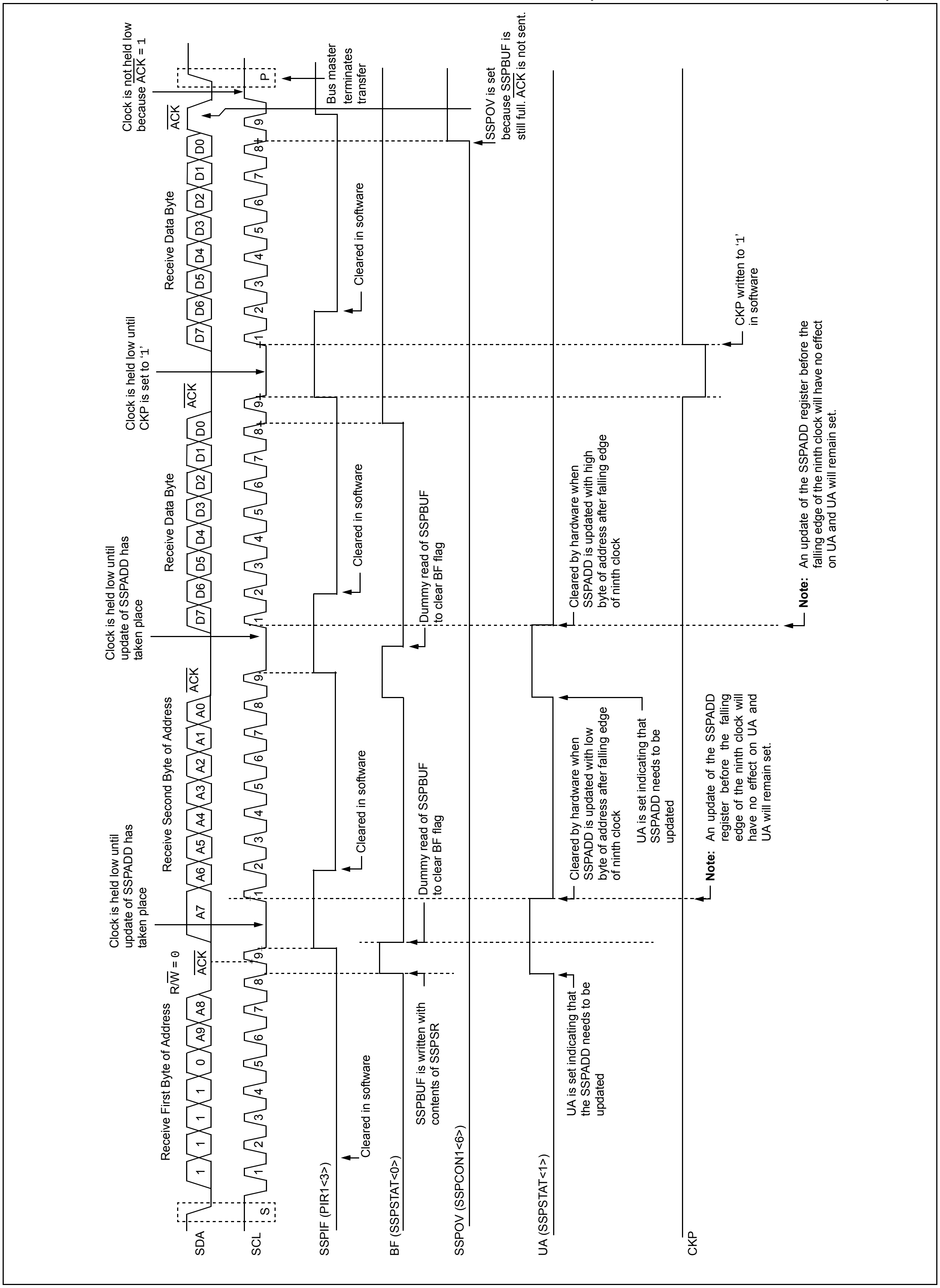
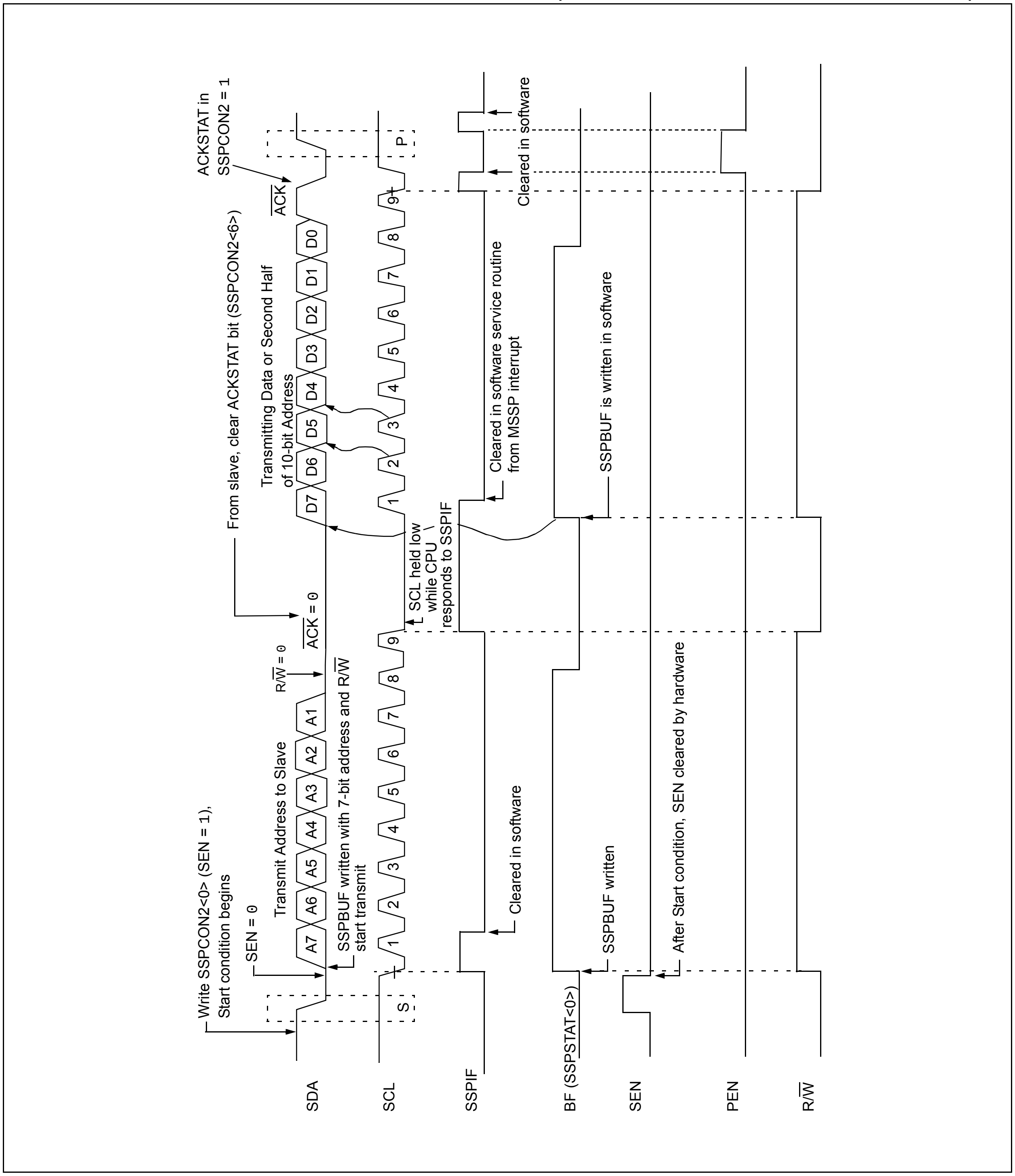


FIGURE 17-23: I²C™ MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)



17.4.17.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

a) SDA or SCL are sampled low at the beginning of the Start condition (Figure 17-28).
b) SCL is sampled low before SDA is asserted low (Figure 17-29).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- the Start condition is aborted;
- the BCLIF flag is set; and
- the MSSP module is reset to its Idle state (Figure 17-28).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded from SSPADD<6:0> and counts down to 0. If the SCL pin is sampled low while SDA is high, a bus collision occurs, because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 17-30). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to 0. If the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note:	The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

FIGURE 17-28: BUS COLLISION DURING START CONDITION (SDA ONLY)

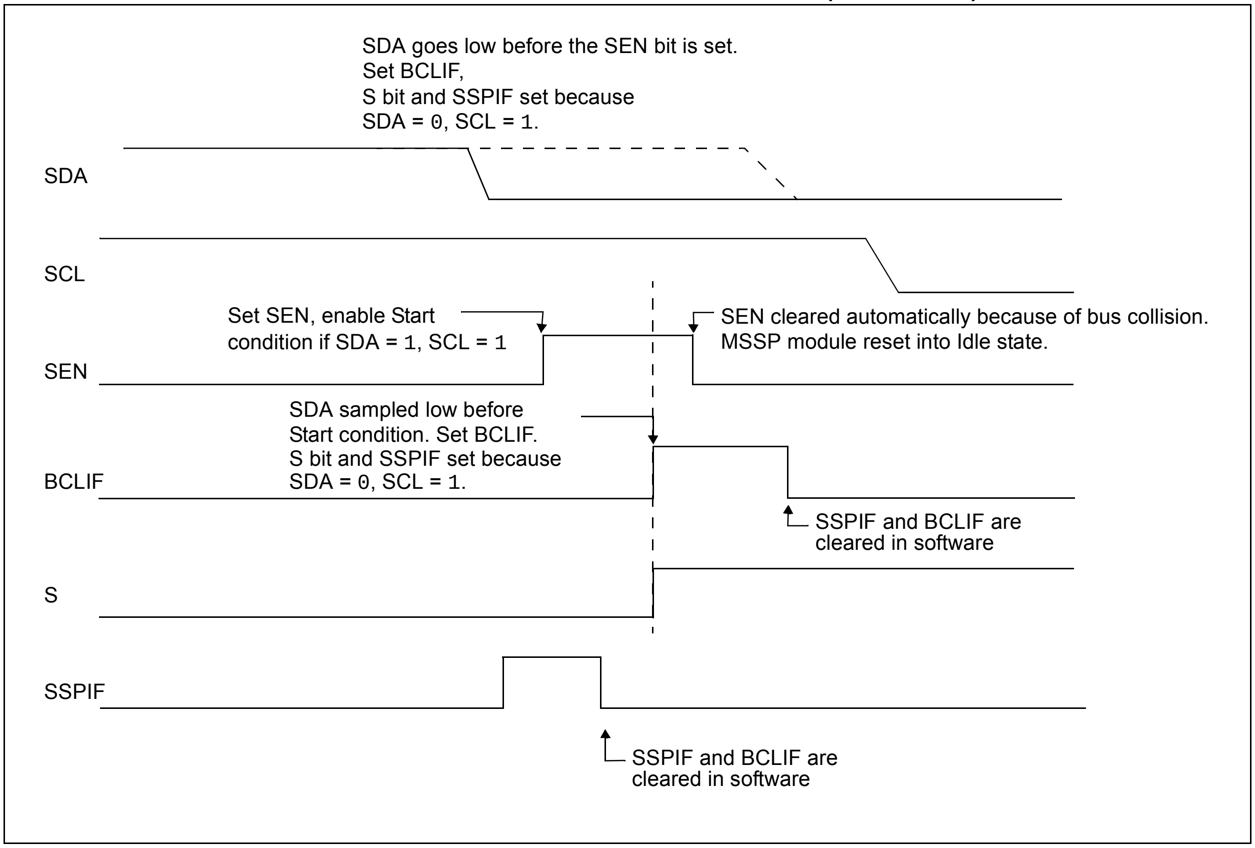


TABLE 17-4: REGISTERS ASSOCIATED WITH I²C™ OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	57
PIR1	—	ADIF	RC1IF	TX1IF	SSPIF	—	TMR2IF	TMR1IF	60
PIE1	—	ADIE	RC1IE	TX1IE	SSPIE	—	TMR2IE	TMR1IE	60
IPR1	—	ADIP	RC1IP	TX1IP	SSPIP	—	TMR2IP	TMR1IP	60
PIR2	OSCFIF	CMIF	—	—	BCLIF	LVDIF	TMR3IF	—	60
PIE2	OSCFIE	CMIE	—	—	BCLIE	LVDIE	TMR3IE	—	60
IPR2	OSCFIP	CMIP	—	—	BCLIP	LVDIP	TMR3IP	—	60
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	60
SSPBUF	MSSP Receive Buffer/Transmit Register								58
SSPADD	MSSP Address Register (I²C™ Slave mode), MSSP Baud Rate Reload Register (I²C Master mode)								58
SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	58
SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	58
	GCEN	ACKSTAT	ADMSK5[(1)]	ADMSK4[(1)]	ADMSK3[(1)]	ADMSK2[(1)]	ADMSK1[(1)]	SEN	
SSPSTAT	SMP	CKE	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF	58

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the MSSP module in I²C™ mode.

Note 1: Alternate bit definitions for use in I²C Slave mode operations only.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (AVDD and AVSS), or the voltage level on the RA3/AN3/VREF+ and RA2/AN2/VREF- pins.

The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

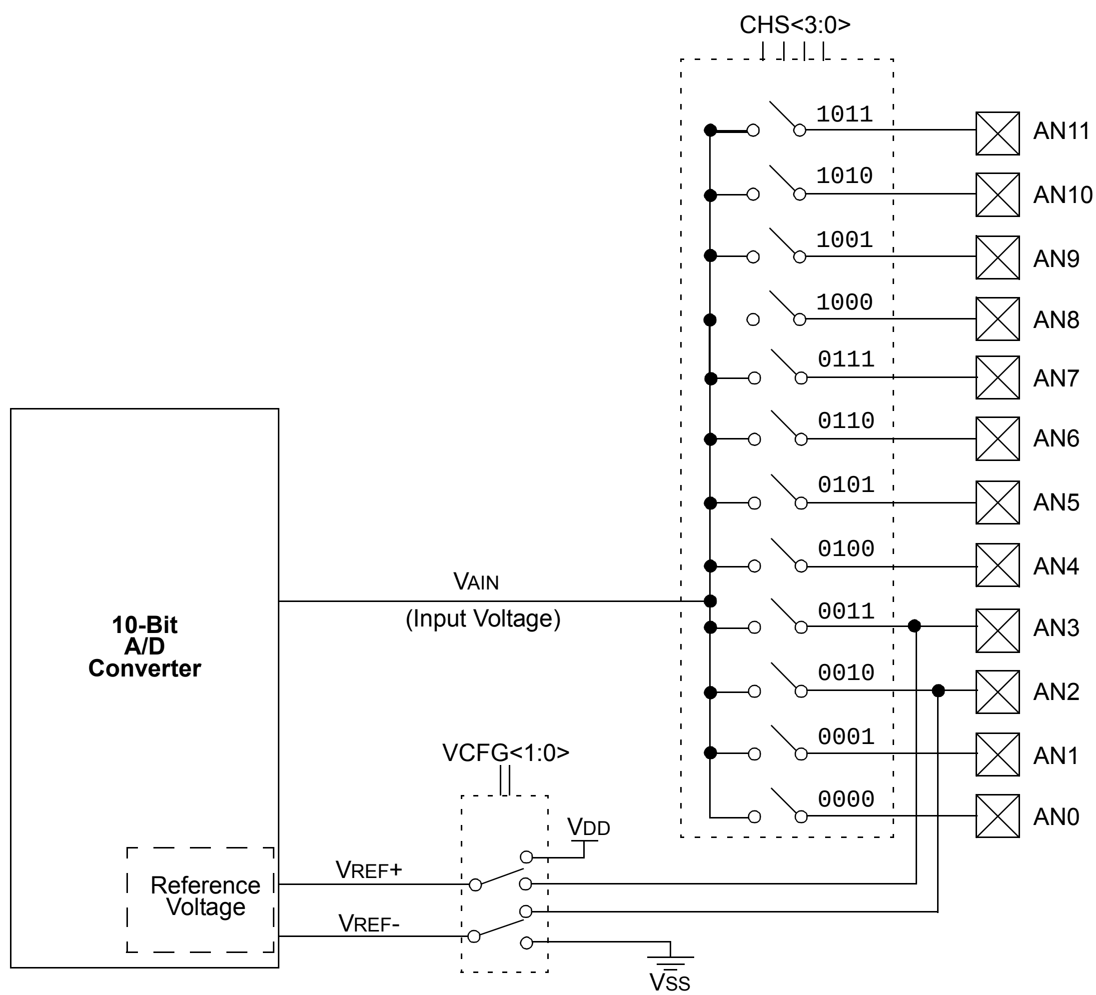
The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and A/D Interrupt Flag bit, ADIF, is set.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted. The value in the ADRESH:ADRESL register pair is not modified for a Power-on Reset. These registers will contain unknown data after a Power-on Reset.

The block diagram of the A/D module is shown in Figure 20-1.

FIGURE 20-1: A/D BLOCK DIAGRAM(1,2)



Note 1: Channels AN15 through AN12 are not available on 64-pin devices.
2: I/O pins have diode protection to VDD and VSS.

NOTES:

REGISTER 23-8: WDTCON: WATCHDOG TIMER CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
REGSLP[(1)]	—	—	—	—	—	—	SWDTEN[(2)]
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **REGSLP:** Voltage Regulator Low-Power Operation Enable bit[(1)]
1 = On-chip regulator enters low-power operation when device enters Sleep mode
0 = On-chip regulator continues to operate normally in Sleep mode

bit 6-1 **Unimplemented**: Read as ‘0’

bit 0 **SWDTEN:** Software Controlled Watchdog Timer Enable bit[(2)]
1 = Watchdog Timer is on
0 = Watchdog Timer is off

Note 1: The REGSLP bit is automatically cleared when a Low-Voltage Detect condition occurs.
2: This bit has no effect if the Configuration bit, WDTEN, is enabled.

TABLE 23-3: SUMMARY OF WATCHDOG TIMER REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
RCON	IPEN	—	$\overline{\text{CM}}$	$\overline{\text{RI}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	58
WDTCON	REGSLP	—	—	—	—	—	—	SWDTEN	58

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used by the Watchdog Timer.

FIGURE 24-1: GENERAL FORMAT FOR INSTRUCTIONS

Example Instruction

Byte-oriented file register operations

15 10	9	8	7 0
OPCODE	d	a	f (FILE #)

`ADDWF MYREG, W, B`

d = `0` for result destination to be WREG register
d = `1` for result destination to be file register (f)
a = `0` to force Access Bank
a = `1` for BSR to select bank
f = 8-bit file register address

Byte to Byte move operations (2-word)

15 12	11 0
OPCODE	f (Source FILE #)

15 12	11 0
`1111`	f (Destination FILE #)

`MOVFF MYREG1, MYREG2`

f = 12-bit file register address

Bit-oriented file register operations

15 12	11 9	8	7 0
OPCODE	b (BIT #)	a	f (FILE #)

`BSF MYREG, bit, B`

b = 3-bit position of bit in file register (f)
a = `0` to force Access Bank
a = `1` for BSR to select bank
f = 8-bit file register address

Literal operations

15 8	7 0
OPCODE	k (literal)

`MOVLW 7Fh`

k = 8-bit immediate value

Control operations

`CALL`, `GOTO` and Branch operations

15 8	7 0
OPCODE	n<7:0> (literal)

15 12	11 0
`1111`	n<19:8> (literal)

`GOTO Label`

n = 20-bit immediate value

15 8	8	7 0
OPCODE	S	n<7:0> (literal)

15 12	11 0
`1111`	n<19:8> (literal)

`CALL MYFUNC`

S = Fast bit

15 11	10 0
OPCODE	n<10:0> (literal)

`BRA MYFUNC`

15 8	7 0
OPCODE	n<7:0> (literal)

`BC MYFUNC`

RETFIE	**Return from Interrupt**
Syntax:	RETFIE {s}
Operands:	s ∈ [0,1]
Operation:	(TOS) → PC, 1 → GIE/GIEH or PEIE/GIEL; if s = 1 (WS) → W, (STATUSS) → STATUS, (BSRS) → BSR, PCLATU, PCLATH are unchanged
Status Affected:	GIE/GIEH, PEIE/GIEL.
Encoding:	`0000` `0000` `0001` `000s`
Description:	Return from interrupt. Stack is popped and Top-of-Stack (TOS) is loaded into the PC. Interrupts are enabled by setting either the high or low-priority global interrupt enable bit. If 's' = 1, the contents of the shadow registers WS, STATUSS and BSRS are loaded into their corresponding registers W, STATUS and BSR. If 's' = 0, no update of these registers occurs.
Words:	1
Cycles:	2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	No operation	POP PC from stack Set GIEH or GIEL
No operation	No operation	No operation	No operation

Example: `RETFIE 1`

After Interrupt

PC	=	TOS
W	=	WS
BSR	=	BSRS
STATUS	=	STATUSS
GIE/GIEH, PEIE/GIEL	=	1

RETLW	**Return Literal to W**
Syntax:	RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → W, (TOS) → PC, PCLATU, PCLATH are unchanged
Status Affected:	None
Encoding:	`0000` `1100` `kkkk` `kkkk`
Description:	W is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). The high address latch (PCLATH) remains unchanged.
Words:	1
Cycles:	2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	POP PC from stack, write to W
No operation	No operation	No operation	No operation

Example:

```
    CALL TABLE ; W contains table
               ; offset value
               ; W now has
               ; table value
   :
TABLE
    ADDWF PCL  ; W = offset
    RETLW k0   ; Begin table
    RETLW k1   ;
   :
   :
    RETLW kn   ; End of table
```

Before Instruction
W = 07h
After Instruction
W = value of kn

25.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

25.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

25.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

25.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

25.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

26.2 DC Characteristics: Power-Down and Supply Current PIC18F85J90 Family (Industrial) (Continued)

PIC18F85J90 Family (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for industrial					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (I_{DD})(2)						
	All devices	2.8	3.8	mA	-40°C	V_{DD} = 2.0V, V_{DDCORE} = 2.0V(4)	F_{OSC} = 4 MHz, 16 MHz internal (**PRI_RUN** mode, HSPLL oscillator)
		3.02	3.8	mA	+25°C		
		3.01	4.5	mA	+85°C		
	All devices	4.5	5.4	mA	-40°C	V_{DD} = 2.5V, V_{DDCORE} = 2.5V(4)	F_{OSC} = 4 MHz, 16 MHz internal (**PRI_RUN** mode, HSPLL oscillator)
		4.8	5.6	mA	+25°C		
		4.54	5.6	mA	+85°C		
	All devices	5.72	6.7	mA	-40°C	V_{DD} = 3.3V(5)	F_{OSC} = 4 MHz, 16 MHz internal (**PRI_RUN** mode, HSPLL oscillator)
		5.55	6.5	mA	+25°C		
		5.3	6.5	mA	+85°C		
	All devices	7.4	8.5	mA	-40°C	V_{DD} = 2.5V, V_{DDCORE} = 2.5V(4)	F_{OSC} = 10 MHz, 40 MHz internal (**PRI_RUN** mode, HSPLL oscillator)
		7.23	8.5	mA	+25°C		
		6.55	7.5	mA	+85°C		
	All devices	9.74	11.6	mA	-40°C	V_{DD} = 3.3V(5)	F_{OSC} = 10 MHz, 40 MHz internal (**PRI_RUN** mode, HSPLL oscillator)
		9.43	11.6	mA	+25°C		
		8.89	10.5	mA	+85°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to V_{DD} or V_{SS}, and all features that add delta current disabled (such as WDT, Timer1 oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD};
$\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator is disabled (ENVREG tied to V_{SS}).

5: Voltage regulator is enabled (ENVREG tied to V_{DD}).

6: Resistor ladder current is not included.

7: Connecting an actual display will increase the current consumption depending on the size of the LCD.

TABLE 26-8: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 2.15V TO 3.6V)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
F10	FOSC	Oscillator Frequency Range	4	—	10	MHz	HS mode only
F11	FSYS	On-Chip VCO System Frequency	16	—	40	MHz	HS mode only
F12	t_{rc}	PLL Start-up Time (Lock Time)	—	—	2	ms	
F13	ΔCLK	CLKO Stability (Jitter)	-2	—	+2	%	

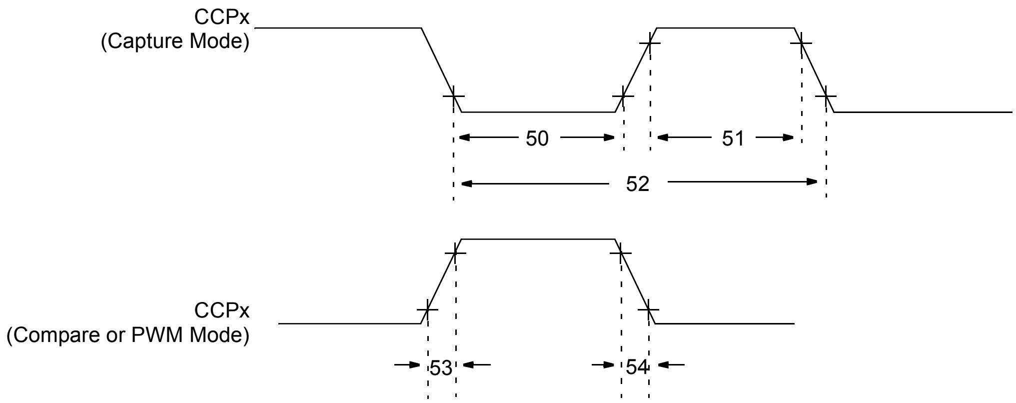
† Data in "Typ" column is at 3.3V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 26-9: INTERNAL RC ACCURACY (INTOSC AND INTRC SOURCES)

PIC18F85J90 Family (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	**Device**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
	INTOSC Accuracy @ Freq = 8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz, 31 kHz(1)						
	All Devices	-2	±1	2	%	+25°C	VDD = 2.7-3.3V
		-5	—	5	%	-10°C to +85°C	VDD = 2.0-3.3V
		-10	±1	10	%	-40°C to +85°C	VDD = 2.0-3.3V
	INTRC Accuracy @ Freq = 31 kHz(1)						
	All Devices	26.562	—	35.938	kHz	-40°C to +85°C	VDD = 2.0-3.3V

Note 1: The accuracy specification of the 31 kHz clock is determined by which source is providing it at a given time. When INTSRC (OSCTUNE<7>) is '1', use the INTOSC accuracy specification. When INTSRC is '0', use the INTRC accuracy specification.

FIGURE 26-8: CAPTURE/COMPARE/PWM TIMINGS (CCP1, CCP2 MODULES)



Note: Refer to Figure 26-3 for load conditions.

TABLE 26-13: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1, CCP2 MODULES)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
50	TCCL	CCPx Input Low Time	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
51	TCCH	CCPx Input High Time	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
52	TCCP	CCPx Input Period		$\frac{3 T_{CY} + 40}{N}$	—	ns	N = prescale value (1, 4 or 16)
53	TCCR	CCPx Output Fall Time		—	25	ns	
54	TCCF	CCPx Output Fall Time		—	25	ns	

B.1 Power Requirement Differences

The most significant difference between the PIC18F85J90 and PIC18F8490 device families is the power requirements. PIC18F85J90 family devices are designed on a smaller process. This results in lower maximum voltage and higher leakage current.

The operating voltage range for PIC18F85J90 devices is 2.0V to 3.6V. In addition, these devices have split power requirements: one for the core logic and one for the I/O. One of the VDD pins is separated for the core logic supply (VDDCORE). This pin has specific voltage and capacitor requirements as described in **Section 26.0 “Electrical Characteristics”**.

B.2 Oscillator Differences

PIC18F8490 and PIC18F85J90 family devices share a similar range of oscillator options. The major difference is that PIC18F85J90 family devices support a smaller number of primary (external) oscillator options, namely HS and EC Oscillator modes.

While both device families have an internal PLL that can be used with the primary oscillators, the PLL for the PIC18F85J90 family is not enabled as a device configuration option. Instead, it must be enabled in software.

The clocking differences should be considered when making a conversion between the PIC18F8490 and PIC18F85J90 device families.

B.3 LCD Module

When converting an LCD application between the PIC18F85J90 and the PIC18F8490 families, the following things must be considered:

- **Available Segments:** The module for PIC18F65J90 devices supports 33 segments, as opposed to 32 segments in PIC18F6490 devices. (The 80-pin devices of both families support 48 segments. All devices support 4 commons.)
- **Bias Generation:** The PIC18F85J90 version of the module also incorporates its own independent voltage regulator, which supports 4 circuit configurations for bias generation, voltage boost to support displays that operate above device VDD and software contrast control.
- **Additional LCD Function Pins:** The PIC18F85J90 family of devices adds 3 additional LCD function pins in comparison to the PIC18F8490 family. The additional pins are associated with LCD bias generation:
  - LCDBIAS0 (RG0)
  - VLCAP1 (RG2)
  - VLCPA2 (RG3)
- **Segment Assignments:** Eight of the LCD segment functions have been relocated to different I/O pins than in PIC18F8490 devices. These segments are listed in Table B-2.
- **Other Considerations:** In all LCD applications, the connections of PIC18F85J90 devices to external components for LCD bias generation are different than PIC18F8490 devices. The addition of the LCDBIAS0 output requires that this pin be included in bias component configurations. A more complete discussion is provided in **Section 16.3 “LCD Bias Generation”**.
  The simultaneous use of the external Timer1 oscillator and Segment 32 is not allowed in PIC18F85J90 devices, since these functions are shared on the same pin.

TABLE B-2: ASSIGNMENTS OF MOVED LCD SEGMENTS

LCD Segment	PIC18F8490	PIC18F85J90
SEG16	RA2	RC4
SEG17	RA3	RC3
SEG18	RF0	RA1
SEG27	RG3	RC6
SEG28	RG2	RC7
SEG29	RG0	RB5
SEG30	RG0	RB0
SEG32	RJ0	RC1

Note: Refer to the pinout diagrams for pin locations of I/O ports.