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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	8 Core, 64-Bit
Speed	1.2GHz
Co-Processors/DSP	-
RAM Controllers	DDR4
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	10GbE (2), 1GbE (8)
SATA	SATA 6Gbps (1)
USB	USB 3.0 (2) + PHY
Voltage - I/O	-
Operating Temperature	0°C ~ 105°C
Security Features	Secure Boot, TrustZone®
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088ase7mqa

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1 Overview

A member of the Layerscape (LS1) series, the LS1088A is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) device featuring eight extremely power-efficient 64-bit ARM® Cortex®-A53 cores with ECC-protected L1 and L2 cache memories for high reliability, running up to 1.6 GHz.

The LS1088A family of devices can be used for enterprise and service provider routers, Virtual CPE, industrial communications, security appliance and military and aerospace applications.

This figure shows the LS1088A block diagram.

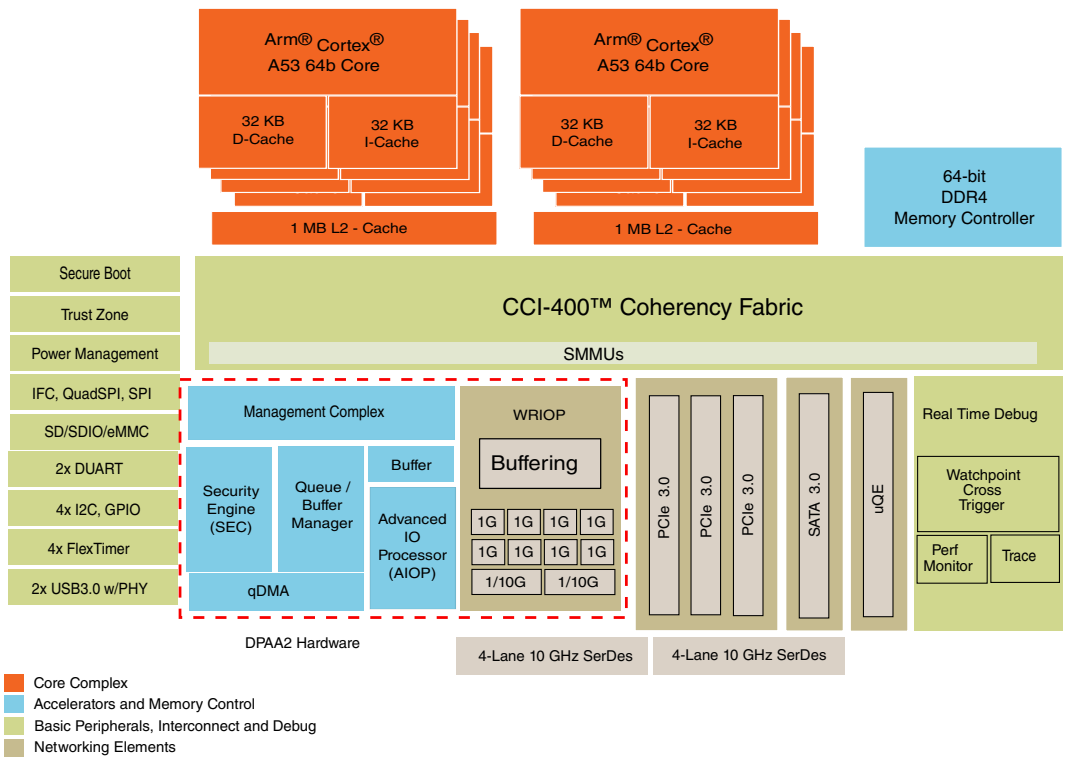


Figure 1. LS1088A block diagram

2 Pin assignments

NOTE: Information given in this section is preliminary and is subject to change.

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ26	Data	L24	IO	$G1V_{DD}$	---
D1_MDQ27	Data	M24	IO	$G1V_{DD}$	---
D1_MDQ28	Data	J22	IO	$G1V_{DD}$	---
D1_MDQ29	Data	H23	IO	$G1V_{DD}$	---
D1_MDQ30	Data	K24	IO	$G1V_{DD}$	---
D1_MDQ31	Data	L25	IO	$G1V_{DD}$	---
D1_MDQ32	Data	V24	IO	$G1V_{DD}$	---
D1_MDQ33	Data	U26	IO	$G1V_{DD}$	---
D1_MDQ34	Data	AA26	IO	$G1V_{DD}$	---
D1_MDQ35	Data	W23	IO	$G1V_{DD}$	---
D1_MDQ36	Data	U24	IO	$G1V_{DD}$	---
D1_MDQ37	Data	U25	IO	$G1V_{DD}$	---
D1_MDQ38	Data	W24	IO	$G1V_{DD}$	---
D1_MDQ39	Data	Y25	IO	$G1V_{DD}$	---
D1_MDQ40	Data	AB24	IO	$G1V_{DD}$	---
D1_MDQ41	Data	AB25	IO	$G1V_{DD}$	---
D1_MDQ42	Data	AE25	IO	$G1V_{DD}$	---
D1_MDQ43	Data	AF25	IO	$G1V_{DD}$	---
D1_MDQ44	Data	Y24	IO	$G1V_{DD}$	---
D1_MDQ45	Data	AA25	IO	$G1V_{DD}$	---
D1_MDQ46	Data	AD25	IO	$G1V_{DD}$	---
D1_MDQ47	Data	AE26	IO	$G1V_{DD}$	---
D1_MDQ48	Data	AA22	IO	$G1V_{DD}$	---
D1_MDQ49	Data	AB23	IO	$G1V_{DD}$	---
D1_MDQ50	Data	AC22	IO	$G1V_{DD}$	---
D1_MDQ51	Data	AB22	IO	$G1V_{DD}$	---
D1_MDQ52	Data	Y22	IO	$G1V_{DD}$	---
D1_MDQ53	Data	AA23	IO	$G1V_{DD}$	---
D1_MDQ54	Data	AD22	IO	$G1V_{DD}$	---
D1_MDQ55	Data	AE22	IO	$G1V_{DD}$	---
D1_MDQ56	Data	AH25	IO	$G1V_{DD}$	---
D1_MDQ57	Data	AF24	IO	$G1V_{DD}$	---
D1_MDQ58	Data	AG22	IO	$G1V_{DD}$	---
D1_MDQ59	Data	AF22	IO	$G1V_{DD}$	---
D1_MDQ60	Data	AH26	IO	$G1V_{DD}$	---
D1_MDQ61	Data	AG25	IO	$G1V_{DD}$	---
D1_MDQ62	Data	AF23	IO	$G1V_{DD}$	---
D1_MDQ63	Data	AH22	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD2_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AE13	I	SV_{DD}	---
SD2_REF_CLK1_P	SerDes PLL 1 Reference Clock	AD13	I	SV_{DD}	---
SD2_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AB19	I	SV_{DD}	---
SD2_REF_CLK2_P	SerDes PLL 2 Reference Clock	AB18	I	SV_{DD}	---
SD2_RX0_N	SerDes Receive Data (negative)	AH15	I	SV_{DD}	---
SD2_RX0_P	SerDes Receive Data (positive)	AG15	I	SV_{DD}	---
SD2_RX1_N	SerDes Receive Data (negative)	AH16	I	SV_{DD}	---
SD2_RX1_P	SerDes Receive Data (positive)	AG16	I	SV_{DD}	---
SD2_RX2_N	SerDes Receive Data (negative)	AH18	I	SV_{DD}	---
SD2_RX2_P	SerDes Receive Data (positive)	AG18	I	SV_{DD}	---
SD2_RX3_N	SerDes Receive Data (negative)	AH19	I	SV_{DD}	---
SD2_RX3_P	SerDes Receive Data (positive)	AG19	I	SV_{DD}	---
SD2_TX0_N	SerDes Transmit Data (negative)	AE15	O	XV_{DD}	---
SD2_TX0_P	SerDes Transmit Data (positive)	AD15	O	XV_{DD}	---
SD2_TX1_N	SerDes Transmit Data (negative)	AE16	O	XV_{DD}	---
SD2_TX1_P	SerDes Transmit Data (positive)	AD16	O	XV_{DD}	---
SD2_TX2_N	SerDes Transmit Data (negative)	AE18	O	XV_{DD}	---
SD2_TX2_P	SerDes Transmit Data (positive)	AD18	O	XV_{DD}	---
SD2_TX3_N	SerDes Transmit Data (negative)	AE19	O	XV_{DD}	---
SD2_TX3_P	SerDes Transmit Data (positive)	AD19	O	XV_{DD}	---
USB PHY 1					
USB1_D_M	USB PHY HS Data (-)	E6	IO	-	---
USB1_D_P	USB PHY HS Data (+)	F6	IO	-	---
USB1_ID	USB PHY ID Detect	F5	I	-	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO1_05/**IFC_AD05**/ cfg_gpinput5	General Purpose Input/Output	B9	O	OV_{DD}	1, 4
GPIO1_06/**IFC_AD06**/ cfg_gpinput6	General Purpose Input/Output	A8	O	OV_{DD}	1, 4
GPIO1_07/**IFC_AD07**/ cfg_gpinput7	General Purpose Input/Output	B8	O	OV_{DD}	1, 4
GPIO1_08/**IFC_AD08**/ cfg_rcw_src1	General Purpose Input/Output	A12	O	OV_{DD}	1, 4
GPIO1_09/**IFC_AD09**/ cfg_rcw_src2	General Purpose Input/Output	A13	O	OV_{DD}	1, 4
GPIO1_10/**IFC_AD10**/ cfg_rcw_src3	General Purpose Input/Output	B14	O	OV_{DD}	1, 4
GPIO1_11/**IFC_AD11**/ cfg_rcw_src4	General Purpose Input/Output	A14	O	OV_{DD}	1, 4
GPIO1_12/**IFC_AD12**/ cfg_rcw_src5	General Purpose Input/Output	B15	O	OV_{DD}	1, 4
GPIO1_13/**IFC_AD13**/ cfg_rcw_src6	General Purpose Input/Output	A15	O	OV_{DD}	1, 4
GPIO1_14/**IFC_AD14**/ cfg_rcw_src7	General Purpose Input/Output	A16	O	OV_{DD}	1, 4
GPIO1_15/**IFC_AD15**/ cfg_rcw_src8	General Purpose Input/Output	A17	O	OV_{DD}	1, 4
GPIO1_16/**IFC_A00**/ QSPI_A_CS0	General Purpose Input/Output	D8	O	OV_{DD}	1, 5
GPIO1_17/**IFC_A01**/ QSPI_A_CS1	General Purpose Input/Output	C8	O	OV_{DD}	1, 5
GPIO1_18/**IFC_A02**/ QSPI_A_SCK	General Purpose Input/Output	C9	O	OV_{DD}	1, 5
GPIO1_19/**IFC_A03**/ QSPI_B_CS0	General Purpose Input/Output	D10	O	OV_{DD}	1, 5
GPIO1_20/**IFC_A04**/ QSPI_B_CS1	General Purpose Input/Output	C10	O	OV_{DD}	1, 5
GPIO1_21/**IFC_A05**/ QSPI_B_SCK/cfg_dram_type	General Purpose Input/Output	C11	O	OV_{DD}	1, 4
GPIO1_22/**IFC_WE0_B**/ cfg_eng_use0	General Purpose Input/Output	C15	O	OV_{DD}	1, 4, 19
GPIO1_23/**IFC_TE**/cfg_ifc_te	General Purpose Input/Output	E14	O	OV_{DD}	1, 4
GPIO1_24/**IFC_ALE**	General Purpose Input/Output	A18	O	OV_{DD}	1, 5
GPIO1_25/**IFC_CLE**/ cfg_rcw_src0	General Purpose Input/Output	C19	O	OV_{DD}	1, 4
GPIO1_26/**IFC_OE_B**/ cfg_eng_use1	General Purpose Input/Output	C18	O	OV_{DD}	1, 5
GPIO1_27/**IFC_WP0_B**/ cfg_eng_use2	General Purpose Input/Output	D19	O	OV_{DD}	1, 5

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND075	Core, Platform and PLL Ground	L6	---	---	---
GND076	Core, Platform and PLL Ground	L10	---	---	---
GND077	Core, Platform and PLL Ground	L12	---	---	---
GND078	Core, Platform and PLL Ground	L14	---	---	---
GND079	Core, Platform and PLL Ground	L16	---	---	---
GND080	Core, Platform and PLL Ground	L18	---	---	---
GND081	Core, Platform and PLL Ground	L20	---	---	---
GND082	Core, Platform and PLL Ground	L23	---	---	---
GND083	Core, Platform and PLL Ground	L26	---	---	---
GND084	Core, Platform and PLL Ground	M6	---	---	---
GND085	Core, Platform and PLL Ground	M9	---	---	---
GND086	Core, Platform and PLL Ground	M11	---	---	---
GND087	Core, Platform and PLL Ground	M13	---	---	---
GND088	Core, Platform and PLL Ground	M15	---	---	---
GND089	Core, Platform and PLL Ground	M17	---	---	---
GND090	Core, Platform and PLL Ground	M19	---	---	---
GND091	Core, Platform and PLL Ground	M21	---	---	---
GND092	Core, Platform and PLL Ground	M23	---	---	---
GND093	Core, Platform and PLL Ground	N2	---	---	---
GND094	Core, Platform and PLL Ground	N4	---	---	---
GND095	Core, Platform and PLL Ground	N6	---	---	---
GND096	Core, Platform and PLL Ground	N8	---	---	---

Table continues on the next page...

NOTE

If using Trust Architecture Security Monity battery backed features, prior to V_{DD} or SV_{DD} ramping up to 0.5 V level, ensure that OV_{DD} is properly ramped to at least 90% and SYSCLK or DIFF_SYSCLK / DIFF_SYSCLK_B is running. The clock should have a minimum frequency of 800 Hz and a maximum frequency no greater that the supported system clock frequency for the device.

Warning

Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

This figure shows the SV_{DD} and V_{DD} ramp-up diagram.

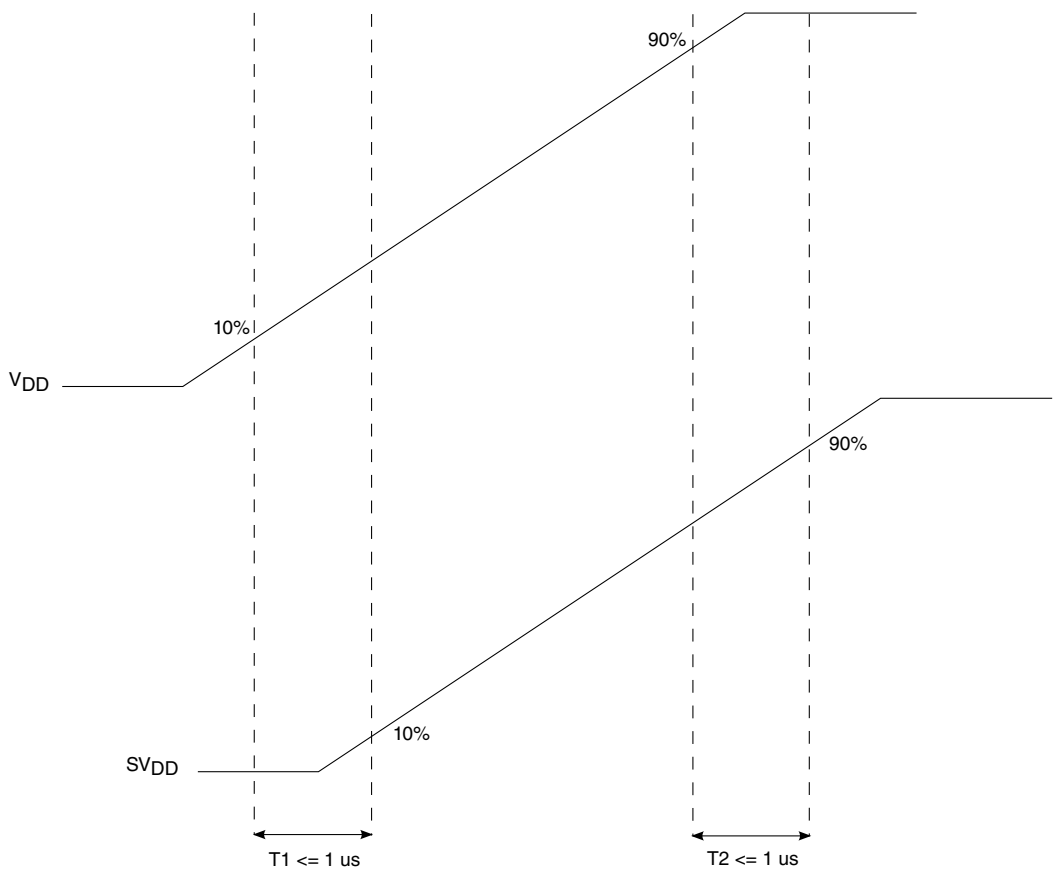


Figure 8. SV_{DD} and V_{DD} ramp-up diagram

For secure boot fuse programming, use the following steps:

1. After negation of PORESET_B, drive TA_PROG_SFP = 1.80 V after a required minimum delay per Table 6.

3.9 Battery-backed security monitor interface

This section describes the DC and AC electrical characteristics for the battery-backed security monitor interface, which includes TA_BB_TMP_DETECT_B.

3.9.1 Battery-backed security monitor interface DC electrical characteristics

This table provides the DC electrical characteristics for the battery-backed security monitor interface operating at 1.0 V ($TA\_BB\_V_{DD}$).

Table 23. Battery-backed security monitor interface DC electrical characteristics ($TA\_BB\_V_{DD}$ = 1.0 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $TA\_BB\_V_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.3 x $TA\_BB\_V_{DD}$	V	1
Input current (V_{IN} = 0 V or V_{IN} = $TA\_BB\_V_{DD}$)	I_{IN}	—	±50	μA	2

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max $TA\_BB\_V_{DD}$ values found in Table 3.
2. The symbol V_{IN}, in this case, represents the $TA\_BB\_V_{DD}$ symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

This table provides the DC electrical characteristics for the battery-backed security monitor interface operating at 0.9 V ($TA\_BB\_V_{DD}$).

Table 24. Battery-backed security monitor interface DC electrical characteristics ($TA\_BB\_V_{DD}$ = 0.9 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $TA\_BB\_V_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.3 x $TA\_BB\_V_{DD}$	V	1
Input current (V_{IN} = 0 V or V_{IN} = $TA\_BB\_V_{DD}$)	I_{IN}	—	±50	μA	2

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max $TA\_BB\_V_{DD}$ values found in Table 3.
2. The symbol V_{IN}, in this case, represents the $TA\_BB\_V_{DD}$ symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

Table 26. DDR4 SDRAM interface DC electrical characteristics (GV_{DD} = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
6. Internal Vref for data bus must be set to 0.7 x GV_{DD}.					
7. For recommended operating conditions, see Table 3.					

3.10.2 DDR4 SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR4 memories. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.10.2.1 DDR4 SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 27. DDR4 SDRAM interface input AC timing specifications (GV_{DD} = 1.2 V ± 5%)$_1$

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage ≤ 2133 MT/s data rate	V_{ILAC}	—	0.7 x GV_{DD} - 0.175	V	—
AC input high voltage ≤ 2133 MT/s data rate	V_{IHAC}	0.7 x GV_{DD} + 0.175	—	V	—
Note: 1. For recommended operating conditions, see Table 3.					

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 28. DDR4 SDRAM interface input AC timing specifications (GV_{DD} = 1.2 V ± 5% for DDR4)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS-MDQ/MECC	t_{CISKEW}	—	—	ps	1
2100 MT/s data rate		-80	80		
1800 MT/s data rate		-93	93		
1600 MT/s data rate		-112	112		
1333 MT/s data rate		-125	125		
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}	—	—	ps	2
2100 MT/s data rate		-154	154		
1800 MT/s data rate		-175	175		

Table continues on the next page...

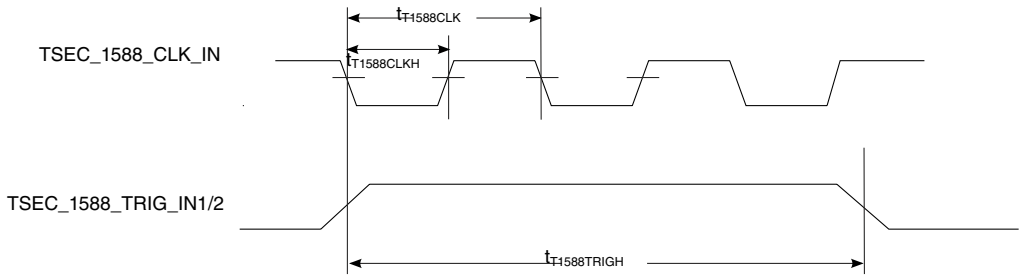


Figure 26. IEEE 1588 input AC timing

3.13.3 RGMII interface

This section describes the DC and AC electrical characteristics for the RGMII interface.

3.13.3.1 RGMII DC electrical characteristics

This table provides the DC electrical characteristics for the RGMII interfaces operating at $LV_{DD}/L1V_{DD}$ = 2.5 V.

Table 49. RGMII DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x LVDD	V	2
Input current (V_{IN}=0V or V_{IN}=LV_{DD})	I_{IN}	-50.0	50.0	µA	3, 4
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.0	-	V	3
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	-	0.4	V	3
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.					
3. The symbol LV_{DD} represents the input voltage of the supply referenced in Table 3.					
4. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the RGMII interface operating at LV_{DD} = 1.8 V.

Table 50. RGMII DC electrical characteristics (LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	V	2
Input low voltage	V_{IL}	-	0.3 x LVDD	V	2

Table continues on the next page...

Table 56. GPIO DC electrical characteristics (O/LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN}/LV_{IN} values found in Table 3.					
3. The symbol OV_{IN}/LV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at O/LV_{DD} = 1.8 V.

Table 57. GPIO DC electrical characteristics (TV_{DD} = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TVDD	-	-	2
Input low voltage	V_{IL}	-	0.2 x TVDD	-	2
Output low current (V_{OL} = 0.2 V)	I_{OL}	4.0	-	mA	-
Output high voltage (TV_{DD} = min, I_{OH} = -100 µA)	V_{OH}	1.0	-	V	3
Output low voltage (TV_{DD} = min, I_{OL} = 100 µA)	V_{OL}	-	0.2	V	3
Input capacitance	C_{IN}	-	10.0	pF	-
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3.					
3. The symbol TV_{DD} represents the input voltage of the supply referenced in Table 3.					

3.14.2 GPIO AC timing specifications

This table provides the AC timing specifications for the GPIO interface.

Table 58. GPIO AC timing specifications

Parameter	Symbol	Min	Unit	Notes
GPIO inputs-minimum pulse width	t_{PIWID}	20.0	ns	GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure shows the AC test load for the GPIO interface.

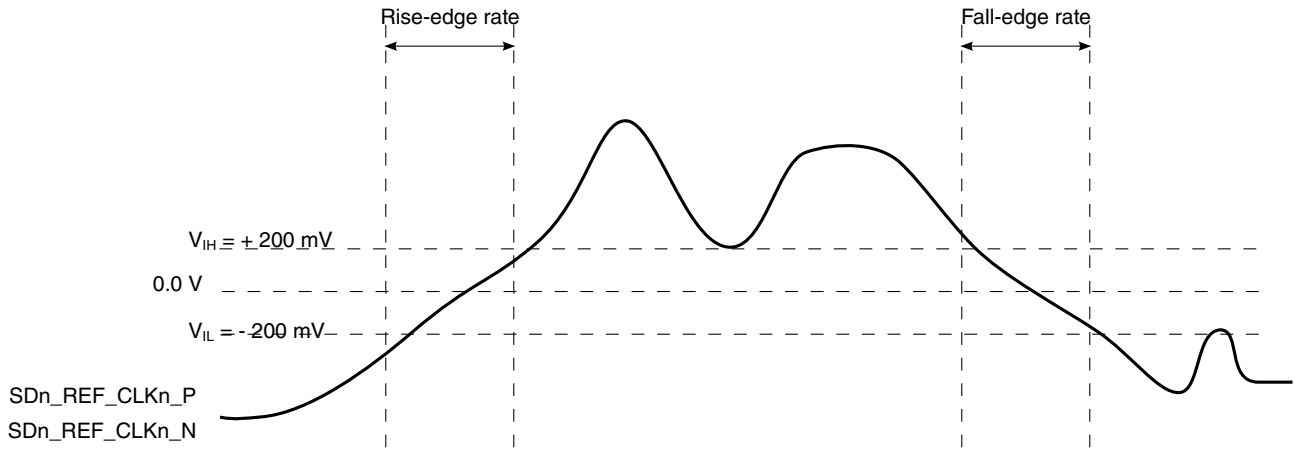


Figure 34. Differential measurement points for rise and fall time

This figure shows the single-ended measurement points for rise and fall time matching.

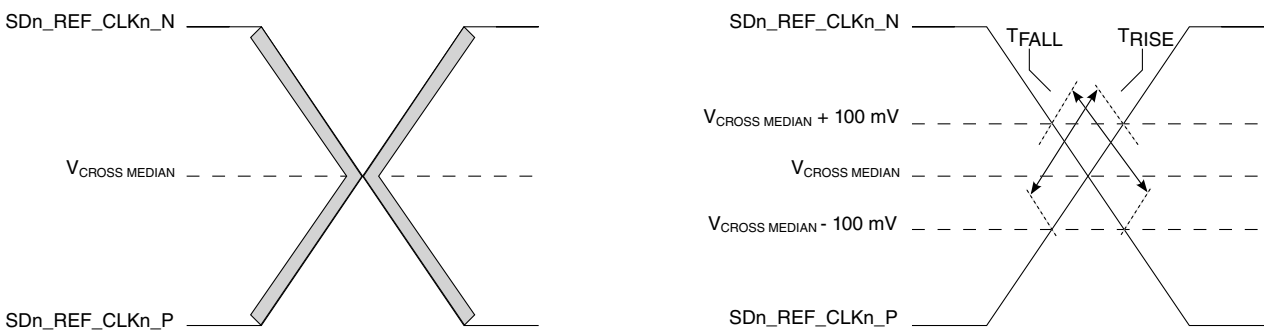


Figure 35. Single-ended measurement points for rise and fall time matching

3.16.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

Figure 36. SerDes transmitter and receiver reference circuits

The DC and AC specifications of the SerDes data lanes are defined in each interface protocol section below based on the application usage:

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 87. Gen 2i/2m 3 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.
2. For recommended operating conditions, see Table 3.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 3i transmission. The AC timing specifications do not include RefClk jitter.

Table 88. Gen 3i transmitter AC specifications

Parameter	Symbol	Min	Typ	Max	Units
Speed	—	—	6.0	—	Gb/s
Total jitter before and after compliance interconnect channel	J_T	—	—	0.52	UI p-p
Random jitter before compliance interconnect channel	J_R	—	—	0.18	UI p-p
Unit interval	UI	166.6083	166.6667	167.5583	ps

3.16.5.2.3 AC differential receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 89. Gen 1i/1m 1.5 G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_RXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_RXTJ250UI}$	—	—	0.60	UI p-p	1

Table continues on the next page...

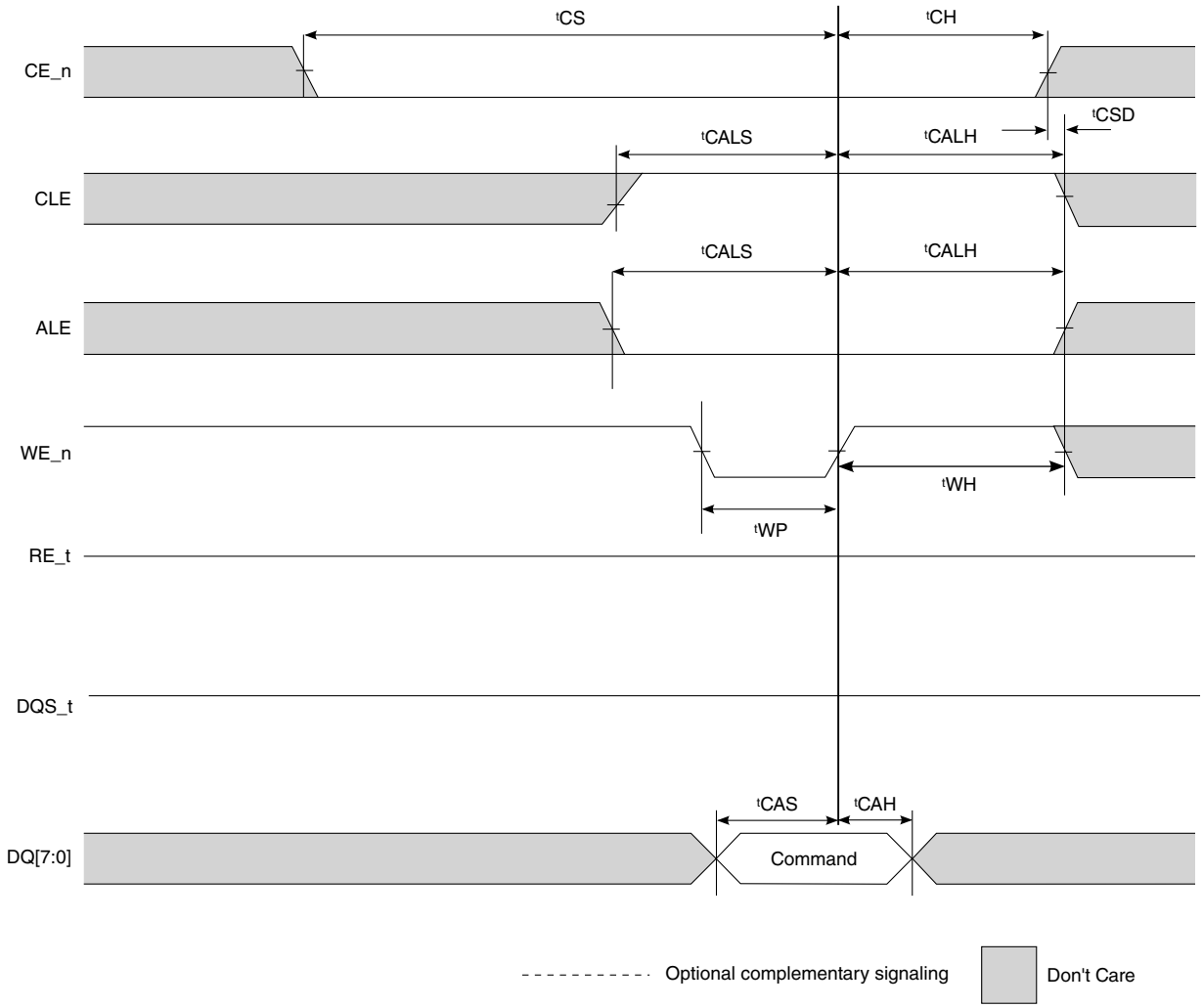


Figure 55. Command cycle

This figure shows the t_{AR} timings.

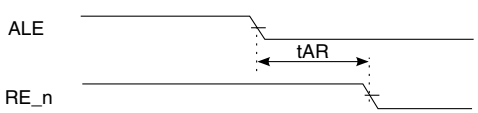


Figure 56. t_{AR} timings

This figure shows the data input cycle timings.

Table 126. JTAG DC electrical characteristics (OV_{DD} = 1.8 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. For recommended operating conditions, see Table 3.					
2. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in the Recommended Operating Conditions table.					
3. Note that the symbol V_{IN}, in this case, represents the OVIN symbol found in the Recommended Operating Conditions table.					
4. TDI, TMS, and TRST_B have internal pull-ups per the IEEE Std. 1149.1 specification.					

3.19.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 78, Figure 79, Figure 80, and Figure 81.

Table 127. JTAG AC timing specifications[1]

Parameter	Symbol	Min	Max	Unit	Notes
JTAG external clock frequency of operation	F_{JTG}	0.0	33.3	MHz	-
JTAG external clock cycle time	t_{JTG}	30.0	-	ns	-
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15.0	-	ns	-
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0.0	2.0	ns	-
TRST_B assert time	t_{TRST}	25.0	-	ns	TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.
Input setup times	t_{JTDVKH}	4.0	-	ns	TA_BB_TMP_DETECT pin requires 13.5ns input setup time for the board JTAG test to go through runTESTIdle.
Input hold times	t_{JTDXKH}	10.0	-	ns	-
Output valid times: boundary-scan data	t_{JTKLDV}	-	15.0	ns	All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
Output valid times: TDO	t_{JTKLDV}	-	10.0	ns	All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in

Table continues on the next page...

This figure shows the QuadSPI clock input timing diagram.

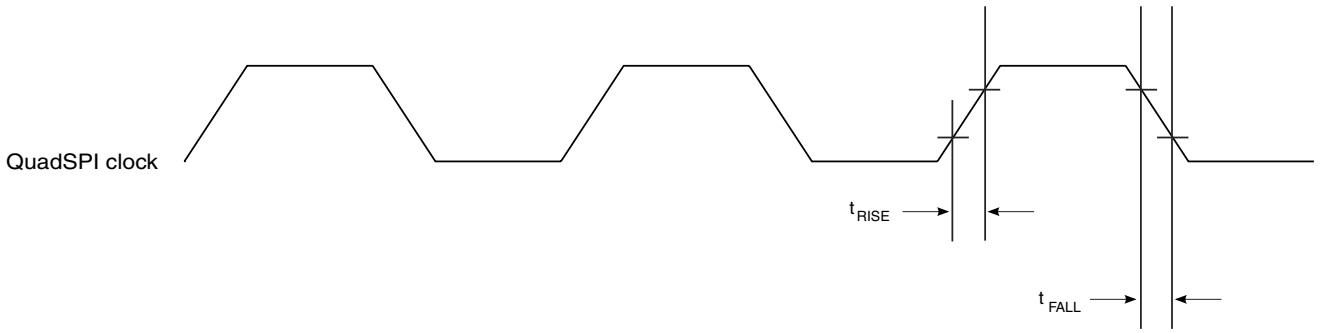


Figure 85. QuadSPI clock input timing diagram

This figure shows the AC test load for QuadSPI.

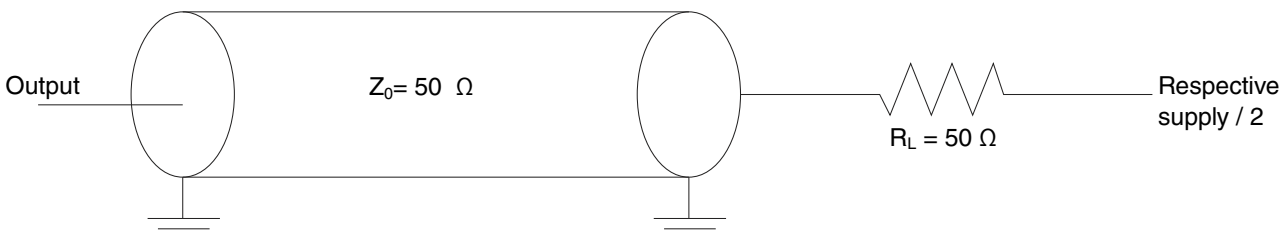


Figure 86. AC test load for QuadSPI

3.21 QUICC engine specifications

The rise/fall time on QUICC engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD}. Fall time refers to transitions from 90% to 10% of V_{DD}.

3.21.1 High-level data link control (HDLC) interface

This section describes the DC and AC electrical characteristics for the high-level data link control (HDLC) interface.

3.21.1.1 HDLC DC electrical characteristics

This table provides the DC electrical characteristics for the HDLC and synchronous UART protocols when operating at DV_{DD} = 3.3 V.

Table 134. HDLC AC timing specifications

Parameter	Symbol	Min	Max	Unit
Internal clock delay	t_{HIKHOV}	0.0	5.5	-
External clock delay	t_{HEKHOV}	1.0	13.0	ns
Internal clock high impedance	t_{HIKHOX}	0.0	5.5	ns
External clock high impedance	t_{HEKHOX}	1.0	8.0	ns
Internal clock input setup time	t_{HIIVKH}	12.6	-	ns
External clock input setup time	t_{HEIVKH}	4.0	-	ns
Internal clock input hold time	t_{HIIXKH}	0.0	-	ns
External clock input hold time	t_{HEIXKH}	1.0	-	ns

This table provides the input and output AC timing specifications for the synchronous UART protocols.

Table 135. Synchronous UART AC timing specifications

Parameter	Symbol	Min	Max	Unit
Internal clock delay	t_{HIKHOV}	0.0	11.0	-
External clock delay	t_{HEKHOV}	1.0	14.0	ns
Internal clock high impedance	t_{HIKHOX}	0.0	11.0	ns
External clock high impedance	t_{HEKHOX}	1.0	14.0	ns
Internal clock input setup time	t_{HIIVKH}	10.0	-	ns
External clock input setup time	t_{HEIVKH}	8.0	-	ns
Internal clock input hold time	t_{HIIXKH}	0.0	-	ns
External clock input hold time	t_{HEIXKH}	1.0	-	ns

This figure shows the AC test load for the HDLC interface.

Table 140. SPI AC timing specifications (continued)

Parameter	Symbol	Min	Condition	Max	Unit
Data valid (after SCK edge) for outputs	t_{NEKHOV}	-	Slave	7.6	ns
Data hold time for outputs	t_{NIKHOX}	0.0	Master	-	ns
Data hold time for outputs	t_{NEKHOX}	0.0	Slave	-	ns

This figure shows the SPI timing master when CPHA = 0.

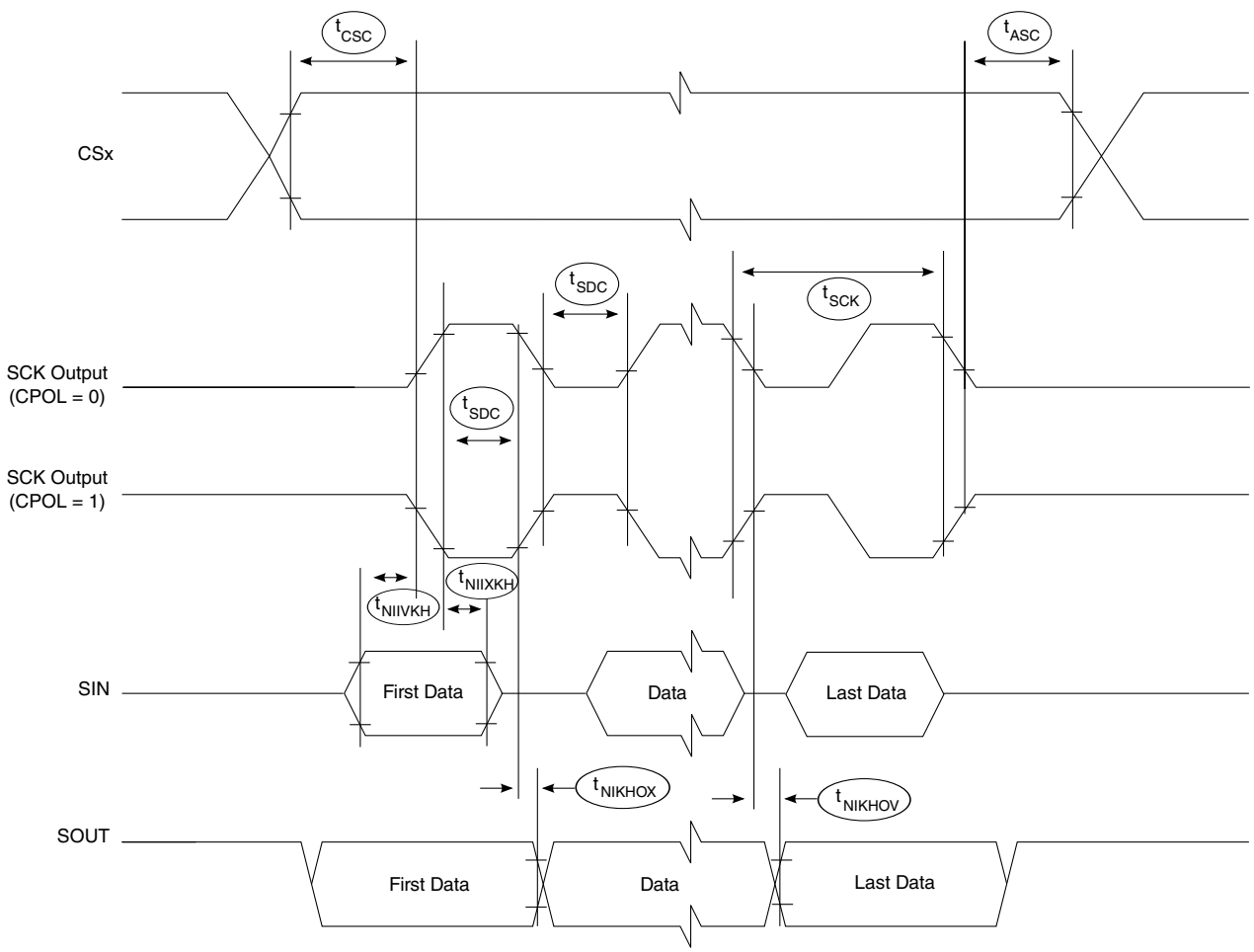


Figure 92. SPI timing master, CPHA = 0

This figure shows the SPI timing master when CPHA = 1.

The table below lists the valid VID fuse values that will be programmed at the factory for this chip.

Table 148. Fuse Status Register (DCFG_CCSR_FUSESR)

Binary value of DA_V / DA_ALT_V	V_{DD} voltage
00000b	1.025 V (default)
00001b	0.9875 V
00010b	0.9750 V
01000b	0.9000 V
10000b	1.0000 V
10001b	1.0125 V
10010b	1.0250 V
All other values	Reserved

For additional information on VID, see the chip reference manual.

5 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 149. Package thermal characteristics

Rating	Board	Symbol	Value	Unit	Notes
Junction-to-ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	23.5	°C/W	1
Junction-to-ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	15.2	°C/W	1
Junction-to-ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	14.8	°C/W	1
Junction-to-ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	10.1	°C/W	1
Junction-to-board	-	$R_{\Theta JB}$	4.4	°C/W	2
Junction-to-case (top)	-	$R_{\Theta JCtop}$	0.56	°C/W	3
Junction-to-lid-top	-	$R_{\Theta JClid}$	0.20	°C/W	4

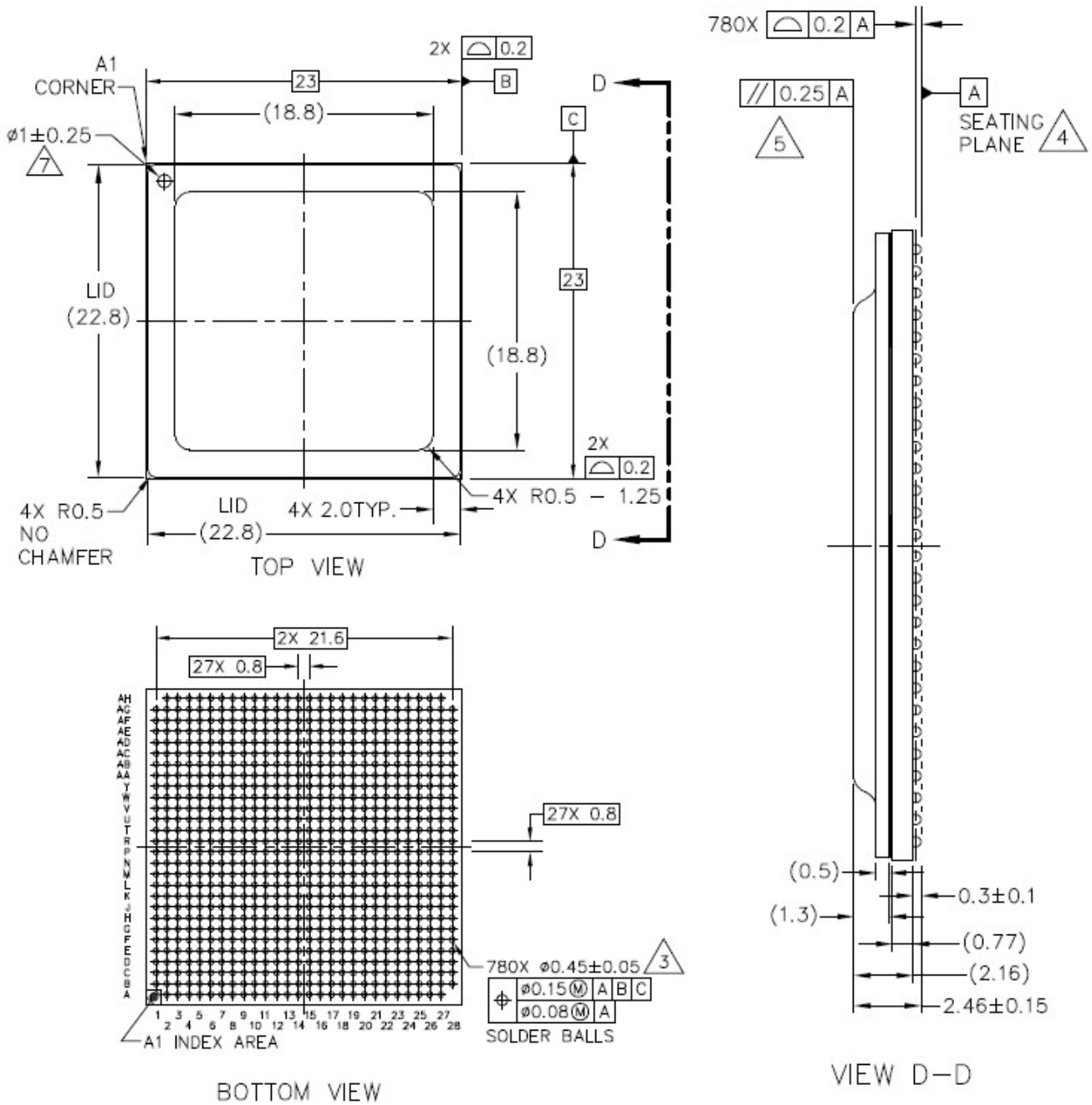
1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-2A and JESD51-6. Thermal test board meets JEDEC specification for this package (JESD51-9).

2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4. Junction-to-lid-top thermal resistance is determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance layer between the package and cold plate.

5. See Thermal management information for additional details.



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	STANDARD: NON–JEDEC	
	03 DEC 2014	

Figure 97. Mechanical dimensions of the FC-PBGA