Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

|	
Product Status	Active
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	8 Core, 64-Bit
Speed	1.4GHz
Co-Processors/DSP	-
RAM Controllers	DDR4
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	10GbE (2), 1GbE (8)
SATA	SATA 6Gbps (1)
USB	USB 3.0 (2) + PHY
Voltage - I/O	-
Operating Temperature	0°C ~ 105°C
Security Features	Secure Boot, TrustZone®
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088ase7pta
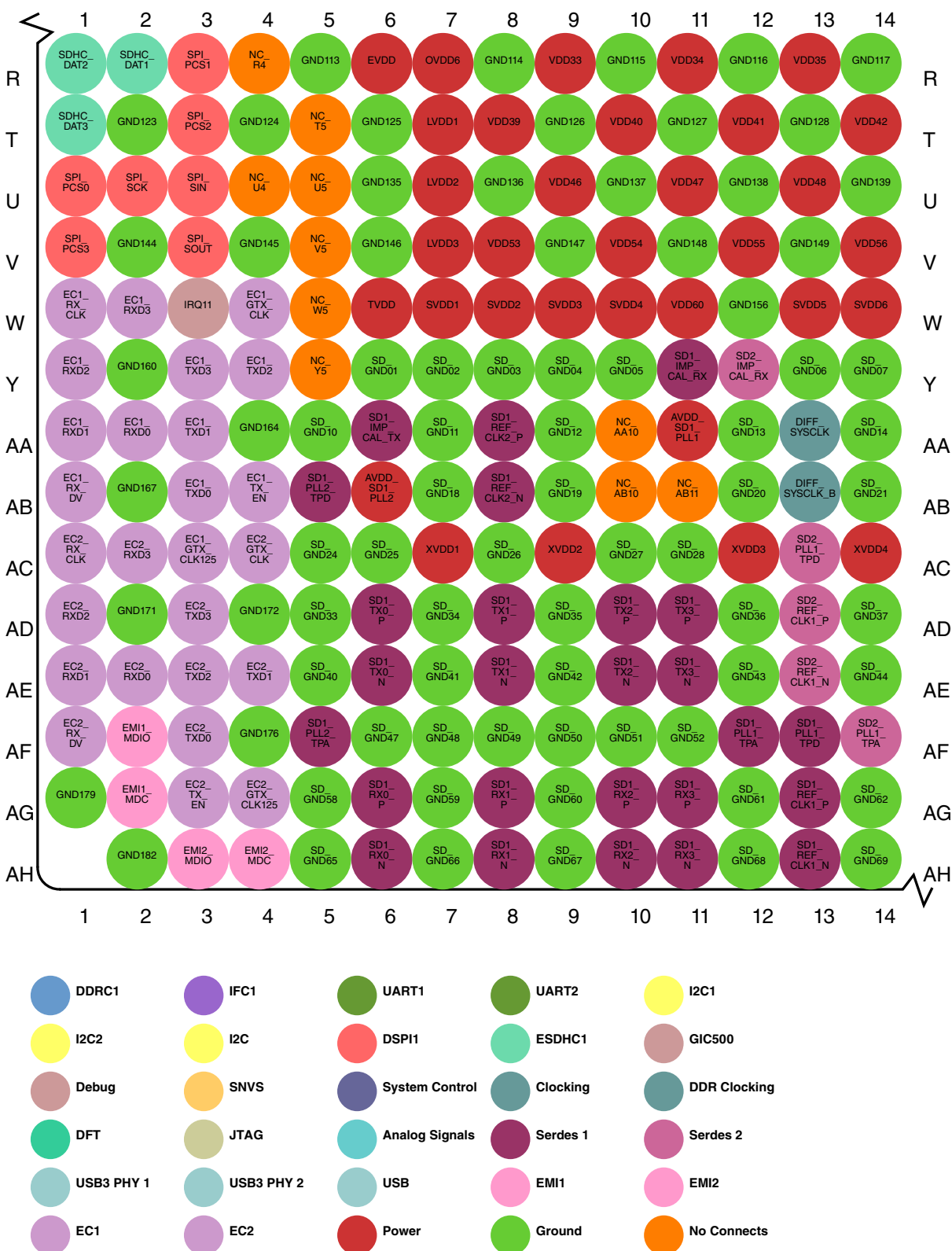
Figure 5. Detail C

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC1_RXD2/GPIO2_30	Receive Data	Y1	I	LV$_{DD}$	1
EC1_RXD3/GPIO2_29	Receive Data	W2	I	LV$_{DD}$	1
EC1_RX_CLK/GPIO4_13	Receive Clock	W1	I	LV$_{DD}$	1
EC1_RX_DV/GPIO4_14	Receive Data Valid	AB1	I	LV$_{DD}$	1
EC1_TXD0/GPIO2_25	Transmit Data	AB3	O	LV$_{DD}$	1
EC1_TXD1/GPIO2_24	Transmit Data	AA3	O	LV$_{DD}$	1
EC1_TXD2/GPIO2_23	Transmit Data	Y4	O	LV$_{DD}$	1
EC1_TXD3/GPIO2_22	Transmit Data	Y3	O	LV$_{DD}$	1
EC1_TX_EN/GPIO2_26	Transmit Enable	AB4	O	LV$_{DD}$	1, 14
Ethernet Controller 2					
EC2_GTX_CLK/GPIO4_20	Transmit Clock Out	AC4	O	LV$_{DD}$	1
EC2_GTX_CLK125/GPIO4_21	Reference Clock	AG4	I	LV$_{DD}$	1
EC2_RXD0/GPIO4_25/ TSEC_1588_TRIG_IN2	Receive Data	AE2	I	LV$_{DD}$	1
EC2_RXD1/GPIO4_24/ TSEC_1588_PULSE_OUT1	Receive Data	AE1	I	LV$_{DD}$	1
EC2_RXD2/GPIO4_23	Receive Data	AD1	I	LV$_{DD}$	1
EC2_RXD3/GPIO4_22	Receive Data	AC2	I	LV$_{DD}$	1
EC2_RX_CLK/GPIO4_26/ TSEC_1588_CLK_IN	Receive Clock	AC1	I	LV$_{DD}$	1
EC2_RX_DV/GPIO4_27/ TSEC_1588_TRIG_IN1	Receive Data Valid	AF1	I	LV$_{DD}$	1
EC2_TXD0/GPIO4_18/ TSEC_1588_PULSE_OUT2	Transmit Data	AF3	O	LV$_{DD}$	1
EC2_TXD1/GPIO4_17/ TSEC_1588_CLK_OUT	Transmit Data	AE4	O	LV$_{DD}$	1
EC2_TXD2/GPIO4_16/ TSEC_1588_ALARM_OUT1	Transmit Data	AE3	O	LV$_{DD}$	1
EC2_TXD3/GPIO4_15/ TSEC_1588_ALARM_OUT2	Transmit Data	AD3	O	LV$_{DD}$	1
EC2_TX_EN/GPIO4_19	Transmit Enable	AG3	O	LV$_{DD}$	1, 14
General Purpose Input/Output					
GPIO1_00/**IFC_AD00**/ cfg_gpinput0	General Purpose Input/Output	B12	O	OV$_{DD}$	1, 4
GPIO1_01/**IFC_AD01**/ cfg_gpinput1	General Purpose Input/Output	A11	O	OV$_{DD}$	1, 4
GPIO1_02/**IFC_AD02**/ cfg_gpinput2	General Purpose Input/Output	B11	O	OV$_{DD}$	1, 4
GPIO1_03/**IFC_AD03**/ cfg_gpinput3	General Purpose Input/Output	A10	O	OV$_{DD}$	1, 4
GPIO1_04/**IFC_AD04**/ cfg_gpinput4	General Purpose Input/Output	A9	O	OV$_{DD}$	1, 4

Table continues on the next page...

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Table 1.   Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
cfg_gpinput7/**IFC_AD07**/ GPIO1_07	Power-on-Reset Configuration	B8	I	OV$_{DD}$	1, 4
cfg_ifc_te/**IFC_TE**/GPIO1_23	Power-on-Reset Configuration	E14	I	OV$_{DD}$	1, 4
cfg_rcw_src0/**IFC_CLE**/ GPIO1_25	Power-on-Reset Configuration	C19	I	OV$_{DD}$	1, 4
cfg_rcw_src1/**IFC_AD08**/ GPIO1_08	Power-on-Reset Configuration	A12	I	OV$_{DD}$	1, 4
cfg_rcw_src2/**IFC_AD09**/ GPIO1_09	Power-on-Reset Configuration	A13	I	OV$_{DD}$	1, 4
cfg_rcw_src3/**IFC_AD10**/ GPIO1_10	Power-on-Reset Configuration	B14	I	OV$_{DD}$	1, 4
cfg_rcw_src4/**IFC_AD11**/ GPIO1_11	Power-on-Reset Configuration	A14	I	OV$_{DD}$	1, 4
cfg_rcw_src5/**IFC_AD12**/ GPIO1_12	Power-on-Reset Configuration	B15	I	OV$_{DD}$	1, 4
cfg_rcw_src6/**IFC_AD13**/ GPIO1_13	Power-on-Reset Configuration	A15	I	OV$_{DD}$	1, 4
cfg_rcw_src7/**IFC_AD14**/ GPIO1_14	Power-on-Reset Configuration	A16	I	OV$_{DD}$	1, 4
cfg_rcw_src8/**IFC_AD15**/ GPIO1_15	Power-on-Reset Configuration	A17	I	OV$_{DD}$	1, 4
Quad SPI					
QSPI_A_CS0/**IFC_A00**/ GPIO1_16	Chip Select	D8	O	OV$_{DD}$	1, 5
QSPI_A_CS1/**IFC_A01**/ GPIO1_17	CS1	C8	O	OV$_{DD}$	1, 5
QSPI_A_DATA0/**IFC_A06**/ GPIO2_00/IFC_WP1_B	DATA0	D11	IO	OV$_{DD}$	---
QSPI_A_DATA1/**IFC_A07**/ GPIO2_01/IFC_WP2_B	DATA1	C12	IO	OV$_{DD}$	---
QSPI_A_DATA2/**IFC_A08**/ GPIO2_02/IFC_WP3_B	DATA2	D13	IO	OV$_{DD}$	---
QSPI_A_DATA3/**IFC_A09**/ GPIO2_03/IFC_RB2_B/ IFC_CS_B4	DATA3	C13	IO	OV$_{DD}$	---
QSPI_A_DATA4/**IFC_PAR0**/ GPIO2_06/QSPI_B_DATA0	DATA4	B18	IO	OV$_{DD}$	---
QSPI_A_DATA5/**IFC_PAR1**/ GPIO2_07/QSPI_B_DATA1	DATA5	D17	IO	OV$_{DD}$	---
QSPI_A_DATA6/ **IFC_PERR_B**/GPIO2_16/ QSPI_B_DATA2	DATA6	E17	IO	OV$_{DD}$	---
QSPI_A_DATA7/**IFC_CS3_B**/ GPIO2_11/QSPI_B_DATA3	DATA7	C20	IO	OV$_{DD}$	---

Table continues on the next page...

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Table 1.   Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UC1_CTSB_RXDV/**IRQ05**/ GPIO3_29/TDMA_RSYNC	Receive Data	J5	I	DV$_{DD}$	1
UC1_RTSB_TXEN/**IRQ07**/ GPIO4_05/TDMA_TSYNC	Transmit Enable	L5	O	DV$_{DD}$	1
UC1_RXD7/**IRQ04**/GPIO3_28/ TDMA_RXD/TDMA_TXD	Receive Data	J4	I	DV$_{DD}$	1
UC1_TXD7/**IRQ06**/GPIO4_04/ TDMA_RXD_EXC/TDMA_TXD	Transmit Data	K5	O	DV$_{DD}$	1
UC3_CDB_RXER/**IIC4_SDA**/ GPIO4_31/EVT8_B/TDMB_RQ	Receive Error	N3	I	DV$_{DD}$	1
UC3_CTSB_RXDV/**IRQ09**/ GPIO4_07/TDMB_RSYNC	Receive Data	N5	I	DV$_{DD}$	1
UC3_RTSB_TXEN/**IRQ03**/ GPIO3_27/TDMB_TSYNC	Transmit Enable	J3	O	DV$_{DD}$	1
UC3_RXD7/**IRQ08**/GPIO4_06/ TDMB_RXD/TDMB_TXD	Receive Data	M5	I	DV$_{DD}$	1
UC3_TXD7/**IRQ10**/GPIO4_08/ TDMB_RXD_EXC/TDMB_TXD	Transmit Data	P4	O	DV$_{DD}$	1
Time Division Multiplexing					
TDMA_RSYNC/**IRQ05**/ GPIO3_29/UC1_CTSB_RXDV	RSYNC	J5	I	DV$_{DD}$	1
TDMA_RXD/**IRQ04**/ GPIO3_28/UC1_RXD7/ TDMA_TXD	RXD	J4	I	DV$_{DD}$	1
TDMA_RXD_EXC/**IRQ06**/ GPIO4_04/TDMA_TXD/ UC1_TXD7	Recieve Data	K5	I	DV$_{DD}$	1
TDMA_TSYNC/**IRQ07**/ GPIO4_05/UC1_RTSB_TXEN	TSYNC	L5	I	DV$_{DD}$	1
TDMA_TXD/**IRQ04**/GPIO3_28/ TDMA_RXD/UC1_RXD7	Transmit Data	J4	O	DV$_{DD}$	1
TDMA_TXD/**IRQ06**/GPIO4_04/ TDMA_RXD_EXC/UC1_TXD7	Transmit Data	K5	O	DV$_{DD}$	1
TDMB_RSYNC/**IRQ09**/ GPIO4_07/UC3_CTSB_RXDV	RSYNC	N5	I	DV$_{DD}$	1
TDMB_RXD/**IRQ08**/ GPIO4_06/UC3_RXD7/ TDMB_TXD	RXD	M5	I	DV$_{DD}$	1
TDMB_RXD_EXC/**IRQ10**/ GPIO4_08/TDMB_TXD/ UC3_TXD7	Recieve Data	P4	I	DV$_{DD}$	1
TDMB_TSYNC/**IRQ03**/ GPIO3_27/UC3_RTSB_TXEN	TSYNC	J3	I	DV$_{DD}$	1
TDMB_TXD/**IRQ08**/GPIO4_06/ TDMB_RXD/UC3_RXD7	Transmit Data	M5	O	DV$_{DD}$	1

Table continues on the next page...

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Table 3. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended value	Unit	Notes
USB PHY analog and digital HS supply		USB_SDV_{DD}	1.0 + 50 mV / - 30 mV	V	7, 9
			0.9 V + 50 mV / - 30 mV	V	7, 9
USB PHY analog and digital SS supply		USB_SV_{DD}	1.0 + 50 mV / - 30 mV	V	8, 9
			0.9 V + 50 mV / - 30 mV	V	8, 9
Input voltage	DDR4 DRAM signals	MV_{IN}	GND to $G1V_{DD}$	V	—
	Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)	LV_{IN}	GND to LV_{DD}	V	—
	IFC, SPI, GIC (IRQ 0/1/2), Tamper_Detect, System control and power management, SYSCLK, DDR_CLK, GPIO3, GPIO2, GPIO1, eSDHC[4-7]/VS/ DAT123_DIR/DAT0_DIR/ CMD_DIR/SYNC), Debug, JTAG, RTC, POR signals	OV_{IN}	GND to OV_{DD}	V	—
	DUART1/2, I²C, DMA, QE, GPIO3, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), USB Control (DRVVBUS, PWRFAULT)	DV_{IN}	GND to DV_{DD}	V	—
	eSDHC[0-3]/CLK/CMD, GPIO3	EV_{IN}	GND to EV_{DD}	V	—
	Main power supply for internal circuitry of SerDes and DIFF_SYSCLK	SV_{IN}	GND to SV_{DD}	V	—
	Ethernet management interface 2 (EMI2), GPIO2	TV_{IN}	GND to TV_{DD}	V	—
PHY transceiver signals	USB transceiver supply for USB PHY	USB_HV_{IN}	GND to USB_HV_{DD}	V	6
	Analog and digital SS supply for USB PHY	USB_SDV_{DD}	GND to USB_SDV_{DD}	V	7
	Analog and digital HS supply for USB PHY	USB_SV_{DD}	0.3 to USB_SV_{DD}	V	8
Operating temperature range	Normal operation	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—
	Extended temperature	T_A, T_J	T_A = -40 (min) to T_J = 105 (max)	°C	—
	Secure boot fuse programming	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	2

Notes:

1. RGMII is supported at 2.5 V or 1.8 V.

2. TA_PROG_SFP must be supplied 1.8 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming, subject to the power sequencing constraints shown in Power sequencing. For all other operating conditions, TA_PROG_SFP must be tied to GND.

3. For additional information, see the Core and platform supply voltage filtering section in the chip design checklist.

interface uses differential receivers referenced by the internally generated MVREF signal. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

NOTE
These values are preliminary estimates.

Table 4. Output drive capability

Driver type	Output impedance (Ω)			Supply Voltage	Notes
	Minimum[2]	Typical	Maximum[3]		
DDR4 signal	-	18 (full-strength mode) 27 (half-strength mode)	-	$G1V_{DD}$ = 1.2 V	1
Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)	30	50	70	LV_{DD} = 2.5 V	-
	30	45	60	LV_{DD} = 1.8 V	-
MDC of Ethernet management interface 2 (EMI 2)	45	65	100	TV_{DD} = 1.2 V	-
	40	55	75	TV_{DD} = 1.8 V	-
	40	60	90	TV_{DD} = 2.5 V	-
MDIO of Ethernet management interface 2 (EMI 2)	30	40	60	TV_{DD} = 1.2 V	-
	25	33	44	TV_{DD} = 1.8 V	-
	25	40	57	TV_{DD} = 2.5 V	-
IFC, SPI, GIC (IRQ 0/1/2), Tamper_Detect, System control and power management, DDR_CLK, GPIO1, GPIO2, GPIO3, eSDHC[4-7]/VS/DAT123_DIR/DAT0_DIR/ CMD_DIR/SYNC), Debug, JTAG, RTC, POR signals	30	45	60	OV_{DD} = 1.8 V	-
DUART1/2, I²C, DMA, QE, GPIO3, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), USB control (DRVVBUS, PWRFAULT)	45	65	90	DV_{DD} = 3.3 V	-
	40	55	75	DV_{DD} = 1.8 V	
eSDHC[0-3]/CLK/CMD, GPIO3	45	65	90	EV_{DD} = 3.3 V	-
	40	55	75	EV_{DD} = 1.8 V	

1. The drive strength of the DDR4 interface in half-strength mode is at T_j = 105°C and at $G1V_{DD}$ (min).

2. Estimated number based on best case processed device.

3. Estimated number based on worst case processed device.

3.7.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content.

The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement.

Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in this table are observed.

Table 14. Spread-spectrum clock source recommendations[3]

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Notes:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 13.

2. Maximum spread-spectrum frequency may not result in exceeding any maximum operating frequency of the device.

3. At recommended operating conditions with OVDD = 1.8 V. See Table 3.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded, regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should use only down-spreading to avoid violating the stated limits.

3.7.3 USB 3.0 reference clock requirements

There are two options for the reference clock of USB PHY: SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B. This table provides the additional requirements when SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B is used as USB REFCLK. The 100 MHz reference clock is also required with the following requirements.

3.9.2 Battery-backed security monitor interface AC timing specifications

This table provides the AC timing specifications for the battery-backed security monitor interface.

Table 25. Battery-backed security monitor interface AC timing specifications[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
TA_BB_TMP_DETECT_B	t_{TMP}	100			ns	1
Notes:						
1. TA_BB_TMP_DETECT_B is asynchronous to any clock.						
2. For recommended operating conditions, see Table 3.						

3.10 DDR4 SDRAM controller

This section describes the DC and AC electrical specifications for the DDR4 SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.10.1 DDR4 SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR4 SDRAM.

Table 26. DDR4 SDRAM interface DC electrical characteristics (GV_{DD} = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input low	V_{IL}	—	0.7 x GV_{DD} - 0.175	V	3, 6
Input high	V_{IH}	0.7 x GV_{DD} + 0.175	—	V	3, 6
I/O leakage current	I_{OZ}	-165	165	µA	5
Notes:					
1. GV_{DD} is expected to be within 60 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.					
2. V_{TT} and VREFCA are applied directly to the DRAM device. Both V_{TT} and VREFCA voltages must track GV_{DD}/2.					
3. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.					
4. See the IBIS model for the complete output IV curve characteristics.					
5. Output leakage is measured with all outputs disabled, 0V ≤ V_{OUT} ≤ GV_{DD}. Made internal per Mazyar's updates in DDR4 spec v2.					

This includes PCI Express (2.5, 5, and 8 GT/s), SGMII (1.25 Gbaud), 2.5 x SGMII (3.125 Gbaud), QSGMII (5 Gbps), and SATA (1.5, 3.0, and 6.0 Gbps). SerDes reference clocks need to be verified by the customer's application design.

Table 65. SDn_REF_CLKn_P and SDn_REF_CLKn_N input clock requirements (SV$_{DD}$ = 0.9V/ 1.0 V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SDn_REF_CLKn_P/ SDn_REF_CLKn_N frequency range	t$_{CLK\_REF}$	—	100/125/156.25	—	MHz	2
SDn_REF_CLKn_P/ SDn_REF_CLKn_N clock frequency tolerance	t$_{CLK\_TOL}$	-300	—	300	ppm	3
SDn_REF_CLKn_P/ SDn_REF_CLKn_N clock frequency tolerance	t$_{CLK\_TOL}$	-100	—	100	ppm	4
SDn_REF_CLKn_P/ SDn_REF_CLKn_N reference clock duty cycle	t$_{CLK\_DUTY}$	40	50	60	%	5
SDn_REF_CLKn_P/ SDn_REF_CLKn_N max deterministic peak-to-peak jitter at 10^{-6} BER	t$_{CLK\_DJ}$	—	—	42	ps	—
SDn_REF_CLKn_P/ SDn_REF_CLKn_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t$_{CLK\_TJ}$	—	—	86	ps	6
SDn_REF_CLKn_P/ SDn_REF_CLKn_N 10 kHz to 1.5 MHz RMS jitter	t$_{REFCLK-LF-RMS}$	—	—	3	ps RMS	7
SDn_REF_CLKn_P/ SDn_REF_CLKn_N > 1.5 MHz to Nyquist RMS jitter	t$_{REFCLK-HF-RMS}$	—	—	3.1	ps RMS	7
RMS reference clock jitter	t$_{REFCLK-RMS-DC}$	—	—	1	ps RMS	8
SDn_REF_CLKn_P/ SDn_REF_CLKn_N rising/ falling edge rate	t$_{CLKRR}$/t$_{CLKFR}$	1	—	4	V/ns	9
Differential input high voltage	V$_{IH}$	200	—	—	mV	5
Differential input low voltage	V$_{IL}$	—	—	-200	mV	5
Rising edge rate (SDn_REF_CLKn_P) to falling edge rate (SDn_REF_CLKn_N) matching	Rise-Fall Matching	—	—	20	%	10, 11

Notes:

1. For recommended operating conditions, see Table 3.

2. **Caution:** Only 100, 125, and 156.25 have been tested. In-between values do not work correctly with the rest of the system.

3. For PCI Express (2.5, 5 and 8 GT/s).

4. For SGMII, 2.5 x SGMII and QSGMII.

5. Measurement taken from differential waveform.

6. Limits from PCI Express CEM Rev 2.0.

7. For PCI Express 5 GT/s, per PCI Express base specification Rev 3.0.

8. For PCI Express 8 GT/s, per PCI Express base specification Rev. 3.0.

9. Measured from -200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLKn_P minus SDn_REF_CLKn_N). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 34.

10. Measurement taken from single-ended waveform.

Table 70. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (SV$_{DD}$ = 0.9V/1.0 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	Z$_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z$_{RX-DC}$	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	Z$_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	V$_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	V$_{RX-IDLE-DET-DIFFp-p}$ = 2 x |V$_{RX-D+}$ -V$_{RX-D-}$| Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

4. For recommended operating conditions, see Table 3.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 71. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SV$_{DD}$ = 0.9V/1.0 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	V$_{RX-DIFFp-p}$	120	1000	1200	mV	V$_{RX-DIFFp-p}$ = 2 x |V$_{RX-D+}$ - V$_{RX-D-}$| See Note 1.
DC differential input impedance	Z$_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z$_{RX-DC}$	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	Z$_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	V$_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	V$_{RX-IDLE-DET-DIFFp-p}$ = 2 x |V$_{RX-D+}$ - V$_{RX-D-}$| Measured at the package pins of the receiver

Table continues on the next page...

Table 72. PCI Express 3.0 (8 GT/s) differential receiver input DC characteristics (SV$_{DD}$ = 0.9V/1.0 V)[6]

Characteristic	Symbol	Min	Typ	Max	Units	Notes
4. V$_{RX-SV-8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. The "SV" in the parameter names refers to stressed voltage.						
5. V$_{RX-SV-8G}$ is referenced to TP2P and is obtained after post processing data captured at TP2.						
6. For recommended operating conditions, see Table 3.						

3.16.4.4 PCI Express AC physical layer specifications

This section describes the AC specifications for the physical layer of PCI Express on this device.

3.16.4.4.1 PCI Express AC physical layer transmitter specifications

This section describes the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 73. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T$_{TX-EYE}$	0.75	-	-	UI	The maximum transmitter jitter can be derived as T$_{TX-MAX-JITTER}$ = 1 - T$_{TX-EYE}$ = 0.25 UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	T$_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI	Jitter is defined as the measurement variation of the crossing points (V$_{TX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C$_{TX}$	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Table continues on the next page...

Table 92. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
		213.1	333.0	482.9		TECR0[AMP_RED]=0b000110
		186.9	292.0	423.4		TECR0[AMP_RED]=0b000111
		160.0	250.0	362.5		TECR0[AMP_RED]=0b010000
Output impedance (differential)	R_O	80	100	120	Ω	-

Notes:

1. This does not align to DC-coupled SGMII.

2. $\left| V_{OD} \right| = \left| V_{SD\_TXn\_P} - V_{SD\_TXn\_N} \right|$. $\left| V_{OD} \right|$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \times \left| V_{OD} \right|$.

3. The $\left| V_{OD} \right|$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.35 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn _TXn_P and SDn_TXn_N.

4. For recommended operating conditions, see Table 3.

5. Example amplitude reduction setting for SGMII on SerDes1 lane E: SRDS1LN4TECR0[AMP_RED] = 0b000001 for an output differential voltage of 459 mV typical.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

Table 113. 10GBase-KR receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Total jitter tolerance	R_{TJ}	-	-	Per IEEE Std 802.3ap-2007, Annex 69a.	UI p-p
Random jitter	R_{RJ}	-	-	0.13	UI p-p
Sinusoidal jitter (maximum)	R_{SJ-max}	-	-	0.115	UI p-p
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p

3.17 I^{2}C interface

This section describes the DC and AC electrical characteristics for the I^{2}C interface.

3.17.1 I^{2}C DC electrical characteristics

This table provides the DC electrical characteristics for the I^{2}C interface when operating at DV_{DD} = 3.3 V.

Table 114. I^{2}C DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	2
Output low voltage (DV_{DD} = min, IOL = 3 mA, DV_{DD} > 2V)	V_{OL}	-	0.4	V	3
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	4
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} (min) and 0.9 x DV_{DD} (max))	I_I	-50.0	50.0	µA	5
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.

3. The output voltage (open drain or open collector) condition = 3 mA sink current.

4. See the chip reference manual for information about the digital filter used.

5. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.

This table provides the DC electrical characteristics for the I^2C interface operating at DV_{DD} = 1.8 V.

Table 115. I^2C DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x DV_{DD}	V	2
Output low voltage (DV_{DD} = min, IOL = 3 mA, DV_{DD} ≤ 2V)	V_{OL}	0.0	0.36	V	3
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	4
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} (min) and 0.9 x DV_{DD} (max))	I_I	-50.0	50.0	µA	5
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.

3. The output voltage (open drain or open collector) condition = 3 mA sink current.

4. See the chip reference manual for information about the digital filter used.

5. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.

3.17.2 I^2C AC timing specifications

This table provides the AC timing specifications for the I^2C interface.

Table 116. I^2C AC timing specifications[1]

| Parameter	Symbol	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0.0	400.0	kHz	-
Low period of the SCL clock	t_{I2CL}	1.3	-	µs	-
High period of the SCL clock	t_{I2CH}	0.6	-	µs	-
Setup time for a repeated START condition	t_{I2SVKH}	0.6	-	µs	-
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	-	µs	-
Data setup time	t_{I2DVKH}	100.0	-	ns	-
Data input hold time (CBUS compatible masters, I^2C bus devices)	t_{I2DXKL}	0.0	-	µs	As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation

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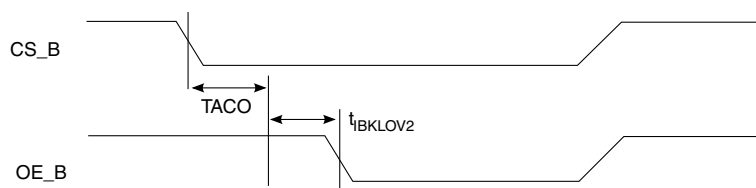
Figure 51. IFC-NOR interface output AC timings

3.18.2.4 IFC AC timing specifications (NAND)

The table below describes the input timing specifications of the IFC-NAND interface.

Table 122. Integrated flash controller input timing specifications for NAND mode (OV$_{DD}$ = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	t$_{IBIVKH3}$	(2 x t$_{IP\_CLK}$) + 2	-	ns	1
Input hold	t$_{IBIXKH3}$	1	-	ns	1
IFC_RB_B pulse width	t$_{IBCH}$	2	-	t$_{IP\_CLK}$	1
NOTE:					
1. t$_{IP\_CLK}$ is the period of ip clock on which IFC is running.					
2. For recommended operating conditions, see Table 3.					

The figure below shows the AC input timing diagram for input signals of IFC-NAND interface. Here TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.
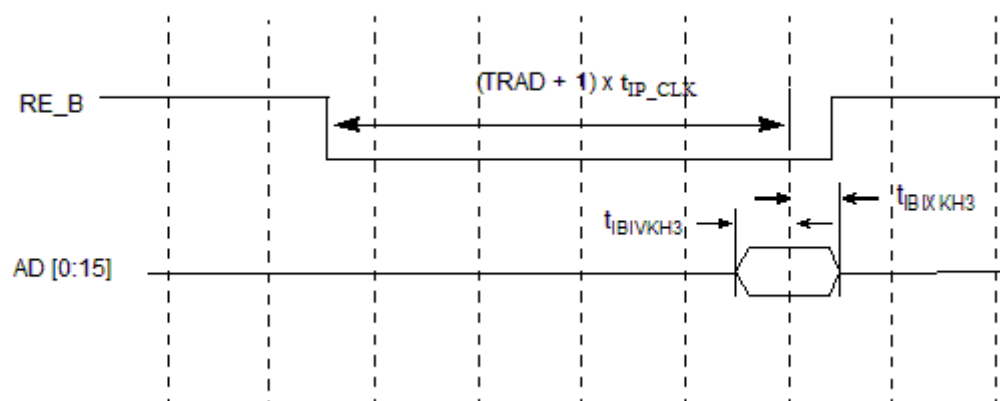
Figure 52. IFC-NAND interface input AC timings

NOTE

t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.

The table below describes the output AC timing specifications for the IFC-NAND interface.

Table 123. Integrated flash controller IFC-NAND interface output timing specifications (OV$_{DD}$ = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV3}$	-	±1.5	ns	1
NOTE:					
1. This effectively means that a signal change may appear anywhere within $t_{IBKLOV3}$ (min) to $t_{IBKLOV3}$ (max) duration, from the point where it's expected to change.					
2. For recommended operating conditions, see Table 3.					

The figure below shows the AC timing diagram for output signals of IFC-NAND interface.The timing specs are shown here by taking the timings between two signals, CS_B and CLE as an example. CLE is supposed to change TCCST (a programmable delay; see the IFC section of the chip reference manual for more information) time after CS_B. Because of the skew between the signals, CLE may change anywhere within window of time defined by $t_{IBKLOV3}$. This concept applies to other output signals of the IFC-NAND interface as well. The diagram is an example to show the skew between any two chronological toggling signals as per the protocol. The list of output signals is as follows: NDWE_B, NDRE_B, NDALE, WP_B, NDCLE, CS_B, AD.
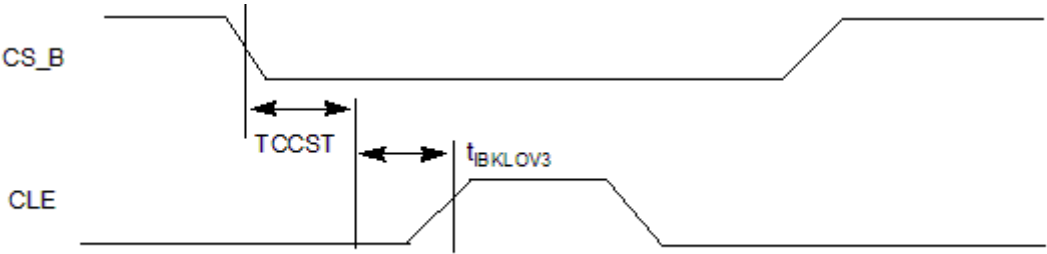

Figure 53. IFC-NAND interface output AC timings

3.18.2.5   IFC-NAND SDR AC timing specifications

This table describes the AC timing specifications for the IFC-NAND SDR interface. These specifications are compliant to the SDR mode of the ONFI specification revision 3.0.

Table 147.   Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency						Unit	Notes
	1200 MHz		1400 MHz		1600 MHz			
	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	600	1200	600	1400	600	1600	MHz	1
Platform clock frequency	400	500	400	600	400	700	MHz	1
Memory bus clock frequency	650	800	650	900	650	1050	MHz	1, 2
IFC clock frequency	-	100	-	100	-	100	MHz	3

1. **Caution:**The coherency domain clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, coherency domain and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock speed is half the DDR4 data rate.

3. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the platform clock divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.

4.2   Power supply design

For additional details on the power supply design, see AN5144, QorIQ LS1088A Design Checklist.

4.2.1   Voltage ID (VID) controllable supply

To guarantee performance and power specifications, a specific method of selecting the optimum voltage-level must be implemented when the chip is used. As part of the chip's boot process, software must read the VID efuse values stored in the Fuse Status register (FUSESR) and then configure the external voltage regulator based on this information. This method requires a point of load voltage regulator for each chip. When VID option is used, the V_{DD} supply should be separated from the SerDes 1.0 V supply SnV_{DD}. It is required in order to control the V_{DD} supply only.

NOTE
During the power-on reset process, the fuse values are read and stored in the FUSESR. It is expected that the chip's boot code reads the FUSESR value very early in the boot sequence and updates the regulator accordingly.

The default voltage regulator setting that is safe for the system to boot is the recommended operating V_{DD} at initial start-up of 1.025 V. It is highly recommended to select a regulator with a Vout range of at least 0.9 V to 1.1 V, with a resolution of 12.5 mV or better, when implementing a VID solution.

5.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

5.2 Temperature diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A). These devices feature series resistance cancellation using three current measurements, where up to 1.5 kΩ of resistance can be automatically cancelled from the temperature result, allowing noise filtering and a more accurate reading.

The following are the specifications of the chip's on-board temperature diode:

Operating range: TBD

Ideality factor TBD; Temperature range TBD

5.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 95. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 15 pounds force.
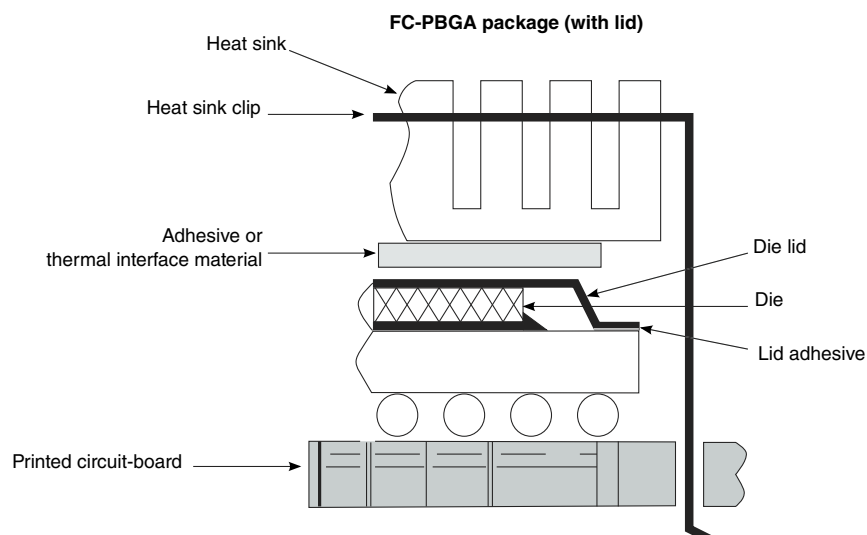
FC-PBGA package (with lid)

Heat sink

Heat sink clip

Adhesive or
thermal interface material

Die lid

Die

Lid adhesive

Printed circuit-board

Figure 95. Package exploded, cross-sectional view-FC-PBGA (with lid)
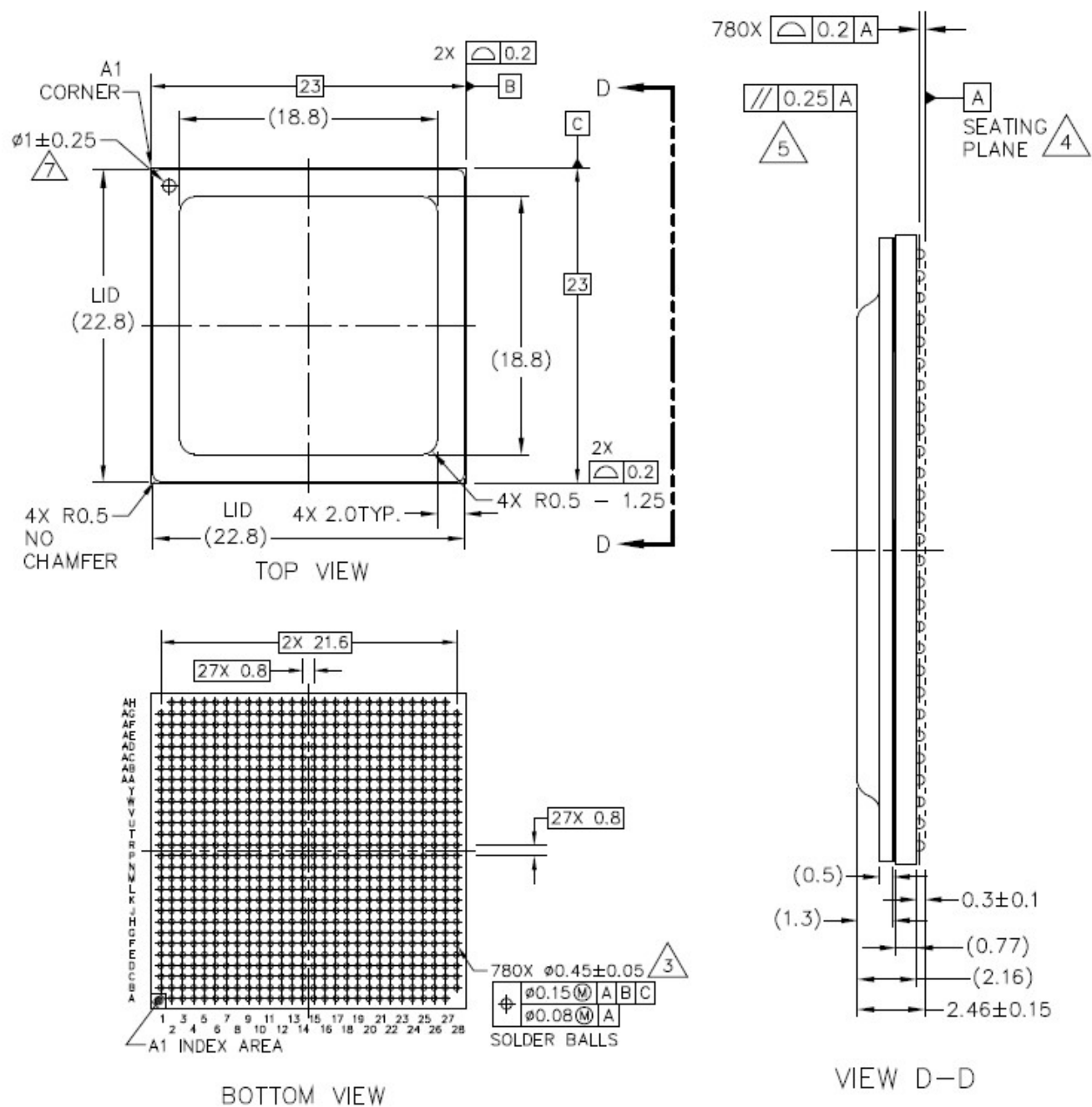
The system board designer can choose between several types of heat sinks to place on the device. There are several commercially available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

5.3.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure shows the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

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Figure 97. Mechanical dimensions of the FC-PBGA