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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	8 Core, 64-Bit
Speed	1.6GHz
Co-Processors/DSP	-
RAM Controllers	DDR4
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	10GbE (2), 1GbE (8)
SATA	SATA 6Gbps (1)
USB	USB 3.0 (2) + PHY
Voltage - I/O	-
Operating Temperature	0°C ~ 105°C
Security Features	Secure Boot, TrustZone®
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088ase7q1a

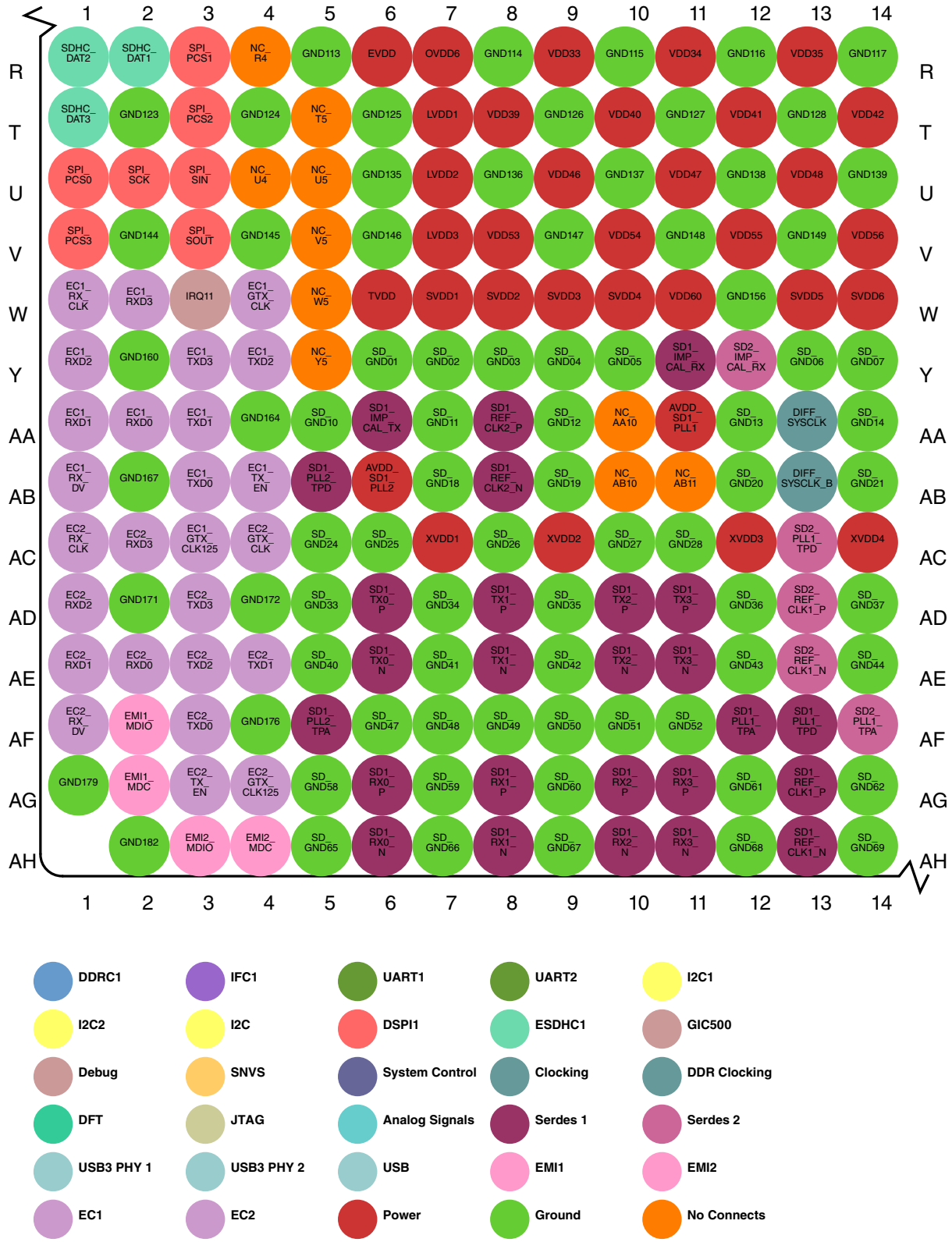


Figure 5. Detail C

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AA8	I	SV_{DD}	---
SD1_RX0_N	SerDes Receive Data (negative)	AH6	I	SV_{DD}	---
SD1_RX0_P	SerDes Receive Data (positive)	AG6	I	SV_{DD}	---
SD1_RX1_N	SerDes Receive Data (negative)	AH8	I	SV_{DD}	---
SD1_RX1_P	SerDes Receive Data (positive)	AG8	I	SV_{DD}	---
SD1_RX2_N	SerDes Receive Data (negative)	AH10	I	SV_{DD}	---
SD1_RX2_P	SerDes Receive Data (positive)	AG10	I	SV_{DD}	---
SD1_RX3_N	SerDes Receive Data (negative)	AH11	I	SV_{DD}	---
SD1_RX3_P	SerDes Receive Data (positive)	AG11	I	SV_{DD}	---
SD1_TX0_N	SerDes Transmit Data (negative)	AE6	O	XV_{DD}	---
SD1_TX0_P	SerDes Transmit Data (positive)	AD6	O	XV_{DD}	---
SD1_TX1_N	SerDes Transmit Data (negative)	AE8	O	XV_{DD}	---
SD1_TX1_P	SerDes Transmit Data (positive)	AD8	O	XV_{DD}	---
SD1_TX2_N	SerDes Transmit Data (negative)	AE10	O	XV_{DD}	---
SD1_TX2_P	SerDes Transmit Data (positive)	AD10	O	XV_{DD}	---
SD1_TX3_N	SerDes Transmit Data (negative)	AE11	O	XV_{DD}	---
SD1_TX3_P	SerDes Transmit Data (positive)	AD11	O	XV_{DD}	---
SerDes 2					
SD2_IMP_CAL_RX	SerDes Receive Impedence Calibration	Y12	I	SV_{DD}	11
SD2_IMP_CAL_TX	SerDes Transmit Impedance Calibration	Y20	I	XV_{DD}	16
SD2_PLL1_TPA	SerDes PLL 1 Test Point Analog	AF14	O	AVDD_SD2_PLL1	12
SD2_PLL1_TPD	SerDes Test Point Digital	AC13	O	XV_{DD}	12
SD2_PLL2_TPA	SerDes PLL 2 Test Point Analog	AF20	O	AVDD_SD2_PLL2	12
SD2_PLL2_TPD	SerDes Test Point Digital	AA20	O	XV_{DD}	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC1_RXD2/GPIO2_30	Receive Data	Y1	I	LV_{DD}	1
EC1_RXD3/GPIO2_29	Receive Data	W2	I	LV_{DD}	1
EC1_RX_CLK/GPIO4_13	Receive Clock	W1	I	LV_{DD}	1
EC1_RX_DV/GPIO4_14	Receive Data Valid	AB1	I	LV_{DD}	1
EC1_TXD0/GPIO2_25	Transmit Data	AB3	O	LV_{DD}	1
EC1_TXD1/GPIO2_24	Transmit Data	AA3	O	LV_{DD}	1
EC1_TXD2/GPIO2_23	Transmit Data	Y4	O	LV_{DD}	1
EC1_TXD3/GPIO2_22	Transmit Data	Y3	O	LV_{DD}	1
EC1_TX_EN/GPIO2_26	Transmit Enable	AB4	O	LV_{DD}	1, 14
Ethernet Controller 2					
EC2_GTX_CLK/GPIO4_20	Transmit Clock Out	AC4	O	LV_{DD}	1
EC2_GTX_CLK125/GPIO4_21	Reference Clock	AG4	I	LV_{DD}	1
EC2_RXD0/GPIO4_25/ TSEC_1588_TRIG_IN2	Receive Data	AE2	I	LV_{DD}	1
EC2_RXD1/GPIO4_24/ TSEC_1588_PULSE_OUT1	Receive Data	AE1	I	LV_{DD}	1
EC2_RXD2/GPIO4_23	Receive Data	AD1	I	LV_{DD}	1
EC2_RXD3/GPIO4_22	Receive Data	AC2	I	LV_{DD}	1
EC2_RX_CLK/GPIO4_26/ TSEC_1588_CLK_IN	Receive Clock	AC1	I	LV_{DD}	1
EC2_RX_DV/GPIO4_27/ TSEC_1588_TRIG_IN1	Receive Data Valid	AF1	I	LV_{DD}	1
EC2_TXD0/GPIO4_18/ TSEC_1588_PULSE_OUT2	Transmit Data	AF3	O	LV_{DD}	1
EC2_TXD1/GPIO4_17/ TSEC_1588_CLK_OUT	Transmit Data	AE4	O	LV_{DD}	1
EC2_TXD2/GPIO4_16/ TSEC_1588_ALARM_OUT1	Transmit Data	AE3	O	LV_{DD}	1
EC2_TXD3/GPIO4_15/ TSEC_1588_ALARM_OUT2	Transmit Data	AD3	O	LV_{DD}	1
EC2_TX_EN/GPIO4_19	Transmit Enable	AG3	O	LV_{DD}	1, 14
General Purpose Input/Output					
GPIO1_00/**IFC_AD00**/ cfg_gpinput0	General Purpose Input/Output	B12	O	OV_{DD}	1, 4
GPIO1_01/**IFC_AD01**/ cfg_gpinput1	General Purpose Input/Output	A11	O	OV_{DD}	1, 4
GPIO1_02/**IFC_AD02**/ cfg_gpinput2	General Purpose Input/Output	B11	O	OV_{DD}	1, 4
GPIO1_03/**IFC_AD03**/ cfg_gpinput3	General Purpose Input/Output	A10	O	OV_{DD}	1, 4
GPIO1_04/**IFC_AD04**/ cfg_gpinput4	General Purpose Input/Output	A9	O	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD15	Supply for cores and platform	M14	---	V_{DD}	---
VDD16	Supply for cores and platform	M16	---	V_{DD}	---
VDD17	Supply for cores and platform	M18	---	V_{DD}	---
VDD18	Supply for cores and platform	M20	---	V_{DD}	---
VDD19	Supply for cores and platform	N9	---	V_{DD}	---
VDD20	Supply for cores and platform	N11	---	V_{DD}	---
VDD21	Supply for cores and platform	N13	---	V_{DD}	---
VDD22	Supply for cores and platform	N15	---	V_{DD}	---
VDD23	Supply for cores and platform	N17	---	V_{DD}	---
VDD24	Supply for cores and platform	N19	---	V_{DD}	---
VDD25	Supply for cores and platform	N21	---	V_{DD}	---
VDD26	Supply for cores and platform	P8	---	V_{DD}	---
VDD27	Supply for cores and platform	P10	---	V_{DD}	---
VDD28	Supply for cores and platform	P12	---	V_{DD}	---
VDD29	Supply for cores and platform	P14	---	V_{DD}	---
VDD30	Supply for cores and platform	P16	---	V_{DD}	---
VDD31	Supply for cores and platform	P18	---	V_{DD}	---
VDD32	Supply for cores and platform	P20	---	V_{DD}	---
VDD33	Supply for cores and platform	R9	---	V_{DD}	---
VDD34	Supply for cores and platform	R11	---	V_{DD}	---
VDD35	Supply for cores and platform	R13	---	V_{DD}	---
VDD36	Supply for cores and platform	R15	---	V_{DD}	---
VDD37	Supply for cores and platform	R17	---	V_{DD}	---
VDD38	Supply for cores and platform	R19	---	V_{DD}	---
VDD39	Supply for cores and platform	T8	---	V_{DD}	---
VDD40	Supply for cores and platform	T10	---	V_{DD}	---
VDD41	Supply for cores and platform	T12	---	V_{DD}	---
VDD42	Supply for cores and platform	T14	---	V_{DD}	---
VDD43	Supply for cores and platform	T16	---	V_{DD}	---
VDD44	Supply for cores and platform	T18	---	V_{DD}	---
VDD45	Supply for cores and platform	T20	---	V_{DD}	---
VDD46	Supply for cores and platform	U9	---	V_{DD}	---
VDD47	Supply for cores and platform	U11	---	V_{DD}	---
VDD48	Supply for cores and platform	U13	---	V_{DD}	---
VDD49	Supply for cores and platform	U15	---	V_{DD}	---
VDD50	Supply for cores and platform	U17	---	V_{DD}	---
VDD51	Supply for cores and platform	U19	---	V_{DD}	---
VDD52	Supply for cores and platform	U21	---	V_{DD}	---

Table continues on the next page...

Table 17. EC*n*_GTX_CLK125 DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 X LV_{DD}	—	—	V	2
Input low voltage	V_{IL}	—	—	0.2 x LV_{DD}	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	—	± 50	μA	3

Notes:

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 3.

This table provides the Ethernet gigabit reference clock AC timing specifications.

Table 18. EC*n*_GTX_CLK125 AC timing specifications [1]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	f_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	—
EC*n*_GTX_CLK125 cycle time	t_{G125}	7.5	8	8.5	ns	—
EC*n*_GTX_CLK125 rise and fall time LV_{DD} = 1.8 V LV_{DD} = 2.5 V	t_{G125R}/t_{G125F}	—	—	 0.54 0.75	ns	2
EC*n*_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	40	—	60	%	3
EC*n*_GTX_CLK125 jitter	—	—	—	± 150	ps	3

Notes:

1. At recommended operating conditions with LV_{DD} = 1.8 V ± 90mV / 2.5 V ± 125 mV. See Table 3.
2. Rise times are measured from 20% of LVDD to 80% of LV_{DD}. Fall times are measured from 80% of LV_{DD} to 20% of LV_{DD}.
3. ECn_GTX_CLK125 is used to generate the GTX clock for the Ethernet transmitter. See RGMII AC timing specifications for duty cycle for the 10Base-T and 100Base-T reference clocks.

3.7.6 DDR clock (DDRCLK)

This section provides the DDRCLK DC electrical characteristics and AC timing specifications.

3.7.6.1 DDRCLK DC electrical characteristics

This table provides the DDRCLK DC electrical characteristics.

Table 28. DDR4 SDRAM interface input AC timing specifications (GV_{DD} = 1.2 V ± 5% for DDR4)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1600 MT/s data rate		-200	200		
1333 MT/s data rate		-250	250		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.

3. For recommended operating conditions, see Table 3.

This figure shows the DDR4 SDRAM interface input timing diagram.

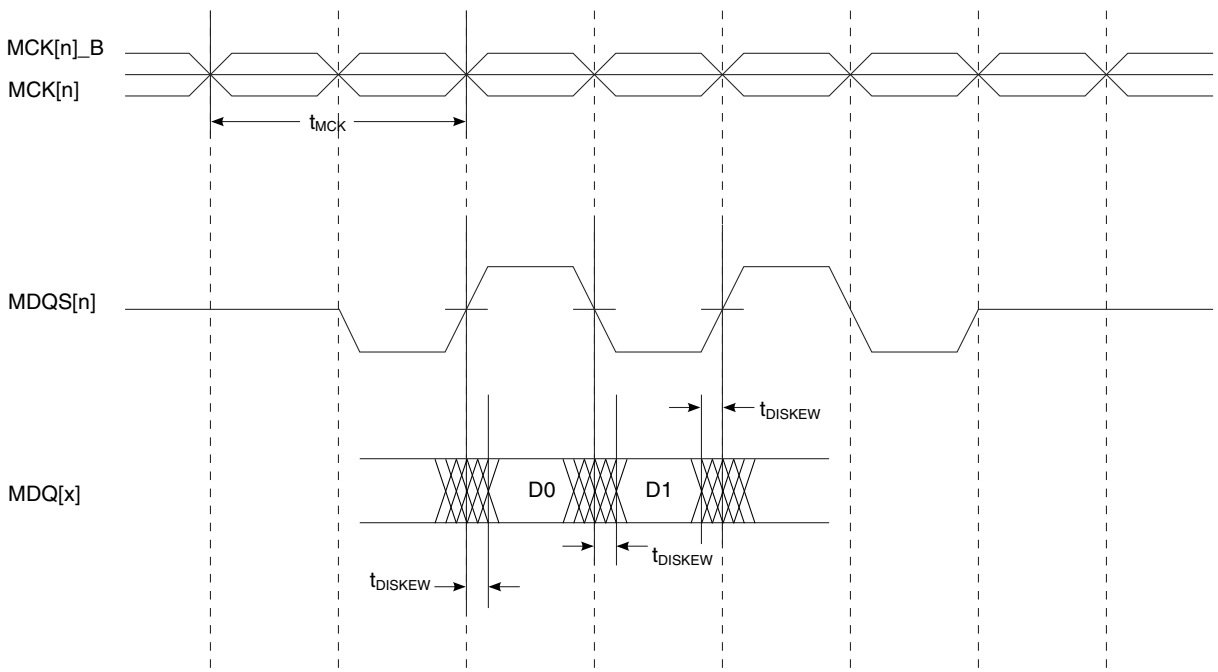


Figure 11. DDR4 SDRAM interface input timing diagram

3.10.2.2 DDR4 SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR4 SDRAM interface.

Table 29. DDR4 SDRAM interface output AC timing specifications (GV_{DD} = 1.2 V)[7]

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	938	1500	ps	2

Table continues on the next page...

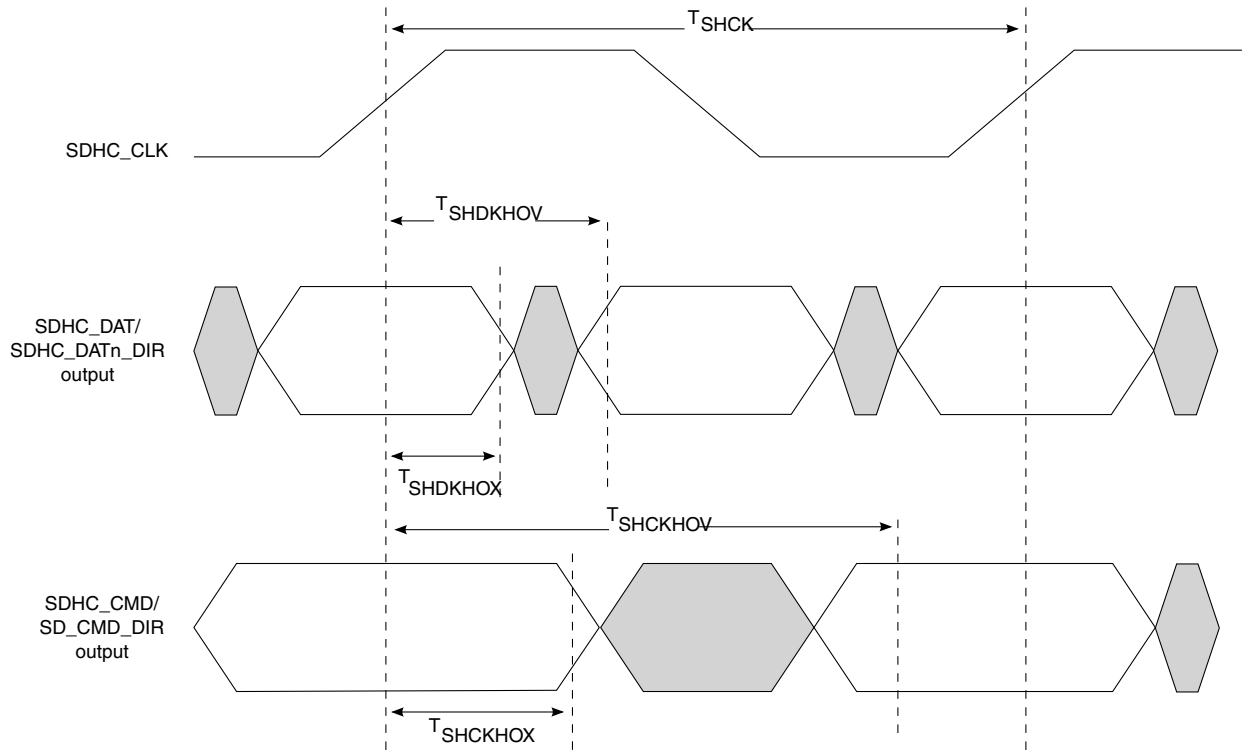


Figure 21. eSDHC DDR50/DDR mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode.

Table 38. eSDHC AC timing specifications (SDR104/eMMC HS200)

Parameter		Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency	SD/SDIO SDR104 mode	f_{SHCK}	-	167	MHz	-
	eMMC HS200 mode			167		-
SDHC_CLK clock rise and fall times		t_{SHCKR}/t_{SHCKF}	-	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOX}	1.58	-	ns	1
	eMMC HS200 mode		1.6			
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOV}	-	3.94	ns	1
	eMMC HS200 mode			3.92		
Input data window (UI)	SD/SDIO SDR104 mode	t_{SHIDV}	0.5	-	Unit Interval	1
	eMMC HS200 mode		0.475			

Notes:

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.
2. For recommended operating conditions, see Table 3.

This figure provides the eSDHC SDR104/HS200 mode timing diagram.

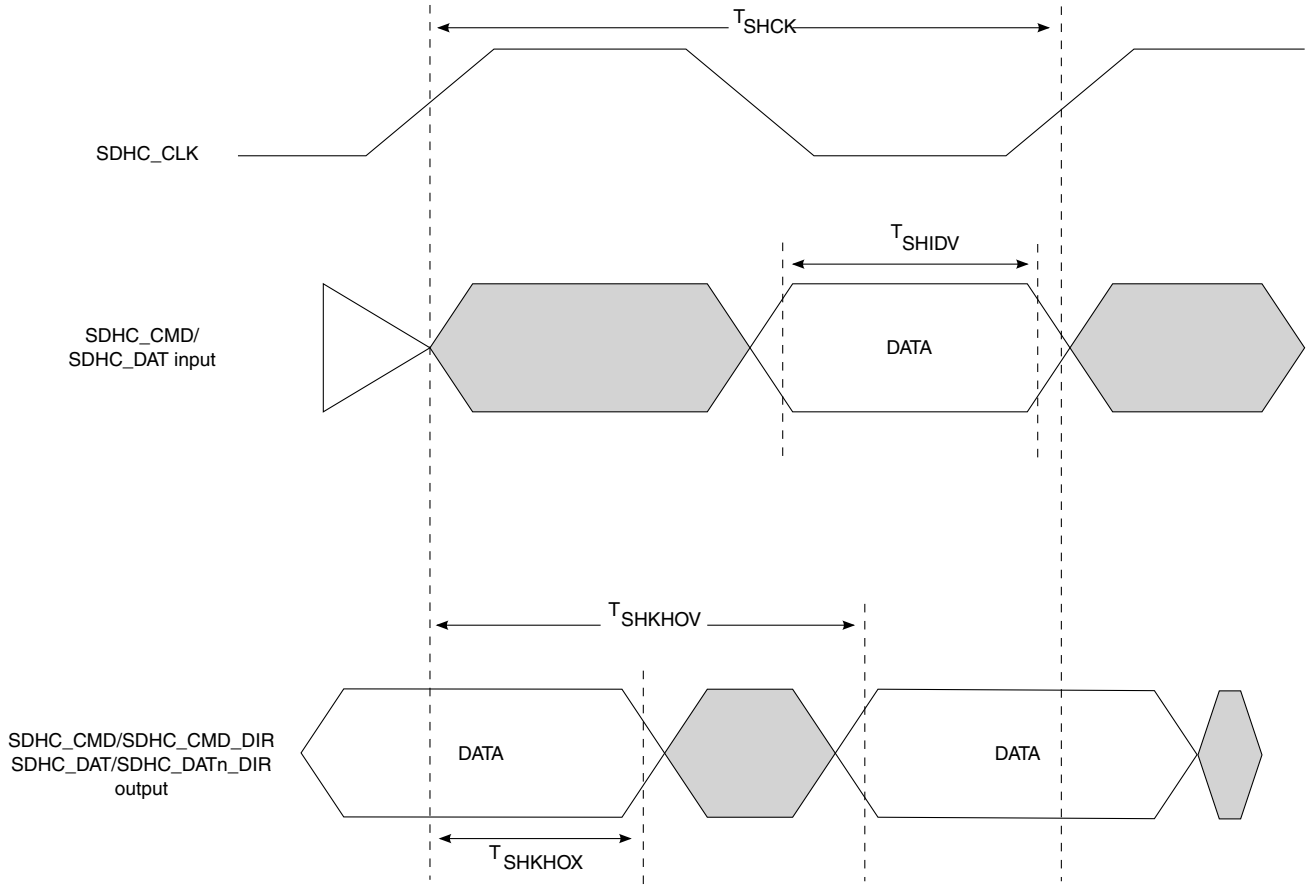


Figure 22. eSDHC SDR104/HS200 mode timing diagram

3.13 Ethernet interface (EMI, RGMII, and IEEE Std 1588™)

This section describes the DC and AC electrical characteristics for the Ethernet controller, Ethernet management, RGMII, and IEEE Std 1588 interfaces.

3.13.1 Ethernet management interface (EMI)

This section describes the electrical characteristics for the Ethernet management interface (EMI).

The EMI1 and EMI2 interface timings are compatible with IEEE Std 802.3™ clauses 22 and 45, respectively.

3.14.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for the GPIO interface operating at D/EV_{DD} = 3.3 V.

Table 52. GPIO DC electrical characteristics (D/EV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/EV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x D/EV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (D/EV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (D/EV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN}/EV_{IN} values found in Table 3. 3. The symbol DV_{IN}/EV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at TV_{DD} = 2.5 V.

Table 53. GPIO DC electrical characteristics (TV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x TV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (TV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (TV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3. 3. The symbol TV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at $D/E/TV_{DD}$ = 1.8 V.

Table 54. GPIO DC electrical characteristics ($D/E/TV_{DD}$ = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $D/E/TV_{DD}$	-	V	2

Table continues on the next page...

- PCI Express
- Serial ATA (SATA) interface
- SGMII interface
- QSGMII interface
- XFI interface

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.16.4 PCI Express

This section describes the clocking dependencies, as well as the DC and AC electrical specifications for the PCI Express bus.

3.16.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.16.4.2 PCI Express clocking requirements for SD2_REF_CLK*n*_P and SD2_REF_CLK*n*_N

SerDes 2 (SD2_REF_CLK[1:2]_P and SD2_REF_CLK[1:2]_N) may be used for various SerDes PCI Express configurations based on the RCW configuration field SRDS_PRTCL. PCI Express is supported on SerDes 2.

For more information on these specifications, see SerDes reference clocks.

3.16.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.16.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 76. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 38 must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

2. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

4. For recommended operating conditions, see Table 3.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 77. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture

Note:

1. For recommended operating conditions, see Table 3.

3.16.6 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 39, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100 Ω output impedance. Each input of the SerDes receiver differential pair features 50 Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 36.

3.16.6.1 SGMII clocking requirements for SDn_REF_CLK1_P and SDn_REF_CLK1_N

When operating in SGMII mode, the EC*n*_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N pins. SerDes lanes may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.16.6.2 SGMII DC electrical characteristics

This section describes the electrical characteristics for the SGMII interface.

3.16.6.2.1 SGMII and SGMII 2.5 G transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N)as shown in Figure 40.

Table 92. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD} \rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD} \rvert_{-min}/2$	-	-	mV	1
Output differential voltage[2, 3, 5] (XV_{DD-Typ} at 1.35 V)	$\lvert V_{OD} \rvert$	320	500.0	725.0	mV	TECR0[AMP_RED]=0b000000
		293.8	459.0	665.6		TECR0[AMP_RED]=0b000001
		266.9	417.0	604.7		TECR0[AMP_RED]=0b000011
		240.6	376.0	545.2		TECR0[AMP_RED]=0b000010

Table continues on the next page...

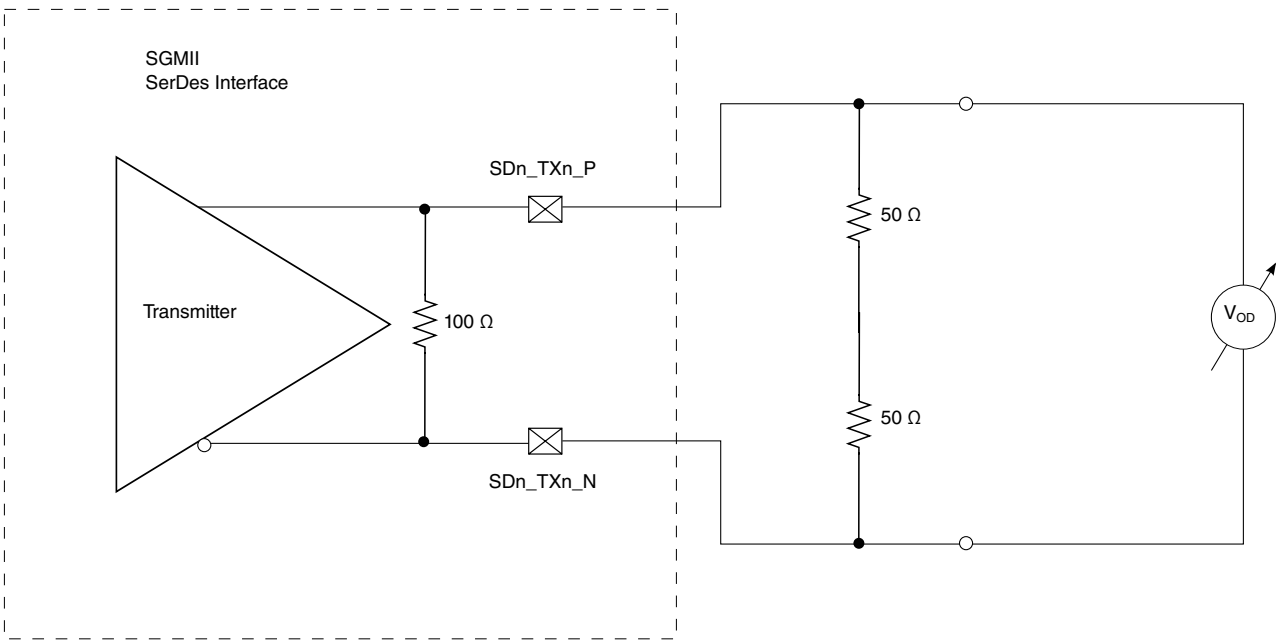


Figure 40. SGMII transmitter DC measurement circuit

This table defines the SGMII 2.5G transmitter DC electrical characteristics for 3.125 GBaud.

Table 93. SGMII 2.5G transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	-	600	mV	-
Output impedance (differential)	R_O	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 3.						

3.16.6.2.2 SGMII and SGMII 2.5 G DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 94. SGMII DC receiver electrical characteristics (SV_{DD} = 0.9 V / 1.0 V)[4]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		-	N/A			-	1
Input differential voltage	REIDL_TH = 001	$V_{RX\_DIFFp-p}$	100	-	1200	mV	2, 5
	REIDL_TH = 100		175	-			
Loss of signal threshold	REIDL_TH = 001	V_{LOS}	30	-	100	mV	3, 5
	REIDL_TH = 100		65	-	175		

Table continues on the next page...

Table 96. SGMII transmit AC timing specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Notes:						
1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.						
2. See Figure 42 for single frequency sinusoidal jitter measurements.						
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.						
4. For recommended operating conditions, see Table 3.						

3.16.6.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) or at the receiver inputs (SD*n*_RX*n*_P and SD*n*_RX*n*_N) respectively, as shown in this figure.

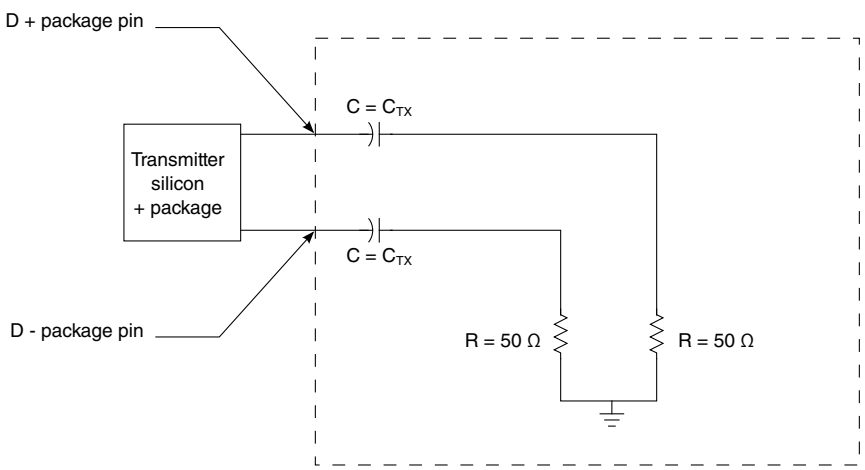


Figure 41. SGMII AC test/measurement load

3.16.6.3.3 SGMII and SGMII 2.5 G receiver AC timing specifications

This table provides the SGMII and SGMII 2.5 G receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 97. SGMII receiver AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2

Table continues on the next page...

The table below describes the output AC timing specifications for the IFC-GPCM and IFC-GASIC interfaces.

Table 119. Integrated flash controller IFC-GPCM and IFC-GASIC interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	10	-	ns	-
IFC_CLK duty cycle	t_{IBKH}/t_{IBK}	45	55	%	-
Output delay	$t_{IBKLOV1}$	-	1.5	ns	-
Output hold	t_{IBKLOX}	-	-2	ns	1
IFC_CLK[0] to IFC_CLK[m] skew	$t_{IBKSKEW}$	0	±75	ps	-

NOTE:

1. The output hold is negative. This means that output transition happens earlier than the falling edge of IFC_CLK.
2. For recommended operating conditions, see Table 3.

The figure below shows the output AC timing diagram for the IFC-GPCM, IFC-GASIC interface.

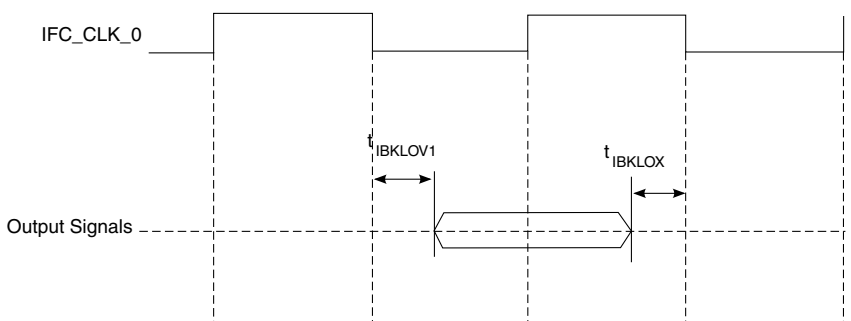


Figure 49. IFC-GPCM, IFC-GASIC signals

3.18.2.3 IFC AC timing specifications (NOR)

The table below describes the input timing specifications for the IFC-NOR interface.

Table 120. Integrated flash controller input timing specifications for NOR mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH2}$	$(2 \times t_{IP\_CLK}) + 2$	-	ns	1
Input hold	$t_{IBIXKH2}$	$(1 \times t_{IP\_CLK}) + 1$	-	ns	1

Notes:

1. t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.
2. For recommended operating conditions, see Table 3.

Table 124. Integrated flash controller IFC-NAND SDR interface AC timing specifications (OVDD = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Address cycle to data loading time	t_{ADL}	O	TADLE - 1500(ps)	TADLE + 1500(ps)	t_{IP_CLK}	Figure 54
ALE hold time	t_{ALH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 55
ALE setup time	t_{ALS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 55
ALE to RE_n delay	t_{AR}	O	TWHRE - 1500(ps)	TWHRE + 1500(ps)	t_{IP_CLK}	Figure 56
CE_n hold time	t_{CH}	O	5 + 1500(ps)	-	ns	Figure 55
CE_n high to input hi-Z	t_{CHZ}	I	TRHZ - 1500(ps)	TRHZ + 1500(ps)	t_{IP_CLK}	Figure 57
CLE hold time	t_{CLH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 55
CLE to RE_n delay	t_{CLR}	O	TWHRE - 1500(ps)	TWHRE - 1500(ps)	t_{IP_CLK}	Figure 58
CLE setup time	t_{CLS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 55
CE_n high to input hold	t_{COH}	I	150 - 1500(ps)	-	ns	Figure 57
CE_n setup time	t_{CS}	O	TCS - 1500(ps)	TCS + 1500(ps)	t_{IP_CLK}	Figure 55
Data hold time	t_{DH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 55
Data setup time	t_{DS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 55
Busy time for Set Features and Get Features	t_{FEAT}	O	-	FTOCNT	t_{IP_CLK}	Figure 59
Output hi-Z to RE_n low	t_{IR}	O	TWHRE - 1500(ps)	TWHRE + 1500(ps)	t_{IP_CLK}	Figure 60
Interface and Timing Mode Change time	t_{ITC}	O	-	FTOCNT	t_{IP_CLK}	Figure 59
RE_n cycle time	t_{RC}	O	TRP + TREH - 1500(ps)	TRP + TREH + 1500(ps)	t_{IP_CLK}	Figure 57
RE_n access time	t_{REA}	I	-	(TRAD - 1) + 2(ns)	t_{IP_CLK}	Figure 57
RE_n high hold time	t_{REH}	I	TREH	TREH	t_{IP_CLK}	Figure 57
RE_n high to input hold	t_{RHOH}	I	0	-	ns	Figure 57
RE_n high to WE_n low	t_{RHW}	O	100 + 1500(ps)	-	ns	Figure 61
RE_n high to input hi-Z	t_{RHZ}	I	TRHZ - 1500(ps)	TRHZ + 1500(ps)	t_{IP_CLK}	Figure 57
RE_n low to input data hold	t_{RLOH}	I	0	-	ns	Figure 62
RE_n pulse width	t_{RP}	O	TRP	TRP	t_{IP_CLK}	Figure 57
Ready to data input cycle (data only)	t_{RR}	O	TRR - 1500(ps)	TRR + 1500(ps)	t_{IP_CLK}	Figure 57

Table continues on the next page...

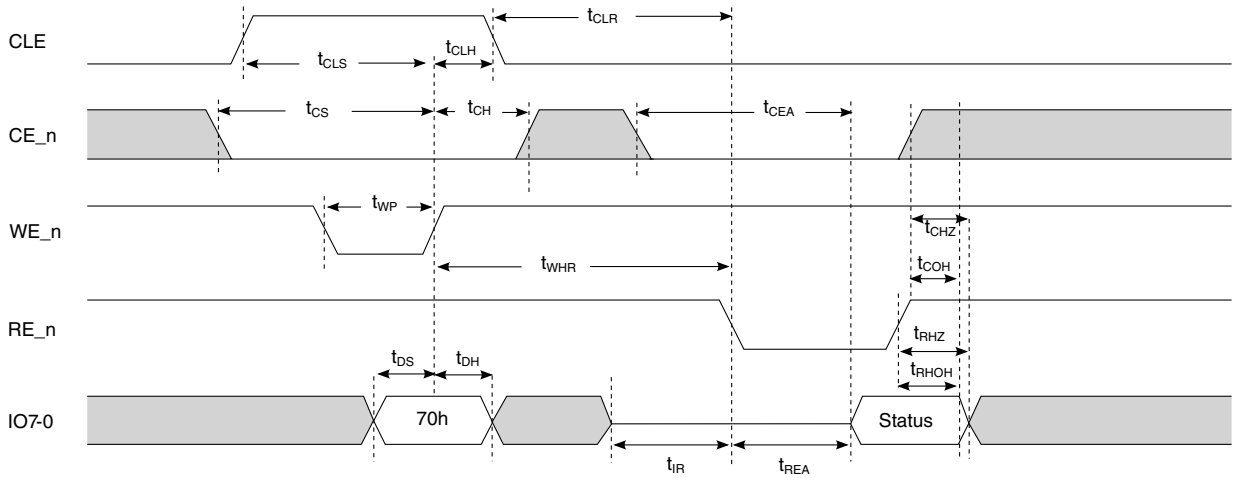


Figure 60. Read status timings

This figure shows the t_{RHW} timings.

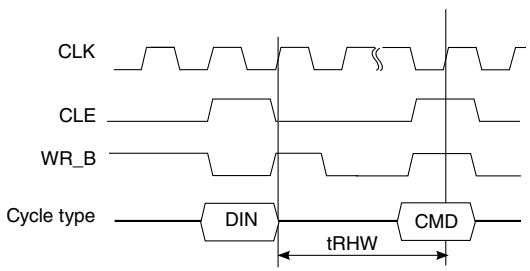


Figure 61. t_{RHW} timings

This figure shows the EDO mode data input cycle timings.

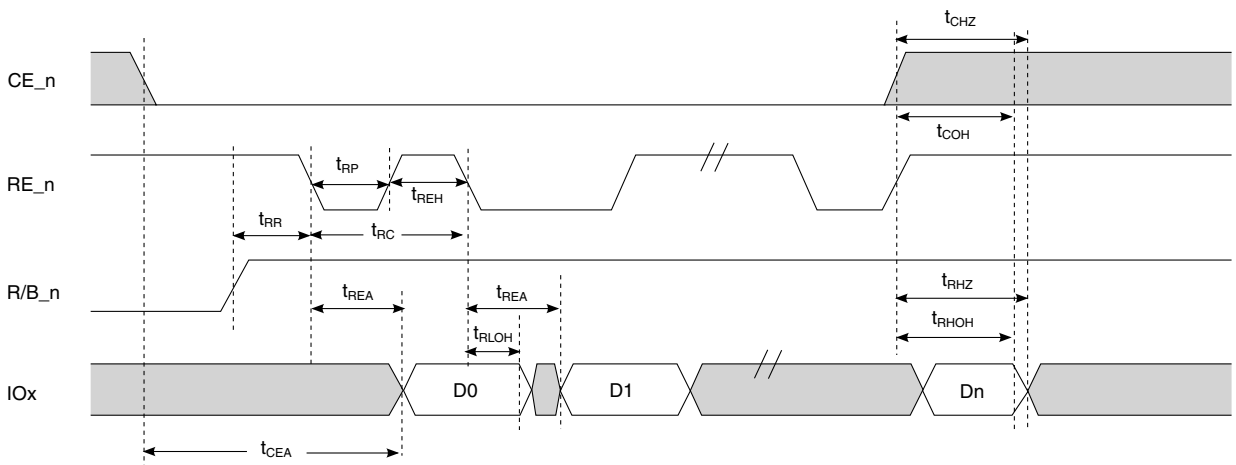


Figure 62. EDO mode data input cycle timings

This figure shows the t_{WB} and t_{RST} timings.

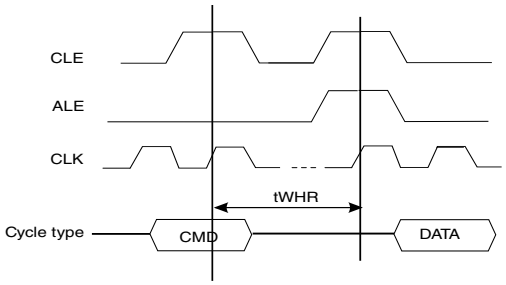


Figure 76. tWHR timings

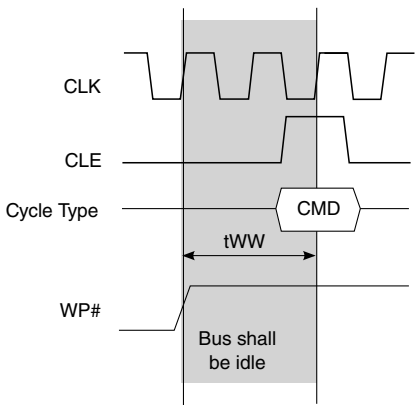


Figure 77. tWW timings

3.19 JTAG interface

This section describes the DC and AC electrical specifications for the JTAG (IEEE 1149.1) interface.

3.19.1 JTAG DC electrical characteristics

This table provides the DC electrical characteristics for the JTAG interface operating at OV_{DD} = 1.8 V.

Table 126. JTAG DC electrical characteristics (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	-100/+50	µA	3, 4
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Table continues on the next page...

The system board designer can choose among several types of commercially available thermal interface materials.

6 Package information

6.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 23 mm x 23 mm, 780 flip-chip, plastic-ball, grid array.

- Package outline - 23 mm x 23 mm
- Interconnects - 780
- Ball Pitch - 0.8 mm
- Ball Diameter (nominal) - 0.45 mm
- Ball Height (nominal) - 0.3 mm
- Solder Balls Composition - 96.5% Sn, 3% Ag, 0.5% Cu
- Module height (typical) - 2.31 mm (minimum), 2.46 mm (typical), 2.61 mm (maximum)

6.2 Mechanical dimensions of the FC-PBGA

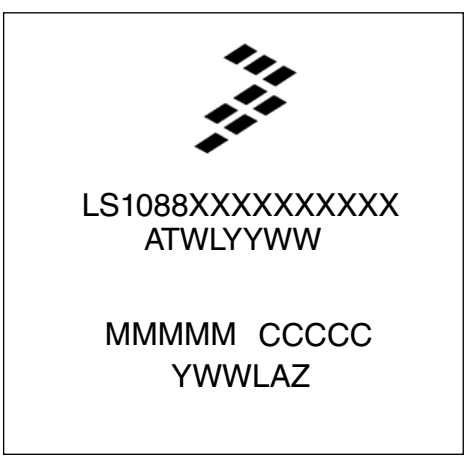
This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.

Table 150. Part numbering nomenclature

q	*p*	*g*	*c*	*u*	*c*	*t*	*e*	*n*	*c*	*d*	r
Qual status	**Product generation**	**Performance level**	**Number of cores**	**Unique ID**	**Core Type**	**Temperature Range**	**Encryption**	**Package type**	**CPU speed[1]**	**DDR data rate**	**Revision**
(blank) = Qualified P = Pre-qual	LS = Layerscape	1	08 = Eight cores 04 = Four cores	8 = with AIOP 4 = without AIOP	A = ARM	S = Standard (0–105°C) X = Extended (-40–105°C)	E = Encryption N = Non-Encryption	7 = FC-PBGA	M = 1200 MHz P = 1400 MHz Q = 1600 MHz	Q = 1600 MHz T = 1800 MHz 1 = 2100 MHz	A = Rev 1.0
1. For the LS1088A family of devices, parts marked with "M" require 0.9 V operating voltage. All others require VID.											

8.2 Part marking

Parts are marked as in the example shown in this figure.



FC-PBGA

Legend:
LS1088XXXXXXXXXX is the part marking on the die.
ATWLYYWW is the test traceability code.
MMMMM is the mask number.
CCCCC is the country code.
YWWLAZ is the assembly traceability code.

Figure 98. Part marking for FC-PBGA chip