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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	8 Core, 64-Bit
Speed	1.2GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	DDR4
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10GbE (2), 1GbE (8)
SATA	SATA 6Gbps (1)
USB	USB 3.0 + PHY (2)
Voltage - I/O	1.2V
Operating Temperature	0°C ~ 105°C (TJ)
Security Features	Secure Boot, TrustZone®
Package / Case	780-BFBGA
Supplier Device Package	780-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088asn7mqa

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_A03/GPIO1_19/ QSPI_B_CS0	IFC Address	D10	O	OV_{DD}	1, 5
IFC_A04/GPIO1_20/ QSPI_B_CS1	IFC Address	C10	O	OV_{DD}	1, 5
IFC_A05/GPIO1_21/ QSPI_B_SCK/cfg_dram_type	IFC Address	C11	O	OV_{DD}	1, 4
IFC_A06/GPIO2_00/ IFC_WP1_B/QSPI_A_DATA0	IFC Address	D11	O	OV_{DD}	1
IFC_A07/GPIO2_01/ IFC_WP2_B/QSPI_A_DATA1	IFC Address	C12	O	OV_{DD}	1
IFC_A08/GPIO2_02/ IFC_WP3_B/QSPI_A_DATA2	IFC Address	D13	O	OV_{DD}	1
IFC_A09/GPIO2_03/ IFC_RB2_B/IFC_CS_B4/ QSPI_A_DATA3	IFC Address	C13	O	OV_{DD}	1
IFC_A10/GPIO2_04/ IFC_RB3_B/IFC_CS_B5/ QSPI_A_DQS	IFC Address	D14	O	OV_{DD}	1
IFC_A11/GPIO2_05/ IFC_CS_B6/QSPI_B_DQS	IFC Address	C14	O	OV_{DD}	1
IFC_AD00/GPIO1_00/ cfg_gpinput0	IFC Address / Data	B12	IO	OV_{DD}	4, 9
IFC_AD01/GPIO1_01/ cfg_gpinput1	IFC Address / Data	A11	IO	OV_{DD}	4, 9
IFC_AD02/GPIO1_02/ cfg_gpinput2	IFC Address / Data	B11	IO	OV_{DD}	4, 9
IFC_AD03/GPIO1_03/ cfg_gpinput3	IFC Address / Data	A10	IO	OV_{DD}	4, 9
IFC_AD04/GPIO1_04/ cfg_gpinput4	IFC Address / Data	A9	IO	OV_{DD}	4, 9
IFC_AD05/GPIO1_05/ cfg_gpinput5	IFC Address / Data	B9	IO	OV_{DD}	4, 9
IFC_AD06/GPIO1_06/ cfg_gpinput6	IFC Address / Data	A8	IO	OV_{DD}	4, 9
IFC_AD07/GPIO1_07/ cfg_gpinput7	IFC Address / Data	B8	IO	OV_{DD}	4, 9
IFC_AD08/GPIO1_08/ cfg_rcw_src1	IFC Address / Data	A12	IO	OV_{DD}	4, 9
IFC_AD09/GPIO1_09/ cfg_rcw_src2	IFC Address / Data	A13	IO	OV_{DD}	4, 9
IFC_AD10/GPIO1_10/ cfg_rcw_src3	IFC Address / Data	B14	IO	OV_{DD}	4, 9
IFC_AD11/GPIO1_11/ cfg_rcw_src4	IFC Address / Data	A14	IO	OV_{DD}	4, 9

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DIFF_SYSCLK_B	Single Source System Clock Differential (negative)	AB13	I	SV_{DD}	20
RTC/GPIO3_30	Real Time Clock	F17	I	OV_{DD}	1
SYSCLK	System Clock	G14	I	OV_{DD}	---
DDR Clocking					
DDRCLK	DDR Controller Clock	J20	I	OV_{DD}	---
DFT					
JTAG_BSR_VSEL	Reserved	J19	I	OV_{DD}	15
SCAN_MODE_B	Reserved	H19	I	OV_{DD}	10
TBSCAN_EN_B	Test Boundary Scan Enable	F19	I	OV_{DD}	6
TEST_SEL_B	Reserved	F20	I	OV_{DD}	10
JTAG					
TCK	Test Clock	E18	I	OV_{DD}	---
TDI	Test Data In	G17	I	OV_{DD}	9
TDO	Test Data Out	E20	O	OV_{DD}	2
TMS	Test Mode Select	G18	I	OV_{DD}	9
TRST_B	Test Reset	E19	I	OV_{DD}	9
Analog Signals					
D1_TPA	Reserved	F21	IO		12
FA_ANALOG_G_V	Reserved	AG21	IO		15
FA_ANALOG_PIN	Reserved	AD21	IO		15
TD1_ANODE	Thermal diode anode	J13	IO		17
TD1_CATHODE	Thermal diode cathode	H13	IO		17
TH_TPA	Reserved	H8	-	-	12
SerDes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	Y11	I	SV_{DD}	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AA6	I	XV_{DD}	16
SD1_PLL1_TPA	SerDes PLL 1 Test Point Analog	AF12	O	AVDD_SD1_PLL1	12
SD1_PLL1_TPD	SerDes Test Point Digital	AF13	O	XV_{DD}	12
SD1_PLL2_TPA	SerDes PLL 2 Test Point Analog	AF5	O	AVDD_SD1_PLL2	12
SD1_PLL2_TPD	SerDes Test Point Digital	AB5	O	XV_{DD}	12
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AH13	I	SV_{DD}	---
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	AG13	I	SV_{DD}	---
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AB8	I	SV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD18	DDR supply	AA27	---	$G1V_{DD}$	---
G1VDD19	DDR supply	AC27	---	$G1V_{DD}$	---
G1VDD20	DDR supply	AE27	---	$G1V_{DD}$	---
G1VDD21	DDR supply	AG27	---	$G1V_{DD}$	---
G1VDD22	DDR supply	AH27	---	$G1V_{DD}$	---
SVDD1	SerDes transceiver supply	W7	---	SV_{DD}	---
SVDD2	SerDes transceiver supply	W8	---	SV_{DD}	---
SVDD3	SerDes transceiver supply	W9	---	SV_{DD}	---
SVDD4	SerDes transceiver supply	W10	---	SV_{DD}	---
SVDD5	SerDes transceiver supply	W13	---	SV_{DD}	---
SVDD6	SerDes transceiver supply	W14	---	SV_{DD}	---
SVDD7	SerDes transceiver supply	W15	---	SV_{DD}	---
SVDD8	SerDes transceiver supply	W16	---	SV_{DD}	---
XVDD1	SerDes transceiver supply	AC7	---	XV_{DD}	---
XVDD2	SerDes transceiver supply	AC9	---	XV_{DD}	---
XVDD3	SerDes transceiver supply	AC12	---	XV_{DD}	---
XVDD4	SerDes transceiver supply	AC14	---	XV_{DD}	---
XVDD5	SerDes transceiver supply	AC17	---	XV_{DD}	---
XVDD6	SerDes transceiver supply	AC20	---	XV_{DD}	---
FA_VL	Reserved	AB21	---	FA_VL	---
PROG_MTR	Reserved	F13	---	PROG_MTR	---
TA_PROG_SFP	SFP Fuse Programming Override supply	G13	---	TA_PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	G8	---	TH_V_{DD}	---
VDD01	Supply for cores and platform	K14	---	V_{DD}	---
VDD02	Supply for cores and platform	K16	---	V_{DD}	---
VDD03	Supply for cores and platform	K18	---	V_{DD}	---
VDD04	Supply for cores and platform	K20	---	V_{DD}	---
VDD05	Supply for cores and platform	K22	---	V_{DD}	---
VDD06	Supply for cores and platform	L9	---	V_{DD}	---
VDD07	Supply for cores and platform	L11	---	V_{DD}	---
VDD08	Supply for cores and platform	L13	---	V_{DD}	---
VDD09	Supply for cores and platform	L15	---	V_{DD}	---
VDD10	Supply for cores and platform	L17	---	V_{DD}	---
VDD11	Supply for cores and platform	L19	---	V_{DD}	---
VDD12	Supply for cores and platform	L21	---	V_{DD}	---
VDD13	Supply for cores and platform	M10	---	V_{DD}	---
VDD14	Supply for cores and platform	M12	---	V_{DD}	---

Table continues on the next page...

3.2 General AC timing specifications

This table provides AC timing specifications for the sections not covered under the specific interface sections.

Table 5. AC Timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Input signal rise and fall times	t_R/t_F	-	5	ns	1
1. Rise time refers to signal transitions from 10% to 90% of Supply; fall time refers to transitions from 90% to 10% of supply					

3.3 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For power up, these requirements are as follows:

1. AV_{DD}_SDn_PLL1, AV_{DD}_SDn_PLL2, EV_{DD}, DV_{DD}, LV_{DD}, OV_{DD}, SV_{DD}, TV_{DD}, XV_{DD}, USB_HV_{DD}, USB_SDV_{DD}, USB_SV_{DD}. Drive TA_PROG_SFP = GND.
   - PORESET_B input must be driven asserted and held during this step.
2. V_{DD}.
3. $G1V_{DD}$.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of their value. XV_{DD}, AV_{DD}_SD*n*_PLL1, and AV_{DD}_SD*n*_PLL2 have no ordering requirement to any other supplies, and they can ramp up in any step. SV_{DD} should ramp up before VDD. Alternatively, V_{DD} may ramp up together with SV_{DD} provided that the relative timing between SV_{DD} and V_{DD} ramp up conforms to Figure 8 below.

All supplies must be at their stable values within 400 ms.

Negate PORESET_B input when the required assertion/hold time has been met per RESET initialization timing specifications.

NOTE

- While V_{DD} is ramping up, leakage current might occur from V_{DD} through LS1088A to $G1V_{DD}$.
- Ensure that SYSCLK is available as soon as power ramps up.
- Ramp rate requirements should be met per Table 11.

3.7.1.1 SYSCLK DC electrical characteristics

This table provides the SYSCLK DC characteristics.

Table 12. SYSCLK DC electrical characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 X OV_{DD}	—	—	V	1
Input low voltage	V_{IL}	—	—	0.3 X OV_{DD}	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (V_{IN}= 0 V or V_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. At recommended operating conditions with OV_{DD}= 1.8 V. See Table 3.

3.7.1.2 SYSCLK AC timing specifications

This table provides the SYSCLK AC timing specifications.

Table 13. SYSCLK AC timing specifications[1, 5]

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	100.0	—	125/133.3	MHz	2, 6
SYSCLK cycle time	t_{SYSCLK}	7.5	—	10.0	ns	1, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at -56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	1.08	—	1.8	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequencies do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8 V. See Table 3.
6. The 125 MHz max frequency is limited to parts with 1200 MHz CPU frequency. The 133 MHz max frequency can be used for parts with 1600 MHz and 1400 MHz CPU frequency.

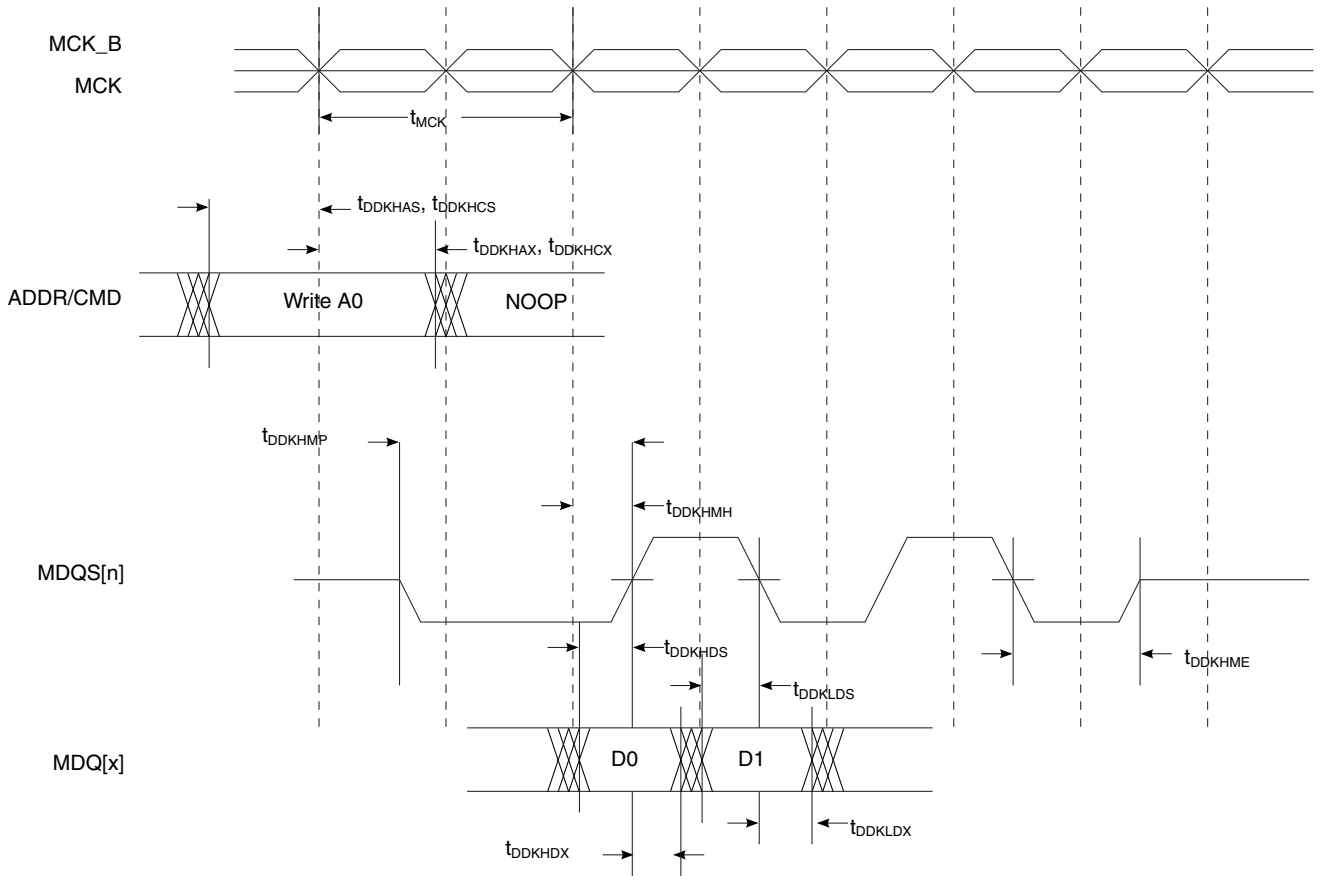

Figure 13. DDR4 output timing diagram

3.11 Dual universal asynchronous receiver/transmitter (DUART) interface

This section describes the DC and AC electrical characteristics for the DUART interface.

3.11.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface when operating at DV_{DD} = 3.3 V.

Table 30. DUART DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x DVDD	V	2

Table continues on the next page...

Table 30. DUART DC electrical characteristics (DV_{DD} = 3.3 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	µA	3
Output high voltage (I_{OH} = -2.0 mA)	V_{OH}	2.4	-	V	-
Output low voltage (I_{OL} = 2.0 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.

2. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in the Recommended Operating Conditions table.

3. Note that the symbol DV_{IN} represents the input voltage of the supply referenced in the Recommended Operating Conditions table.

This table provides the DC electrical characteristics for the DUART interface when operating at DV_{DD} = 1.8 V.

Table 31. DUART DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x DV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	µA	3
Output high voltage (I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.

2. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in the Recommended Operating Conditions table.

3. Note that the symbol DV_{IN} represents the input voltage of the supply referenced in the Recommended Operating Conditions table.

3.11.2 DUART AC timing specifications

This table provides the AC timing specifications for the DUART interface.

Table 32. DUART AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Minimum baud rate	baud	f_{PLAT}/(2 x 1,048,576)	-	baud	1, 2
Maximum baud rate	baud	-	f_{PLAT}/(2 x 16)	baud	1, 3

1. f_{PLAT} refers to the internal platform clock.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

3. The actual attainable baud rate is limited by the latency of interrupt processing.

Table 37. eSDHC AC timing specifications (DDR50/DDR)[3] (continued)

Parameter	Symbol	Min	Max	Units	Notes
Notes:					
1. C_{CARD} ≤ 10 pF, (1 card).					
2. $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ ≤ 20 pF for MMC, ≤ 25pF for Input Data of DDR50, ≤ 30pF for Input CMD of DDR50.					
3. For recommended operating conditions, see Table 3.					
4. Total clock duty cycle and data and clock skew on the board should be limited to 0.2ns.					
5. Total clock duty cycle and command and clock skew on the board should be limited to 0.3ns.					

This figure provides the eSDHC DDR50/DDR mode input AC timing diagram.

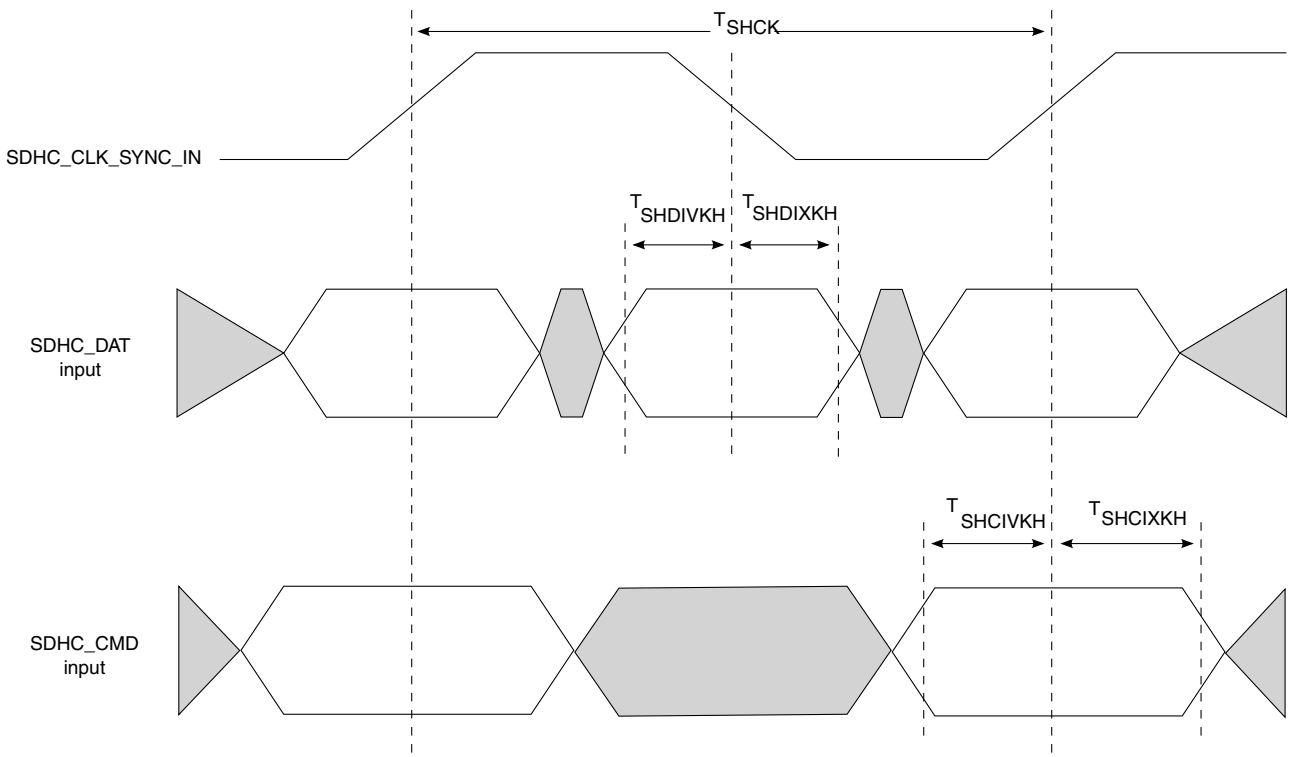

Figure 20. eSDHC DDR50/DDR mode input AC timing diagram

This figure provides the eSDHC DDR50/DDR mode output AC timing diagram.

Table 42. EMI2 DC electrical characteristics (TV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
3. The symbol TV_{IN} represents the input voltage of the supply referenced in Table 3.					
4. The symbol TV_{DD} represents the input voltage of the supply referenced in Table 3.					

This table provides the EMI2 DC electrical characteristics when operating at TV_{DD} = 1.8 V.

Table 43. EMI2 DC electrical characteristics (TV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TVDD	-	-	2
Input low voltage	V_{IL}	-	0.3 x TVDD	-	2
Input current (V_{IN} = 0 or V_{IN} = TV_{DD})	I_{IN}	-50.0	50.0	-	3, 4
Output high voltage (TV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	-	4
Output low voltage (TV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	-	4
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3.					
3. The symbol TV_{IN} represents the input voltage of the supply referenced in Table 3.					
4. The symbol TV_{DD} represents the input voltage of the supply referenced in Table 3.					

This table provides the EMI2 DC electrical characteristics when operating at TV_{DD} = 1.2 V.

Table 44. EMI2 DC electrical characteristics (TV_{DD} = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TVDD	-	-	2
Input low voltage	V_{IL}	-	0.2 x TVDD	-	2
Output low current (V_{OL} = 0.2 V)	I_{OL}	4.0	-	mA	-
Output high voltage (TV_{DD} = min, I_{OH} = -100 µA)	V_{OH}	1.0	-	V	3
Output low voltage (TV_{DD} = min, I_{OL} = 100 µA)	V_{OL}	-	0.2	V	3
Input capacitance	C_{IN}	-	10.0	pF	-
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3.					
3. The symbol TV_{DD} represents the input voltage of the supply referenced in Table 3.					

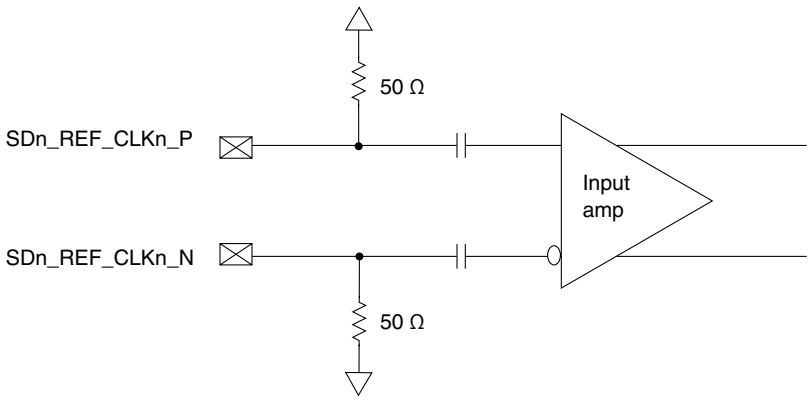

Figure 30. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes transceiver's core power supply voltage requirements (SV_{DD}) are as specified in Table 3.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N are internally AC-coupled differential inputs as shown in Figure 30. Each differential clock input (SD*n*_REF_CLK*n*_P or SD*n*_REF_CLK*n*_N) has on-chip 50-Ω termination to SGND*n* followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions in Signal terms definitions for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND*n*. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N inputs cannot drive 50 Ω to SGND*n* DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.16.7.1 QSGMII clocking requirements for SDn_REF_CLKn_P and SDn_REF_CLKn_N

For more information on these specifications, see the SerDes reference clocks section of this data sheet.

3.16.7.2 QSGMII DC electrical characteristics

This table describes the QSGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N).

Table 98. QSGMII transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit
Output differential voltage	V_{DIFF}	400.0	-	900.0	mV
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω
1. For recommended operating conditions, see Table 3.					

This table defines the QSGMII receiver DC electrical characteristics.

Table 99. QSGMII receiver DC timing specifications (SV_{DD} = 0.9 V / 1.0 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit
Input differential voltage	V_{DIFF}	100.0	-	900.0	mV
Differential resistance	R_{RDIN}	80.0	100.0	120.0	Ω
1. For recommended operating conditions, see Table 3.					

3.16.7.3 QSGMII AC timing specifications

This table provides the QSGMII transmitter AC timing specifications.

Table 100. QSGMII transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud rate	T_{BAUD}	5.000-100ppm	5.0	5.000+100ppm	Gb/s
Uncorrelated high probability jitter	T_{UHPJ}	-	-	0.15	UI p-p
Total jitter tolerance	J_T	-	-	0.3	UI p-p

This table provides the QSGMII receiver AC timing specifications.

The figure below shows the AC input timing diagram for input signals for the IFC-NOR interface. Here TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.

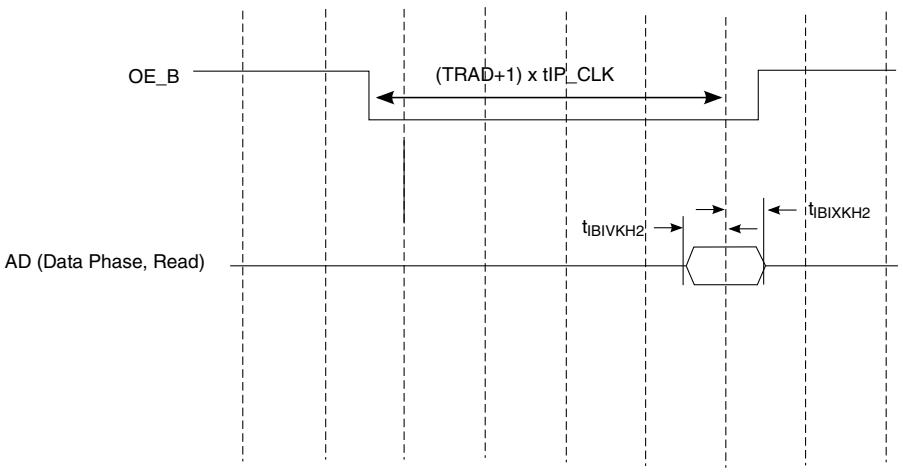

Figure 50. IFC-NOR interface input AC timings

The table below describes the output AC timing specifications of IFC-NOR interface.

Table 121. Integrated flash controller IFC-NOR interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV2}$	-	±1.5	ns	1

NOTE:

1. This effectively means that a signal change may appear anywhere within $\pm t_{IBKLOV2}$ (max) duration, from the point where it's expected to change.

2. For recommended operating conditions, see Table 3.

The figure below shows the AC timing diagram for IFC-NOR interface output signals. The timing specs have been illustrated here by taking timings between two signals, CS_B and OE_B as an example. In a read operation, OE_B is supposed to change the TACO (a programmable delay; see the IFC section of the chip reference manual for more information) time after CS_B. Because of the skew between the signals, OE_B may change anywhere within the window of time defined by tIBKLOV2. This concept applies to other IFC-NOR interface output signals as well. The diagram is an example that shows the skew between any two chronological toggling signals as per the protocol. The list of IFC-NOR output signals is as follows: NRALE, NRAVD_B, NRWE_B, NROE_B, CS_B, AD (Address phase).

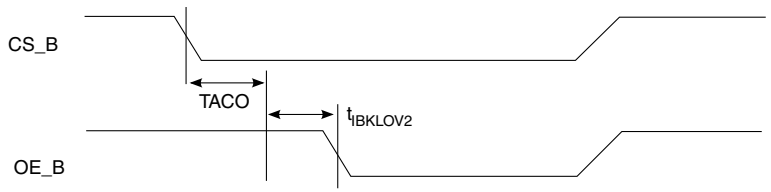

Figure 51. IFC-NOR interface output AC timings

3.18.2.4 IFC AC timing specifications (NAND)

The table below describes the input timing specifications of the IFC-NAND interface.

Table 122. Integrated flash controller input timing specifications for NAND mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH3}$	(2 x t_{IP_CLK}) + 2	-	ns	1
Input hold	$t_{IBIXKH3}$	1	-	ns	1
IFC_RB_B pulse width	t_{IBCH}	2	-	t_{IP_CLK}	1
NOTE: 1. t_{IP_CLK} is the period of ip clock on which IFC is running. 2. For recommended operating conditions, see Table 3.					

The figure below shows the AC input timing diagram for input signals of IFC-NAND interface. Here TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.

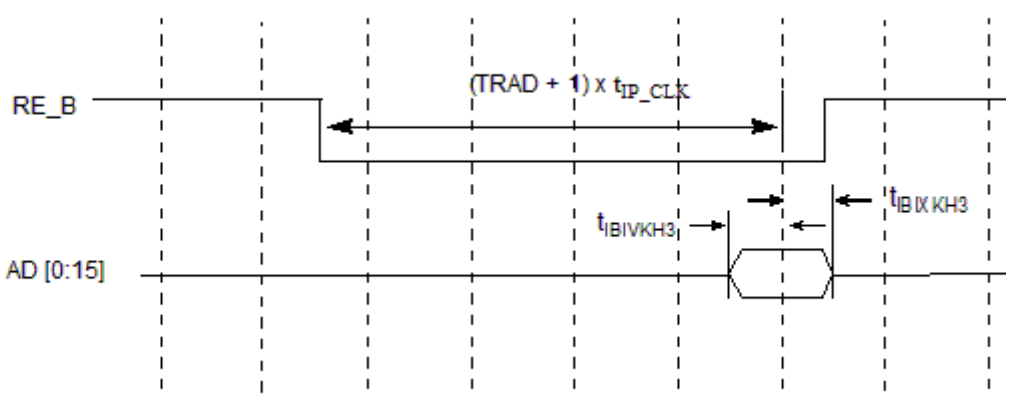

Figure 52. IFC-NAND interface input AC timings

NOTE

t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.

The table below describes the output AC timing specifications for the IFC-NAND interface.

Table 123. Integrated flash controller IFC-NAND interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV3}$	-	±1.5	ns	1

NOTE:

1. This effectively means that a signal change may appear anywhere within $t_{IBKLOV3}$ (min) to $t_{IBKLOV3}$ (max) duration, from the point where it's expected to change.

2. For recommended operating conditions, see Table 3.

The figure below shows the AC timing diagram for output signals of IFC-NAND interface.The timing specs are shown here by taking the timings between two signals, CS_B and CLE as an example. CLE is supposed to change TCCST (a programmable delay; see the IFC section of the chip reference manual for more information) time after CS_B. Because of the skew between the signals, CLE may change anywhere within window of time defined by $t_{IBKLOV3}$. This concept applies to other output signals of the IFC-NAND interface as well. The diagram is an example to show the skew between any two chronological toggling signals as per the protocol. The list of output signals is as follows: NDWE_B, NDRE_B, NDALE, WP_B, NDCLE, CS_B, AD.

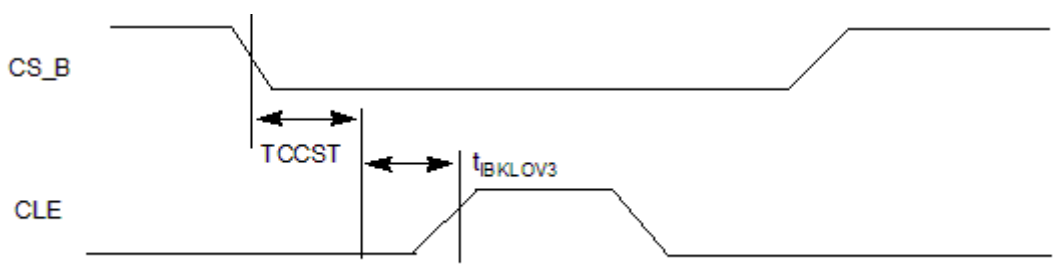

Figure 53. IFC-NAND interface output AC timings

3.18.2.5 IFC-NAND SDR AC timing specifications

This table describes the AC timing specifications for the IFC-NAND SDR interface. These specifications are compliant to the SDR mode of the ONFI specification revision 3.0.

Table 124. Integrated flash controller IFC-NAND SDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	t_{RST} (raw NAND)	O	-	FTOCNT	t_{IP_CLK}	Figure 63
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	t_{RST2} (EZ NAND)	O	-	FTOCNT	t_{IP_CLK}	Figure 63
(WE_n high or CLK rising edge) to SR[6] low	t_{WB}	O	TWBE + TWH - 1500(ps)	TWBE + TWH + 1500(ps)	t_{IP_CLK}	Figure 55
WE_n cycle time	t_{WC}	O	TWP + TWH	TWP + TWH	t_{IP_CLK}	Figure 64
WE_n high hold time	t_{WH}	O	TWH	TWH	t_{IP_CLK}	Figure 64
Command, address, or data input cycle to data output cycle	t_{WHR}	O	TWHRE + TWH - 1500(ps)	TWHRE + TWH + 1500(ps)	t_{IP_CLK}	Figure 65
WE_n pulse width	t_{WP}	O	TWP	TWP	t_{IP_CLK}	Figure 55
WP_n transition to command cycle	t_{WW}	O	TWW - 1500(ps)	TWW + 1500(ps)	t_{IP_CLK}	Figure 66
Data Input hold	$t_{IBIXKH4}$	I	1	-	t_{IP_CLK}	Figure 67

NOTE:

1. t_{IP_CLK} is the clock period of the IP clock (on which the IFC IP is running). Note that that the IFC IP clock does not come out of the device.

This figure shows the t_{ADL} timing.

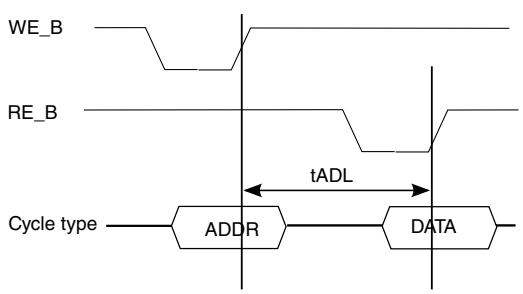

Figure 54. t_{ADL} timing

This figure shows the command cycle.

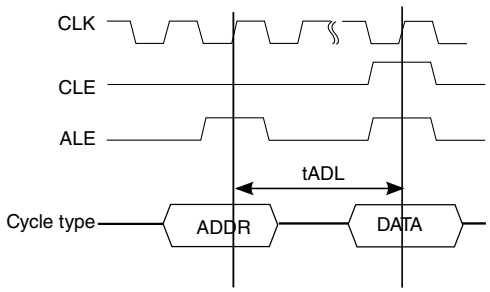

Figure 72. t_{ADL} timings

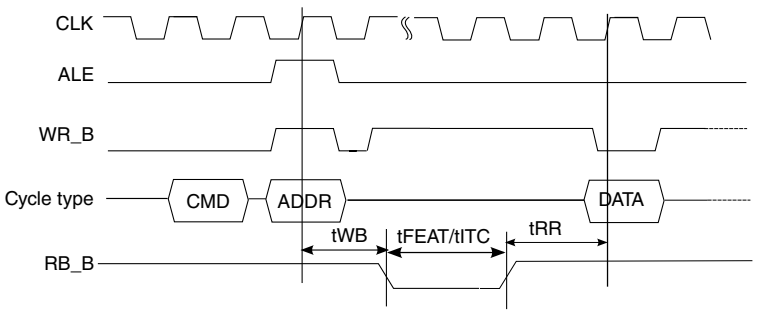

Figure 73. t_{WB}, t_{FEAT}, t_{ITC}, t_{RR} timings

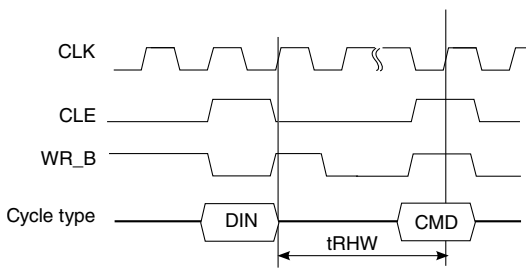

Figure 74. t_{RHW} timings

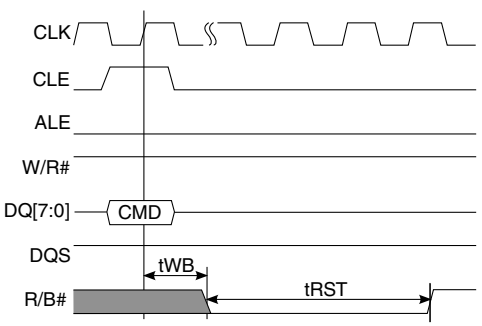

Figure 75. t_{WB} and t_{RST} timings

Table 134. HDLC AC timing specifications

Parameter	Symbol	Min	Max	Unit
Internal clock delay	t_{HIKHOV}	0.0	5.5	-
External clock delay	t_{HEKHOV}	1.0	13.0	ns
Internal clock high impedance	t_{HIKHOX}	0.0	5.5	ns
External clock high impedance	t_{HEKHOX}	1.0	8.0	ns
Internal clock input setup time	t_{HIIVKH}	12.6	-	ns
External clock input setup time	t_{HEIVKH}	4.0	-	ns
Internal clock input hold time	t_{HIIXKH}	0.0	-	ns
External clock input hold time	t_{HEIXKH}	1.0	-	ns

This table provides the input and output AC timing specifications for the synchronous UART protocols.

Table 135. Synchronous UART AC timing specifications

Parameter	Symbol	Min	Max	Unit
Internal clock delay	t_{HIKHOV}	0.0	11.0	-
External clock delay	t_{HEKHOV}	1.0	14.0	ns
Internal clock high impedance	t_{HIKHOX}	0.0	11.0	ns
External clock high impedance	t_{HEKHOX}	1.0	14.0	ns
Internal clock input setup time	t_{HIIVKH}	10.0	-	ns
External clock input setup time	t_{HEIVKH}	8.0	-	ns
Internal clock input hold time	t_{HIIXKH}	0.0	-	ns
External clock input hold time	t_{HEIXKH}	1.0	-	ns

This figure shows the AC test load for the HDLC interface.

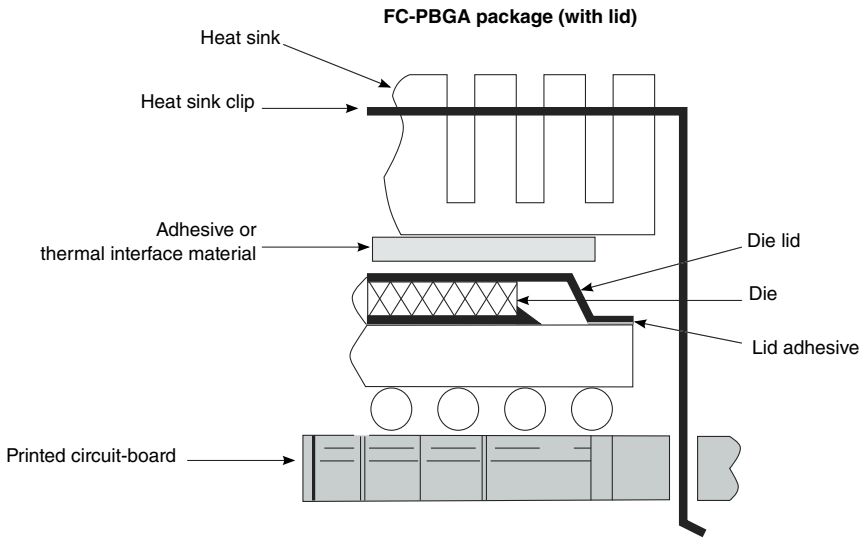

Figure 95. Package exploded, cross-sectional view-FC-PBGA (with lid)

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

5.3.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure shows the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.
7. Pin 1 thru hole shall be centered within foot area.
8. 23.2 mm maximum package assembly (lid + laminate) X and Y.

7 Security fuse processor

This chip implements trust architecture 3.0, which supports capabilities such as secure boot. Use of the trust architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8 V to the TA_PROG_SFP pin per Power sequencing. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times, TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Power sequencing. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

NOTE

Users not implementing the QorIQ platform's trust architecture features should connect TA_PROG_SFP to GND.

8 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

8.1 Part numbering nomenclature

This table provides the NXP Layerscape platform part numbering nomenclature.