Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	8 Core, 64-Bit
Speed	1.4GHz
Co-Processors/DSP	-
RAM Controllers	DDR4
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	10GbE (2), 1GbE (8)
SATA	SATA 6Gbps (1)
USB	USB 3.0 (2) + PHY
Voltage - I/O	-
Operating Temperature	0°C ~ 105°C
Security Features	Secure Boot, TrustZone®
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088asn7pta

2.1 780 BGA ball layout diagrams

This figure shows the complete view of the LS1088A BGA ball map diagram. Figure 3, Figure 4, Figure 5, and Figure 6 show quadrant views.

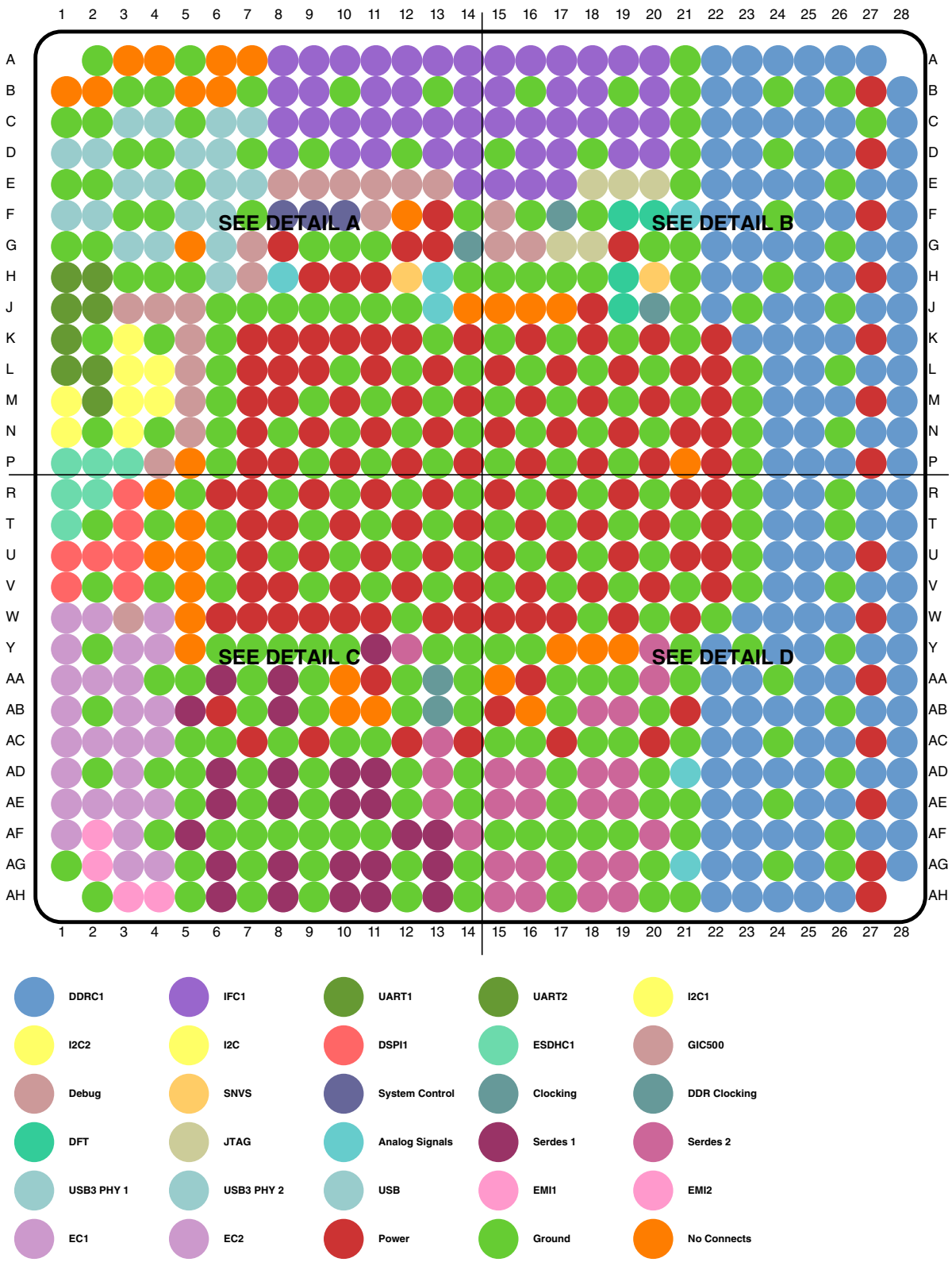

Figure 2. Complete BGA Map for the LS1088A

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_A03/GPIO1_19/ QSPI_B_CS0	IFC Address	D10	O	OV_{DD}	1, 5
IFC_A04/GPIO1_20/ QSPI_B_CS1	IFC Address	C10	O	OV_{DD}	1, 5
IFC_A05/GPIO1_21/ QSPI_B_SCK/cfg_dram_type	IFC Address	C11	O	OV_{DD}	1, 4
IFC_A06/GPIO2_00/ IFC_WP1_B/QSPI_A_DATA0	IFC Address	D11	O	OV_{DD}	1
IFC_A07/GPIO2_01/ IFC_WP2_B/QSPI_A_DATA1	IFC Address	C12	O	OV_{DD}	1
IFC_A08/GPIO2_02/ IFC_WP3_B/QSPI_A_DATA2	IFC Address	D13	O	OV_{DD}	1
IFC_A09/GPIO2_03/ IFC_RB2_B/IFC_CS_B4/ QSPI_A_DATA3	IFC Address	C13	O	OV_{DD}	1
IFC_A10/GPIO2_04/ IFC_RB3_B/IFC_CS_B5/ QSPI_A_DQS	IFC Address	D14	O	OV_{DD}	1
IFC_A11/GPIO2_05/ IFC_CS_B6/QSPI_B_DQS	IFC Address	C14	O	OV_{DD}	1
IFC_AD00/GPIO1_00/ cfg_gpinput0	IFC Address / Data	B12	IO	OV_{DD}	4, 9
IFC_AD01/GPIO1_01/ cfg_gpinput1	IFC Address / Data	A11	IO	OV_{DD}	4, 9
IFC_AD02/GPIO1_02/ cfg_gpinput2	IFC Address / Data	B11	IO	OV_{DD}	4, 9
IFC_AD03/GPIO1_03/ cfg_gpinput3	IFC Address / Data	A10	IO	OV_{DD}	4, 9
IFC_AD04/GPIO1_04/ cfg_gpinput4	IFC Address / Data	A9	IO	OV_{DD}	4, 9
IFC_AD05/GPIO1_05/ cfg_gpinput5	IFC Address / Data	B9	IO	OV_{DD}	4, 9
IFC_AD06/GPIO1_06/ cfg_gpinput6	IFC Address / Data	A8	IO	OV_{DD}	4, 9
IFC_AD07/GPIO1_07/ cfg_gpinput7	IFC Address / Data	B8	IO	OV_{DD}	4, 9
IFC_AD08/GPIO1_08/ cfg_rcw_src1	IFC Address / Data	A12	IO	OV_{DD}	4, 9
IFC_AD09/GPIO1_09/ cfg_rcw_src2	IFC Address / Data	A13	IO	OV_{DD}	4, 9
IFC_AD10/GPIO1_10/ cfg_rcw_src3	IFC Address / Data	B14	IO	OV_{DD}	4, 9
IFC_AD11/GPIO1_11/ cfg_rcw_src4	IFC Address / Data	A14	IO	OV_{DD}	4, 9

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB1_RESREF	USB PHY Impedance Calibration	G3	IO	-	---
USB1_RX_M	USB PHY SS Receive Data (-)	E4	I	-	---
USB1_RX_P	USB PHY SS Receive Data (+)	E3	I	-	---
USB1_TX_M	USB PHY SS Transmit Data (-)	F2	O	-	---
USB1_TX_P	USB PHY SS Transmit Data (+)	F1	O	-	---
USB1_VBUS	USB PHY VBUS	E7	I	-	---
USB PHY 2					
USB2_D_M	USB PHY HS Data (-)	C6	IO	-	---
USB2_D_P	USB PHY HS Data (+)	D6	IO	-	---
USB2_ID	USB PHY ID Detect	D5	I	-	---
USB2_RESREF	USB PHY Impedance Calibration	G4	IO	-	---
USB2_RX_M	USB PHY SS Receive Data (-)	C4	I	-	---
USB2_RX_P	USB PHY SS Receive Data (+)	C3	I	-	---
USB2_TX_M	USB PHY SS Transmit Data (-)	D2	O	-	---
USB2_TX_P	USB PHY SS Transmit Data (+)	D1	O	-	---
USB2_VBUS	USB PHY VBUS	C7	I	-	---
USB1 and 2					
USB2_DRVVBUS/**IIC3_SCL**/ GPIO4_28/EVT5_B/BRGO4/ CLK11	DRV VBus	L4	O	DV_{DD}	1
USB2_PWRFAULT/**IIC3_SDA**/ GPIO4_29/EVT6_B/BRGO1/ CLK12_CLK8	PWR Fault	M4	I	DV_{DD}	1
USB_DRVVBUS/GPIO4_02	USB_DRVVBUS	H6	O	DV_{DD}	1
USB_PWRFAULT/GPIO4_03	USB_PWRFAULT	G6	I	DV_{DD}	1
Ethernet Management Interface 1					
EMI1_MDC/GPIO4_00	Management Data Clock	AG2	O	LV_{DD}	1, 13
EMI1_MDIO/GPIO4_01	Management Data In/Out	AF2	IO	LV_{DD}	13
Ethernet Management Interface 2					
EMI2_MDC/GPIO2_20	Management Data Clock	AH4	O	TV_{DD}	1
EMI2_MDIO/GPIO2_21	Management Data In/Out	AH3	IO	TV_{DD}	---
Ethernet Controller 1					
EC1_GTX_CLK/GPIO2_27	Transmit Clock Out	W4	O	LV_{DD}	1
EC1_GTX_CLK125/GPIO2_28	Reference Clock	AC3	I	LV_{DD}	1
EC1_RXD0/GPIO4_12	Receive Data	AA2	I	LV_{DD}	1
EC1_RXD1/GPIO4_11	Receive Data	AA1	I	LV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND031	Core, Platform and PLL Ground	E21	---	---	---
GND032	Core, Platform and PLL Ground	E26	---	---	---
GND033	Core, Platform and PLL Ground	F3	---	---	---
GND034	Core, Platform and PLL Ground	F4	---	---	---
GND035	Core, Platform and PLL Ground	F7	---	---	---
GND036	Core, Platform and PLL Ground	F14	---	---	---
GND037	Core, Platform and PLL Ground	F16	---	---	---
GND038	Core, Platform and PLL Ground	F18	---	---	---
GND039	Core, Platform and PLL Ground	F24	---	---	---
GND040	Core, Platform and PLL Ground	G1	---	---	---
GND041	Core, Platform and PLL Ground	G2	---	---	---
GND042	Core, Platform and PLL Ground	G9	---	---	---
GND043	Core, Platform and PLL Ground	G10	---	---	---
GND044	Core, Platform and PLL Ground	G11	---	---	---
GND045	Core, Platform and PLL Ground	G21	---	---	---
GND046	Core, Platform and PLL Ground	G26	---	---	---
GND047	Core, Platform and PLL Ground	H3	---	---	---
GND048	Core, Platform and PLL Ground	H4	---	---	---
GND049	Core, Platform and PLL Ground	H5	---	---	---
GND050	Core, Platform and PLL Ground	H14	---	---	---
GND051	Core, Platform and PLL Ground	H15	---	---	---
GND052	Core, Platform and PLL Ground	H16	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD15	Supply for cores and platform	M14	---	V_{DD}	---
VDD16	Supply for cores and platform	M16	---	V_{DD}	---
VDD17	Supply for cores and platform	M18	---	V_{DD}	---
VDD18	Supply for cores and platform	M20	---	V_{DD}	---
VDD19	Supply for cores and platform	N9	---	V_{DD}	---
VDD20	Supply for cores and platform	N11	---	V_{DD}	---
VDD21	Supply for cores and platform	N13	---	V_{DD}	---
VDD22	Supply for cores and platform	N15	---	V_{DD}	---
VDD23	Supply for cores and platform	N17	---	V_{DD}	---
VDD24	Supply for cores and platform	N19	---	V_{DD}	---
VDD25	Supply for cores and platform	N21	---	V_{DD}	---
VDD26	Supply for cores and platform	P8	---	V_{DD}	---
VDD27	Supply for cores and platform	P10	---	V_{DD}	---
VDD28	Supply for cores and platform	P12	---	V_{DD}	---
VDD29	Supply for cores and platform	P14	---	V_{DD}	---
VDD30	Supply for cores and platform	P16	---	V_{DD}	---
VDD31	Supply for cores and platform	P18	---	V_{DD}	---
VDD32	Supply for cores and platform	P20	---	V_{DD}	---
VDD33	Supply for cores and platform	R9	---	V_{DD}	---
VDD34	Supply for cores and platform	R11	---	V_{DD}	---
VDD35	Supply for cores and platform	R13	---	V_{DD}	---
VDD36	Supply for cores and platform	R15	---	V_{DD}	---
VDD37	Supply for cores and platform	R17	---	V_{DD}	---
VDD38	Supply for cores and platform	R19	---	V_{DD}	---
VDD39	Supply for cores and platform	T8	---	V_{DD}	---
VDD40	Supply for cores and platform	T10	---	V_{DD}	---
VDD41	Supply for cores and platform	T12	---	V_{DD}	---
VDD42	Supply for cores and platform	T14	---	V_{DD}	---
VDD43	Supply for cores and platform	T16	---	V_{DD}	---
VDD44	Supply for cores and platform	T18	---	V_{DD}	---
VDD45	Supply for cores and platform	T20	---	V_{DD}	---
VDD46	Supply for cores and platform	U9	---	V_{DD}	---
VDD47	Supply for cores and platform	U11	---	V_{DD}	---
VDD48	Supply for cores and platform	U13	---	V_{DD}	---
VDD49	Supply for cores and platform	U15	---	V_{DD}	---
VDD50	Supply for cores and platform	U17	---	V_{DD}	---
VDD51	Supply for cores and platform	U19	---	V_{DD}	---
VDD52	Supply for cores and platform	U21	---	V_{DD}	---

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Characteristic		Symbol	Min	Max	Unit	Notes
DUART1/2, I^2C, DMA, QE, GPIO3, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), USB control (DRVVBUS, PWRFAULT)		DV_{DD}	-0.3	3.63; 1.98	V	9
eSDHC[0-3]/CLK/CMD, GPIO3		EV_{DD}	-0.3	3.63; 1.98	V	—
DDR4 DRAM I/O voltage		$G1V_{DD}$	-0.3	1.32	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers and DIFF_SYSCLK		SV_{DD}	-0.3	1.1	V	—
Pad power supply for SerDes transmitter		XV_{DD}	-0.3	1.48	V	—
Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)		LV_{DD}	-0.3	2.75; 1.98	V	—
Ethernet management interface 2 (EMI2), GPIO2		TV_{DD}	-0.3	2.75; 1.98; 1.32	V	—
USB PHY Transceiver supply voltage		USB_HV_{DD}	-0.3	3.63	V	10
		USB_SDV_{DD}	-0.3	1.1	V	11
		USB_SV_{DD}	-0.3	1.1	V	12
Battery Backed Security Monitor supply		$TA\_BB\_V_{DD}$	-0.3	1.1	V	—
Input voltage	DDR4 DRAM signals	MV_{IN}	-0.3	$G1V_{DD}$ + 0.3	V	2
	SerDes interface and DIFF_SYSCLK	SV_{IN}	-0.3	-0.3 to (SV_{DD} + 0.3)	V	5
	Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)	LV_{IN}	-0.3	LV_{DD} + 0.3	V	4, 5
	IFC, SPI, GIC (IRQ 0/1/2), Tamper_Detect, System control and power management, SYSCLK, DDR_CLK, GPIO3, GPIO2, GPIO1, eSDHC[4-7]/VS/ DAT123_DIR/ DAT0_DIR/CMD_DIR/ SYNC), Debug, JTAG, RTC, POR signals	OV_{IN}	-0.3	OV_{DD} + 0.3	V	3, 5
	eSDHC[0-3]/CLK/ CMD, GPIO3	EV_{IN}	-0.3	EV_{DD} + 0.3	V	5, 6, 7
	DUART1/2, I^2C, DMA, QE, GPIO3, GPIO4, GIC (IRQ	DV_{IN}	-0.3	DV_{DD} + 0.3	V	5, 6, 9

Table continues on the next page...

3.13.1.1 Ethernet management interface 1 (EMI1)

This section describes the electrical characteristics for the EMI1 interface.

The EMI1 interface timing is compatible with IEEE Std 802.3™ clause 22.

3.13.1.1.1 EMI1 DC electrical characteristics

This section describes the DC electrical characteristics for EMI1_MDIO and EMI1_MDC. The pins are available on LV_{DD}. For operating voltages, see the Recommended operating conditions table.

This table provides the EMI1 DC electrical characteristics when operating at LV_{DD} = 2.5 V.

Table 39. EMI1 DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x LVDD	V	2
Input current (V_{IN} = 0 or V_{IN} = LV_{DD})	I_{IN}	-50.0	50.0	µA	3, 4
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.0	-	V	4
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	-	0.4	V	4

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.
4. The symbol LV_{DD} represents the input voltage of the supply referenced in Table 3.

This table provides the EMI1 DC electrical characteristics when operating at LV_{DD} = 1.8 V.

Table 40. EMI1 DC electrical characteristics (LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	-	2
Input low voltage	V_{IL}	-	0.3 x LVDD	-	2
Input current (V_{IN} = 0 or V_{IN} = LV_{DD})	I_{IN}	-50.0	50.0	-	3, 4
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	-	4
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	-	4

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.

Table 60. GIC DC electrical characteristics (DV_{DD} = 1.8 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current (V_{IN} = 0V or V_{IN}= DV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3. 3. The symbol DV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GIC interface operating at LV_{DD} = 2.5 V.

Table 61. GIC DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x LV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3. 3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GIC interface operating at O/LV_{DD} = 1.8 V.

Table 62. GIC DC electrical characteristics (O/LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x O/LV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x O/LV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= O/LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (O/LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (O/LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max O/LV_{IN} values found in Table 3. 3. The symbol O/LV_{IN} represents the input voltage of the supply referenced in Table 3.					

- PCI Express
- Serial ATA (SATA) interface
- SGMII interface
- QSGMII interface
- XFI interface

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.16.4 PCI Express

This section describes the clocking dependencies, as well as the DC and AC electrical specifications for the PCI Express bus.

3.16.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.16.4.2 PCI Express clocking requirements for SD2_REF_CLK*n*_P and SD2_REF_CLK*n*_N

SerDes 2 (SD2_REF_CLK[1:2]_P and SD2_REF_CLK[1:2]_N) may be used for various SerDes PCI Express configurations based on the RCW configuration field SRDS_PRTCL. PCI Express is supported on SerDes 2.

For more information on these specifications, see SerDes reference clocks.

3.16.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.16.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 71. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SV_{DD} = 0.9V/1.0 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Notes: 1. Measured at the package pins with a test load of 50 Ω to GND on each pin. 2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port. 3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground. 4. For recommended operating conditions, see Table 3.						

This table defines the DC characteristics for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 72. PCI Express 3.0 (8 GT/s) differential receiver input DC characteristics (SV_{DD} = 0.9V/1.0 V)[6]

Characteristic	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Generator launch voltage	$V_{RX-LAUNCH-8G}$	—	800	—	mV	Measured at TP1 per PCI Express base spec. rev 3.0
Eye height (-20dB Channel)	$V_{RX-SV-8G}$	25	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-12dB Channel)	$V_{RX-SV-8G}$	50	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-3dB Channel)	$V_{RX-SV-8G}$	200	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver
Notes: 1. Measured at the package pins with a test load of 50 Ω to GND on each pin. 2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port. 3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.						

Table 96. SGMII transmit AC timing specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Notes:						
1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.						
2. See Figure 42 for single frequency sinusoidal jitter measurements.						
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.						
4. For recommended operating conditions, see Table 3.						

3.16.6.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) or at the receiver inputs (SD*n*_RX*n*_P and SD*n*_RX*n*_N) respectively, as shown in this figure.

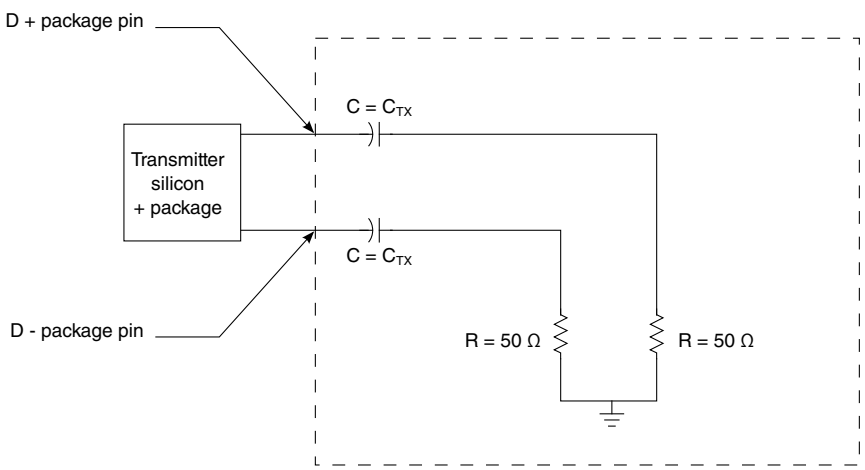

Figure 41. SGMII AC test/measurement load

3.16.6.3.3 SGMII and SGMII 2.5 G receiver AC timing specifications

This table provides the SGMII and SGMII 2.5 G receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 97. SGMII receiver AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2

Table continues on the next page...

3.16.8.3 XFI AC timing specifications

NOTE

The AC specifications do not include RefClk jitter.

This table defines the XFI transmitter AC timing specifications.

Table 104. XFI transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud Rate	T_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter tolerance	T_J	-	-	0.3	UI p-p

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 105. XFI receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	-	96.96	-	ps	-
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s	-
Total non-EQJ jitter	$T_{NON-EQJ}$	-	-	0.45	UI p-p	1
Total jitter tolerance	T_J	-	-	0.65	UI p-p	1, 2

1. The total jitter (TJ) consists of Random Jitter (RJ), Duty Cycle Distortion (DCD), Periodic Jitter (PJ), and Inter-Symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (RJ), and periodic jitter (PJ). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = TJ - ISI = RJ + DCD + PJ.

2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.

This figure shows the sinusoidal jitter tolerance of XFI receiver.

The table below describes the output AC timing specifications for the IFC-GPCM and IFC-GASIC interfaces.

Table 119. Integrated flash controller IFC-GPCM and IFC-GASIC interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	10	-	ns	-
IFC_CLK duty cycle	t_{IBKH}/t_{IBK}	45	55	%	-
Output delay	$t_{IBKLOV1}$	-	1.5	ns	-
Output hold	t_{IBKLOX}	-	-2	ns	1
IFC_CLK[0] to IFC_CLK[m] skew	$t_{IBKSKEW}$	0	±75	ps	-

NOTE:

1. The output hold is negative. This means that output transition happens earlier than the falling edge of IFC_CLK.
2. For recommended operating conditions, see Table 3.

The figure below shows the output AC timing diagram for the IFC-GPCM, IFC-GASIC interface.

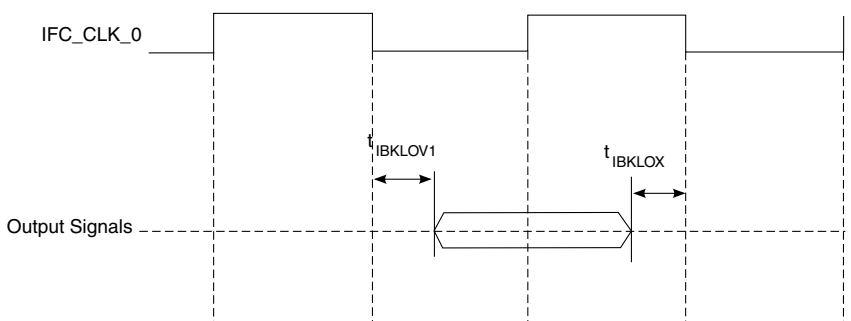

Figure 49. IFC-GPCM, IFC-GASIC signals

3.18.2.3 IFC AC timing specifications (NOR)

The table below describes the input timing specifications for the IFC-NOR interface.

Table 120. Integrated flash controller input timing specifications for NOR mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH2}$	$(2 \times t_{IP\_CLK}) + 2$	-	ns	1
Input hold	$t_{IBIXKH2}$	$(1 \times t_{IP\_CLK}) + 1$	-	ns	1

Notes:

1. t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.
2. For recommended operating conditions, see Table 3.

The figure below shows the AC input timing diagram for input signals for the IFC-NOR interface. Here TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.

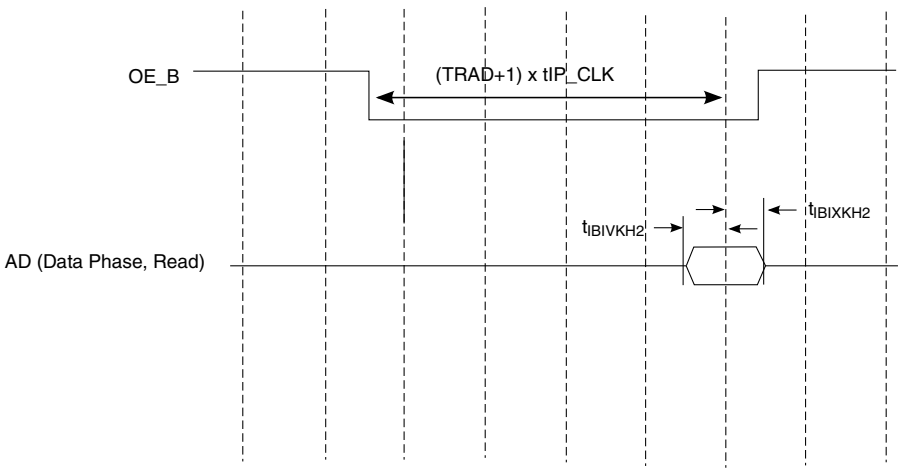

Figure 50. IFC-NOR interface input AC timings

The table below describes the output AC timing specifications of IFC-NOR interface.

Table 121. Integrated flash controller IFC-NOR interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV2}$	-	±1.5	ns	1

NOTE:

1. This effectively means that a signal change may appear anywhere within $\pm t_{IBKLOV2}$ (max) duration, from the point where it's expected to change.

2. For recommended operating conditions, see Table 3.

The figure below shows the AC timing diagram for IFC-NOR interface output signals. The timing specs have been illustrated here by taking timings between two signals, CS_B and OE_B as an example. In a read operation, OE_B is supposed to change the TACO (a programmable delay; see the IFC section of the chip reference manual for more information) time after CS_B. Because of the skew between the signals, OE_B may change anywhere within the window of time defined by tIBKLOV2. This concept applies to other IFC-NOR interface output signals as well. The diagram is an example that shows the skew between any two chronological toggling signals as per the protocol. The list of IFC-NOR output signals is as follows: NRALE, NRAVD_B, NRWE_B, NROE_B, CS_B, AD (Address phase).

Table 125. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
DQS-DQ skew, DQS to last DQ valid, per access	t_{DQSQ}	I	-	1000	ps	Figure 71
Data output to first DQS latching transition	t_{DQSS}	O	0.75 + 150 (ps)	1.25 - 150 (ps)	tCK	Figure 70
Data DQ setup time	t_{DS}	O	1050	-	ps	Figure 70
DQS falling edge to CLK rising - hold time	t_{DSH}	O	0.2 + 150 (ps)	-	tCK	Figure 70
DQS falling edge to CLK rising - setup time	t_{DSS}	O	0.2 + 150 (ps)	-	tCK	Figure 70
Input data valid window	t_{DVW}	I	tDVW = tQH - tDQSQ	-	ns	Figure 71
Busy time for Set Features and Get Features	t_{FEAT}	I	-	FTOCNT	t_{IP_CLK}	Figure 73
Half-clock period	t_{HP}	O	tHP = min(tCKL, tCKH)	-	ns	Figure 71
Interface and Timing Mode Change time	t_{ITC}	I	-	FTOCNT	t_{IP_CLK}	Figure 73
The deviation of a given tCK(abs) from tCK(avg)	t_{JIT}(per)	O	-0.5	0.5	ns	NA
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t_{QH}	I	tQH = tHP - tQHS	-	t_{IP_CLK}	Figure 71
Data hold skew factor	tQHS	I	-	1+150 (ps)		-
Data input cycle to command, address, or data output cycle	t_{RHW}	O	TRHW	-	t_{IP_CLK}	Figure 74
Ready to data input cycle (data only)	t_{RR}	I	TRR	-	t_{IP_CLK}	Figure 73
Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	t_{RST} (raw NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}	Figure 75
Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	t_{RST2} (EZ NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}	Figure 75
CLK rising edge to SR[6] low	t_{WB}	O	TWB - 150 (ps)	TWB + 150 (ps)	t_{IP_CLK}	Figure 75
Command, address or data output cycle to data input cycle	t_{WHR}	O	TWHR	-	t_{IP_CLK}	Figure 76
DQS write preamble	t_{WPRE}	O	1.5	-	tCK	Figure 70
DQS write postamble	t_{WPST}	O	1.5	-	tCK	Figure 70
W/R# low to data input cycle	t_{WRCK}	I	TWRCK - 150 (ps)	TWRCK + 150 (ps)	t_{IP_CLK}	Figure 71

Table continues on the next page...

Table 134. HDLC AC timing specifications

Parameter	Symbol	Min	Max	Unit
Internal clock delay	t_{HIKHOV}	0.0	5.5	-
External clock delay	t_{HEKHOV}	1.0	13.0	ns
Internal clock high impedance	t_{HIKHOX}	0.0	5.5	ns
External clock high impedance	t_{HEKHOX}	1.0	8.0	ns
Internal clock input setup time	t_{HIIVKH}	12.6	-	ns
External clock input setup time	t_{HEIVKH}	4.0	-	ns
Internal clock input hold time	t_{HIIXKH}	0.0	-	ns
External clock input hold time	t_{HEIXKH}	1.0	-	ns

This table provides the input and output AC timing specifications for the synchronous UART protocols.

Table 135. Synchronous UART AC timing specifications

Parameter	Symbol	Min	Max	Unit
Internal clock delay	t_{HIKHOV}	0.0	11.0	-
External clock delay	t_{HEKHOV}	1.0	14.0	ns
Internal clock high impedance	t_{HIKHOX}	0.0	11.0	ns
External clock high impedance	t_{HEKHOX}	1.0	14.0	ns
Internal clock input setup time	t_{HIIVKH}	10.0	-	ns
External clock input setup time	t_{HEIVKH}	8.0	-	ns
Internal clock input hold time	t_{HIIXKH}	0.0	-	ns
External clock input hold time	t_{HEIXKH}	1.0	-	ns

This figure shows the AC test load for the HDLC interface.

The table below lists the valid VID fuse values that will be programmed at the factory for this chip.

Table 148. Fuse Status Register (DCFG_CCSR_FUSESR)

Binary value of DA_V / DA_ALT_V	V_{DD} voltage
00000b	1.025 V (default)
00001b	0.9875 V
00010b	0.9750 V
01000b	0.9000 V
10000b	1.0000 V
10001b	1.0125 V
10010b	1.0250 V
All other values	Reserved

For additional information on VID, see the chip reference manual.

5 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 149. Package thermal characteristics

Rating	Board	Symbol	Value	Unit	Notes
Junction-to-ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	23.5	°C/W	1
Junction-to-ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	15.2	°C/W	1
Junction-to-ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	14.8	°C/W	1
Junction-to-ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	10.1	°C/W	1
Junction-to-board	-	$R_{\Theta JB}$	4.4	°C/W	2
Junction-to-case (top)	-	$R_{\Theta JCtop}$	0.56	°C/W	3
Junction-to-lid-top	-	$R_{\Theta JClid}$	0.20	°C/W	4

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-2A and JESD51-6. Thermal test board meets JEDEC specification for this package (JESD51-9).

2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4. Junction-to-lid-top thermal resistance is determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance layer between the package and cold plate.

5. See Thermal management information for additional details.

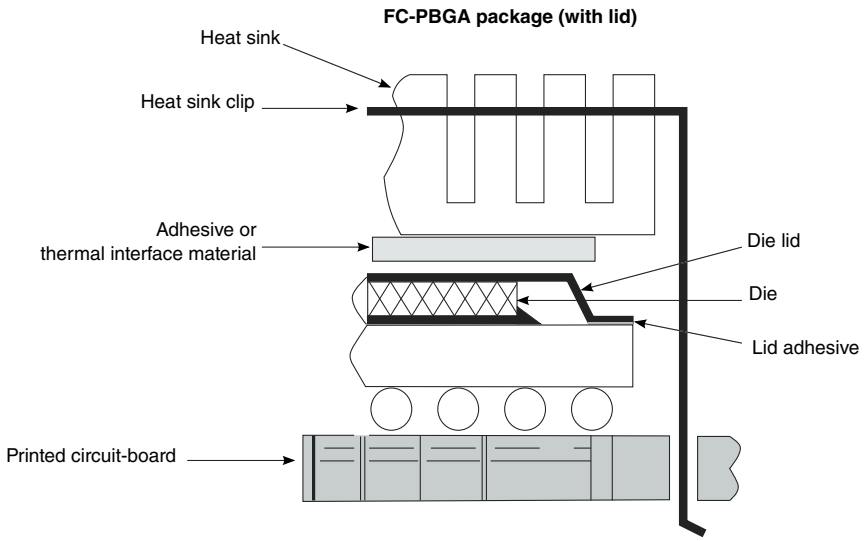

Figure 95. Package exploded, cross-sectional view-FC-PBGA (with lid)

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

5.3.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure shows the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

9 Revision history

This table summarizes revisions to this document.

Table 151. Revision history

Revision	Date	Description
0	01/2018	Initial release.