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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	8 Core, 64-Bit
Speed	1.6GHz
Co-Processors/DSP	-
RAM Controllers	DDR4
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	10GbE (2), 1GbE (8)
SATA	SATA 6Gbps (1)
USB	USB 3.0 (2) + PHY
Voltage - I/O	-
Operating Temperature	0°C ~ 105°C
Security Features	Secure Boot, TrustZone®
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088asn7q1a

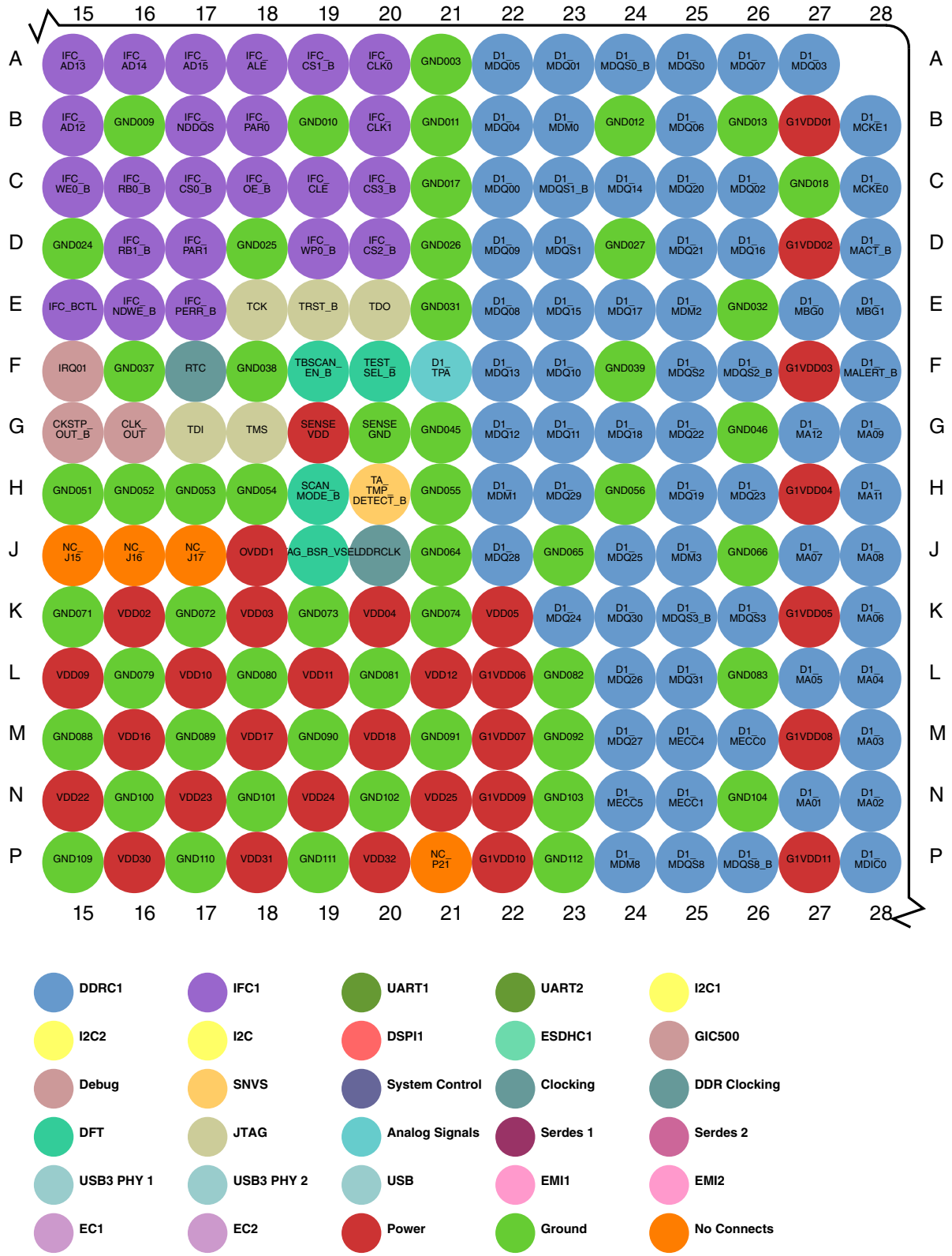

Figure 4. Detail B

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD18	DDR supply	AA27	---	$G1V_{DD}$	---
G1VDD19	DDR supply	AC27	---	$G1V_{DD}$	---
G1VDD20	DDR supply	AE27	---	$G1V_{DD}$	---
G1VDD21	DDR supply	AG27	---	$G1V_{DD}$	---
G1VDD22	DDR supply	AH27	---	$G1V_{DD}$	---
SVDD1	SerDes transceiver supply	W7	---	SV_{DD}	---
SVDD2	SerDes transceiver supply	W8	---	SV_{DD}	---
SVDD3	SerDes transceiver supply	W9	---	SV_{DD}	---
SVDD4	SerDes transceiver supply	W10	---	SV_{DD}	---
SVDD5	SerDes transceiver supply	W13	---	SV_{DD}	---
SVDD6	SerDes transceiver supply	W14	---	SV_{DD}	---
SVDD7	SerDes transceiver supply	W15	---	SV_{DD}	---
SVDD8	SerDes transceiver supply	W16	---	SV_{DD}	---
XVDD1	SerDes transceiver supply	AC7	---	XV_{DD}	---
XVDD2	SerDes transceiver supply	AC9	---	XV_{DD}	---
XVDD3	SerDes transceiver supply	AC12	---	XV_{DD}	---
XVDD4	SerDes transceiver supply	AC14	---	XV_{DD}	---
XVDD5	SerDes transceiver supply	AC17	---	XV_{DD}	---
XVDD6	SerDes transceiver supply	AC20	---	XV_{DD}	---
FA_VL	Reserved	AB21	---	FA_VL	---
PROG_MTR	Reserved	F13	---	PROG_MTR	---
TA_PROG_SFP	SFP Fuse Programming Override supply	G13	---	TA_PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	G8	---	TH_V_{DD}	---
VDD01	Supply for cores and platform	K14	---	V_{DD}	---
VDD02	Supply for cores and platform	K16	---	V_{DD}	---
VDD03	Supply for cores and platform	K18	---	V_{DD}	---
VDD04	Supply for cores and platform	K20	---	V_{DD}	---
VDD05	Supply for cores and platform	K22	---	V_{DD}	---
VDD06	Supply for cores and platform	L9	---	V_{DD}	---
VDD07	Supply for cores and platform	L11	---	V_{DD}	---
VDD08	Supply for cores and platform	L13	---	V_{DD}	---
VDD09	Supply for cores and platform	L15	---	V_{DD}	---
VDD10	Supply for cores and platform	L17	---	V_{DD}	---
VDD11	Supply for cores and platform	L19	---	V_{DD}	---
VDD12	Supply for cores and platform	L21	---	V_{DD}	---
VDD13	Supply for cores and platform	M10	---	V_{DD}	---
VDD14	Supply for cores and platform	M12	---	V_{DD}	---

Table continues on the next page...

3.7.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content.

The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement.

Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in this table are observed.

Table 14. Spread-spectrum clock source recommendations[3]

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Notes:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 13.

2. Maximum spread-spectrum frequency may not result in exceeding any maximum operating frequency of the device.

3. At recommended operating conditions with OVDD = 1.8 V. See Table 3.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded, regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should use only down-spreading to avoid violating the stated limits.

3.7.3 USB 3.0 reference clock requirements

There are two options for the reference clock of USB PHY: SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B. This table provides the additional requirements when SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B is used as USB REFCLK. The 100 MHz reference clock is also required with the following requirements.

Table 15. USB AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Reference clock frequency-offset	F_{REF_OFFSET}	-300.0	300.0	ppm	-
Reference clock random jitter (RMS)	$JRMS_{REF\_CLK}$	-	3.0	ps	1, 2
Reference clock deterministic jitter	DJ_{REF_CLK}	-	150.0	ps	3
Duty cycle	DC_{REF_CLK}	40.0	60.0	%	-
1. 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz.					
2. The peak-to-peak Rj specification is calculated at 14.069 times the RJ_{RMS} for 10^{-12} BER.					
3. DJ across all frequencies.					

3.7.4 Real-time clock timing

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the time base unit of the core; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC pin may be grounded if not needed.

3.7.5 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC electrical characteristics with LV_{DD} = 1.8 V.

Table 16. EC*n*_GTX_CLK125 DC electrical characteristics (LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	—	V	2
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	—	± 50	μA	3
Notes:						
1. For recommended operating conditions, see Table 3.						
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 3.						
3. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 3.						

This table provides the Ethernet gigabit reference clock DC electrical characteristics with LV_{DD} = 2.5 V.

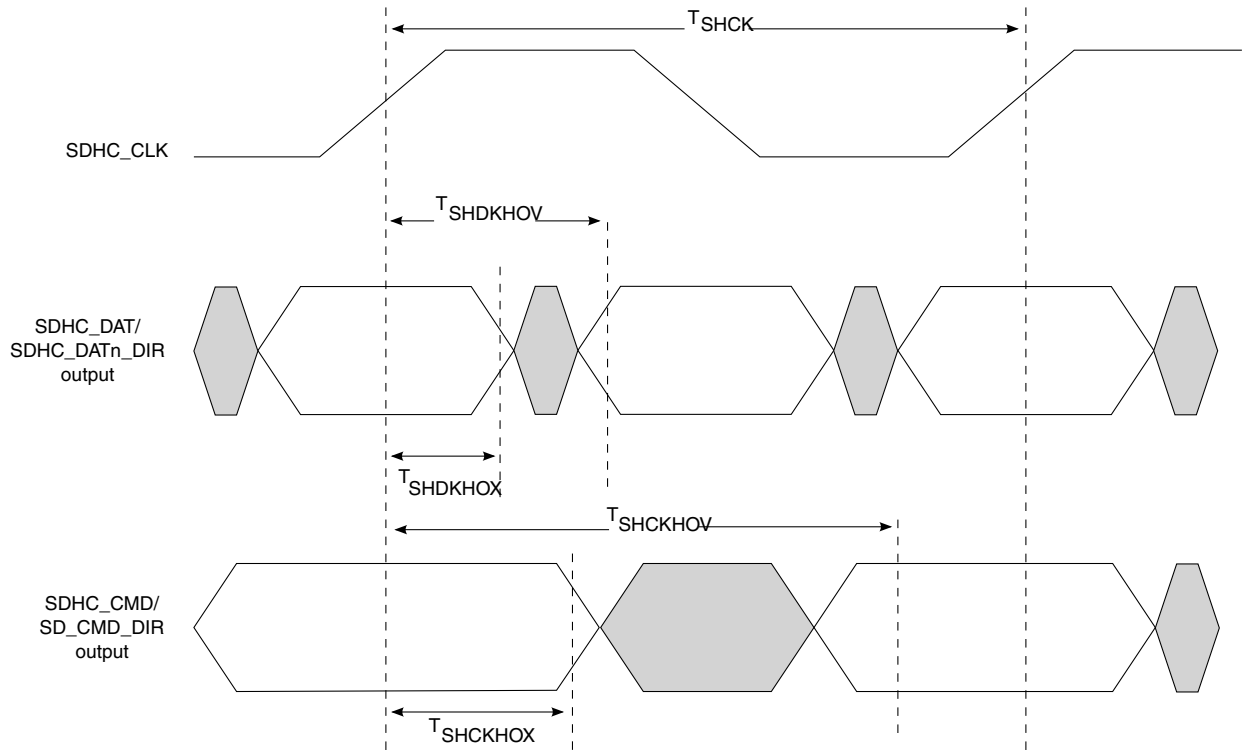

Figure 21. eSDHC DDR50/DDR mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode.

Table 38. eSDHC AC timing specifications (SDR104/eMMC HS200)

Parameter		Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency	SD/SDIO SDR104 mode	f_{SHCK}	-	167	MHz	-
	eMMC HS200 mode			167		-
SDHC_CLK clock rise and fall times		t_{SHCKR}/t_{SHCKF}	-	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOX}	1.58	-	ns	1
	eMMC HS200 mode		1.6			
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOV}	-	3.94	ns	1
	eMMC HS200 mode			3.92		
Input data window (UI)	SD/SDIO SDR104 mode	t_{SHIDV}	0.5	-	Unit Interval	1
	eMMC HS200 mode		0.475			

Notes:

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.
2. For recommended operating conditions, see Table 3.

This figure provides the eSDHC SDR104/HS200 mode timing diagram.

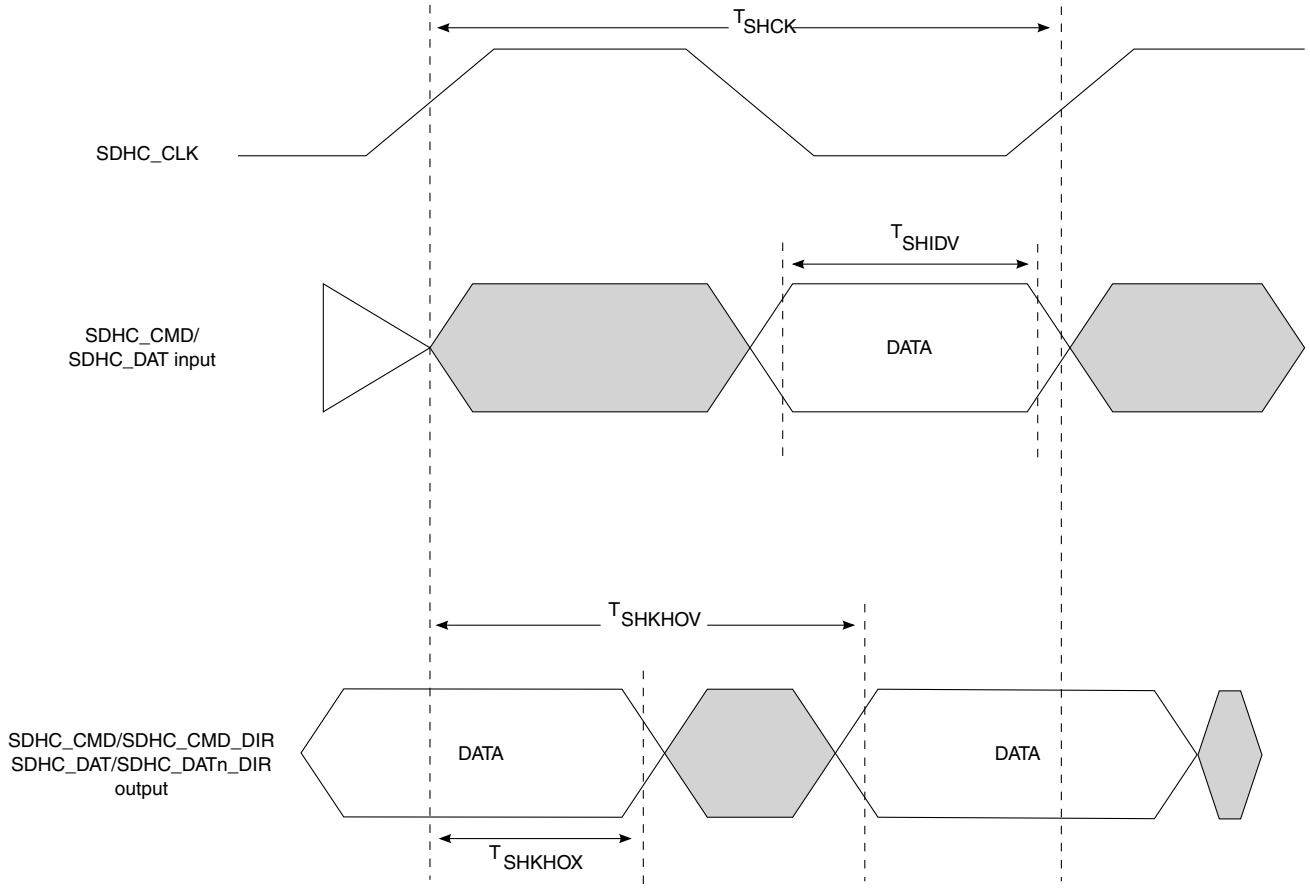

Figure 22. eSDHC SDR104/HS200 mode timing diagram

3.13 Ethernet interface (EMI, RGMII, and IEEE Std 1588™)

This section describes the DC and AC electrical characteristics for the Ethernet controller, Ethernet management, RGMII, and IEEE Std 1588 interfaces.

3.13.1 Ethernet management interface (EMI)

This section describes the electrical characteristics for the Ethernet management interface (EMI).

The EMI1 and EMI2 interface timings are compatible with IEEE Std 802.3™ clauses 22 and 45, respectively.

Table 50. RGMII DC electrical characteristics (LV_{DD} = 1.8 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current (V_{IN}=0V or V_{IN}=LV_{DD})	I_{IN}	-50.0	50.0	µA	3, 4
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	3
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	3

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.

3. The symbol LV_{DD} represents the input voltage of the supply referenced in Table 3.

4. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.

3.13.3.2 RGMII AC timing specifications

This table provides the AC timing specifications for the RGMII interface.

Table 51. RGMII AC timing specifications[7]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-400	0.0	600	ps	1
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	-	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40.0	50.0	60.0	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45.0	50.0	55.0	%	-
Rise time (20%-80%) L1/ LV_{DD}=2.5V	t_{RGTR}	-	-	0.75	ns	5, 6
Rise time (20%-80%) L1/ LV_{DD}=1.8V	t_{RGTR}	-	-	0.54	ns	5, 6
Fall time (20%-80%) L1/LV_{DD}=2.5V	t_{RGTF}	-	-	0.75	ns	5, 6
Fall time (20%-80%) L1/LV_{DD}=1.8V	t_{RGTF}	-	-	0.54	ns	5, 6

1. The frequency of ECn_RX_CLK (input) should not exceed the frequency of ECn_GTX_CLK (output) by more than 300 ppm.

2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three tRGT of the lowest speed transitioned between.

5. Applies to inputs and outputs.

6. The system/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

Table 54. GPIO DC electrical characteristics (D/E/TV_{DD} = 1.8 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	-	0.3 x D/E/TV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (D/E/TV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (D/E/TV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN}/EV_{IN}/TV_{IN} values found in Table 3.					
3. The symbol DV_{IN}/EV_{IN}/TV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at LV_{DD} = 2.5 V.

Table 55. GPIO DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x LVDD	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.					
3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at O/LV_{DD} = 1.8 V.

Table 56. GPIO DC electrical characteristics (O/LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x O/LVDD	-	V	2
Input low voltage	V_{IL}	-	0.3 x O/LVDD	V	2
Input current (V_{IN} = 0V or V_{IN}= O/LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (O/LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (O/LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3.					

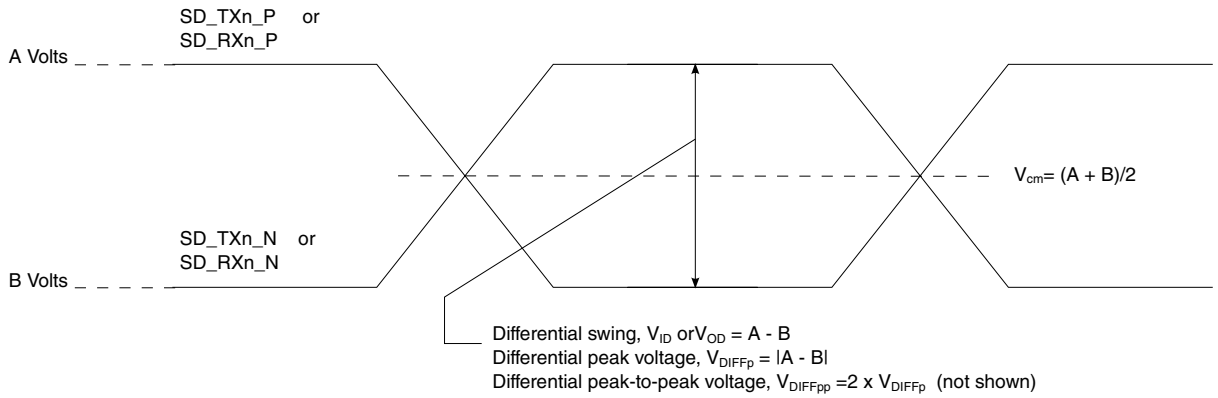

Figure 29. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as described in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred to as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD\_TXn\_P}$ - $V_{SD\_TXn\_N}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing)

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD\_RXn\_P}$- $V_{SD\_RXn\_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |A - B| volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 x V_{DIFFp} = 2 x |(A - B)| volts, which is twice the differential swing in amplitude, or twice the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p}$ = 2 x |V_{OD}|.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example)

within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 34 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn\_P} + V_{SD\_TXn\_N}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.16.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal phase-locked loop (PLL) whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD*n*_REF_CLK[1:2]_P and SD*n*_REF_CLK[1:2]_N.

SerDes may be used for various combinations of the following IP block based on the RCW Configuration field SRDS_PRTCLn:

- SGMII (1.25 Gbaud or 3.125 Gbaud), QSGMII (5 Gbps)
- XFI (10.3125 Gb/s)
- PCIe (2.5, 5, and 8 GT/s)
- SATA (1.5, 3.0, and 6.0 Gbps)

The following sections describe the SerDes reference clock requirements and provide application information.

- PCI Express
- Serial ATA (SATA) interface
- SGMII interface
- QSGMII interface
- XFI interface

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.16.4 PCI Express

This section describes the clocking dependencies, as well as the DC and AC electrical specifications for the PCI Express bus.

3.16.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.16.4.2 PCI Express clocking requirements for SD2_REF_CLK*n*_P and SD2_REF_CLK*n*_N

SerDes 2 (SD2_REF_CLK[1:2]_P and SD2_REF_CLK[1:2]_N) may be used for various SerDes PCI Express configurations based on the RCW configuration field SRDS_PRTCL. PCI Express is supported on SerDes 2.

For more information on these specifications, see SerDes reference clocks.

3.16.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.16.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 82. Gen1i/1m 1.5 G receiver input DC specifications (SV_{DD} = 0.9 V / 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 3.

This table provides the Gen2i/2m or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 83. Gen2i/2m 3 G receiver input DC specifications (SV_{DD} = 0.9 V / 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 3.

This table provides the Gen 3i differential receiver input DC characteristics for the SATA interface.

Table 84. Gen 3i receiver input DC specifications (SV_{DD} = 0.9 V / 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	1000	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	—	75	120	200	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 3.

3.16.5.2 SATA AC timing specifications

This section describes the SATA AC timing specifications.

Table 113. 10GBase-KR receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Total jitter tolerance	R_{TJ}	-	-	Per IEEE Std 802.3ap-2007, Annex 69a.	UI p-p
Random jitter	R_{RJ}	-	-	0.13	UI p-p
Sinusoidal jitter (maximum)	R_{SJ-max}	-	-	0.115	UI p-p
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p

3.17 I²C interface

This section describes the DC and AC electrical characteristics for the I²C interface.

3.17.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interface when operating at DV_{DD} = 3.3 V.

Table 114. I²C DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	2
Output low voltage (DV_{DD} = min, IOL = 3 mA, DV_{DD} > 2V)	V_{OL}	-	0.4	V	3
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	4
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} (min) and 0.9 x DV_{DD} (max))	I_I	-50.0	50.0	µA	5
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.

3. The output voltage (open drain or open collector) condition = 3 mA sink current.

4. See the chip reference manual for information about the digital filter used.

5. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.

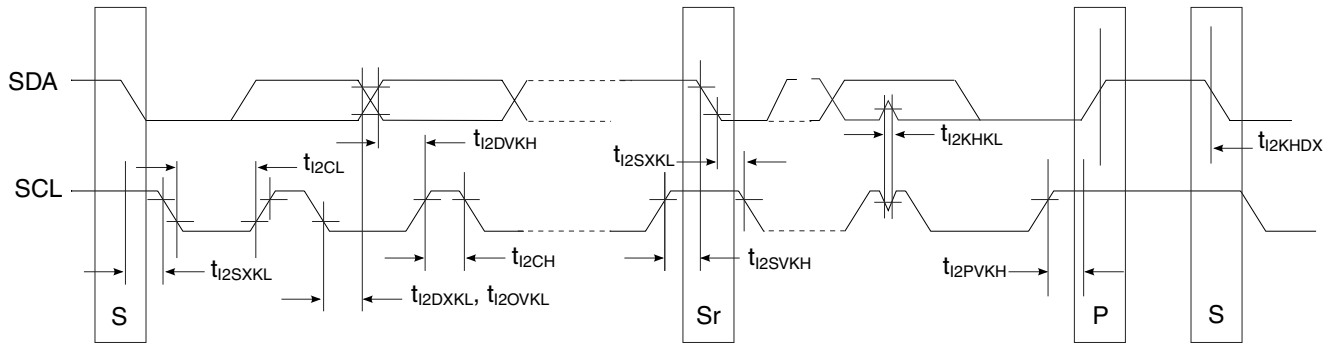

Figure 46. I²C bus AC timing diagram

3.18 Integrated Flash Controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.18.1 Integrated Flash Controller DC electrical characteristics

Table below provides the DC electrical characteristics for the integrated flash controller when operating at OV_{DD} = 1.8 V.

Table 117. Integrated Flash Controller DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.6	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.32	V	-

NOTE:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

3.18.2 Integrated Flash Controller AC timing specifications

This section describes the AC timing specifications for the integrated flash controller.

3.18.2.1 Test condition

The figure below provides the AC test load for the integrated flash controller.

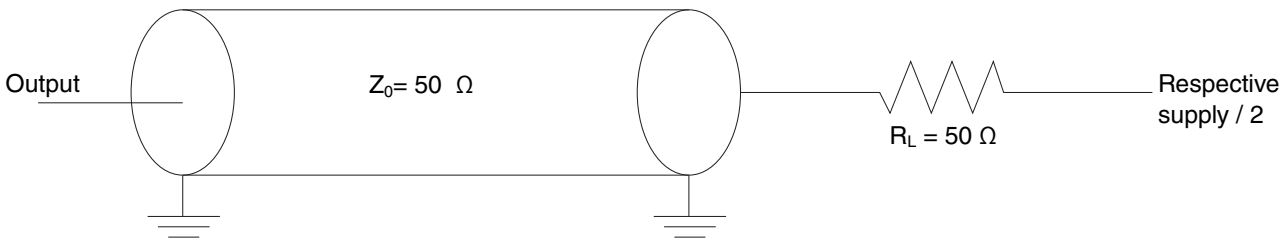

Figure 47. Integrated Flash Controller AC test load

3.18.2.2 IFC AC timing specifications (GPCM/GASIC)

The table below describes the input AC timing specifications for the IFC-GPCM and IFC-GASIC interface.

Table 118. Integrated flash controller input timing specifications for GPCM and GASIC mode (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH1}$	4	-	ns	-
Input hold	$t_{IBIXKH1}$	1	-	ns	-

NOTE:

1. For recommended operating conditions, see Table 3.

The figure below shows the input AC timing diagram for the IFC-GPCM, IFC-GASIC interface.

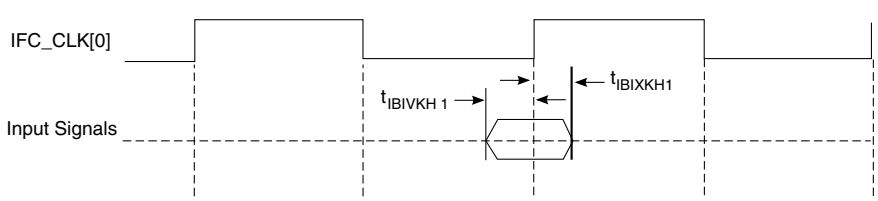

Figure 48. IFC-GPCM, IFC-GASIC input AC timing specifictions

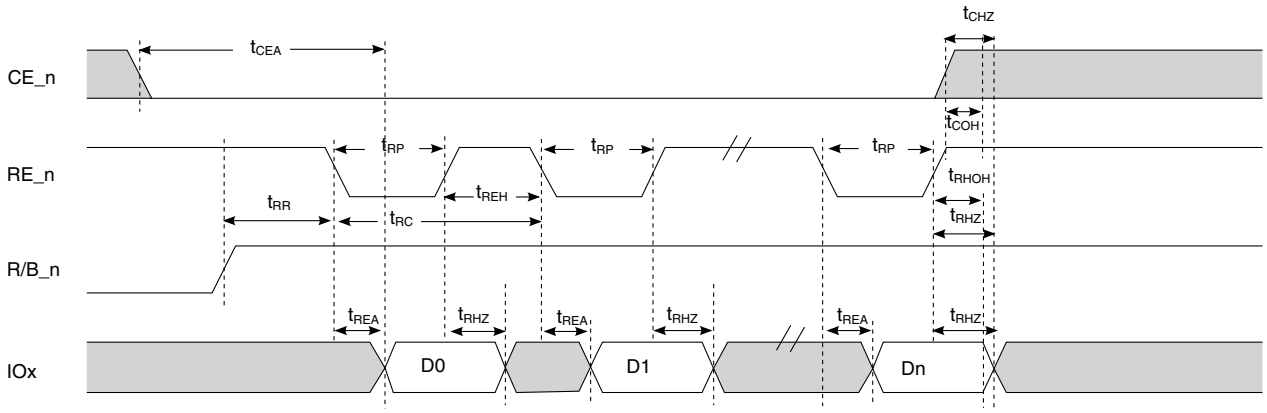

Figure 57. Data input cycle timings

This figure shows the t_{CLR} timings.

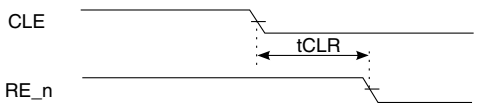

Figure 58. t_{CLR} timings

This figure shows the t_{WB}, t_{FEAT}, t_{ITC}, and t_{RR} timings.

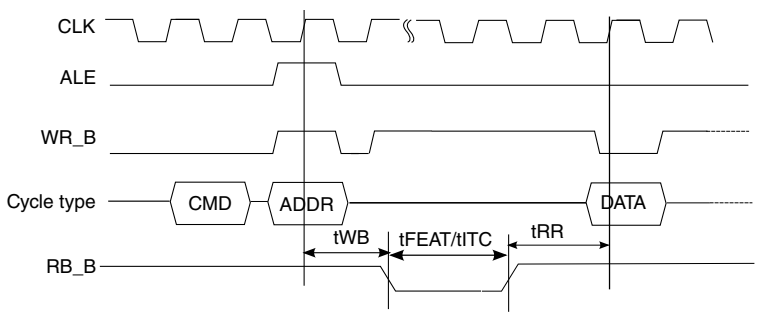

Figure 59. t_{WB}, t_{FEAT}, t_{ITC}, and t_{RR} timings

This figure shows the read status timings.

Table 137. TDM/SI DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.65 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.35 x DVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	µA	3
Output high voltage (DV_{DD}=min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (DV_{DD}=min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.

3. The symbol V_{IN} represents the input voltage of the supply referenced in Table 3.

3.21.2.2 TDM/SI AC timing specifications

NOTE

Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This table provides the AC timing specifications for the TDM/SI interface.

Table 138. TDM/SI AC timing specifications

Parameter	Symbol	Min	Max	Unit
External clock delay	t_{SEKHOV}	2.0	11.0	ns
External clock high impedance	t_{SEKHOX}	2.0	10.0	ns
External clock input setup time	t_{SEIVKH}	5.0	-	ns
External clock input hold time	t_{SEIXKH}	2.0	-	ns

This figure shows the AC test load for the TDM/SI.

Table 139. SPI DC electrical characteristics (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.

2. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in the Recommended Operating Conditions table.

3. Note that the symbol OV_{IN} represents the input voltage of the supply referenced in the Recommended Operating Conditions table.

3.22.2 SPI AC timing specifications

This table provides the AC timing specifications for the SPI interface when operating with a single master device.

Table 140. SPI AC timing specifications

Parameter	Symbol	Min	Condition	Max	Unit
SCK clock pulse width	t_{SDC}	40	-	60	%
CS to SCK delay	t_{CSC}	16.0	Master	-	ns
After SCK delay	t_{ASC}	16.0	Master	-	ns
Slave access time (SS active to SOUT driven)	t_{A}	-	Slave	15	ns
Slave disable time (SS inactive to SOUT High-Z or invalid)	t_{DI}	-	Slave	10	ns
Data setup time for inputs	t_{NIIVKH}	9.0	Master	-	ns
Data setup time for inputs	t_{NEIVKH}	8.0	Slave	-	ns
Data hold time for inputs	t_{NIIXKH}	0.0	Master	-	ns
Data hold time for inputs	t_{NEIXKH}	2.0	Slave	-	ns
Data valid (after SCK edge) for outputs	t_{NIKHOV}	-	Master	5.0	ns

Table continues on the next page...

Table 143. USB 3.0 receiver DC electrical characteristics[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
LFPS detect threshold	$V_{TRX-IDLE-DET-DC-DIFFpp}$	100.0	-	300.0	mV	2
1. For recommended operating conditions, see Table 3.						
2. Below the minimum is noise. Must wake up above the maximum.						

3.23.1.2 USB 3.0 AC timing specifications

This table provides the USB 3.0 transmitter AC timing specifications at package pins.

Table 144. USB 3.0 transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Speed	-	-	5.0	-	Gb/s	-
Transmitter eye	T_{TX-EYE}	0.625	-	-	UI	-
Unit Interval	UI	199.94	-	200.06	ps	UI does not account for SSC-caused variations.
AC coupling capacitor	AC_{CAP}	75.0	-	200.0	nF	-

This table provides the USB 3.0 receiver AC timing specifications at receiver package pins.

Table 145. USB 3.0 receiver AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Unit Interval	UI	199.94	200.06	ps	UI does not account for SSC-caused variations.

3.23.1.3 USB 3.0 LFPS specifications

This table provides the key LFPS electrical specifications at the transmitter.

Table 146. LFPS electrical specifications at the transmitter

Parameter	Symbol	Min	Max	Unit	Notes
Period	t_{Period}	20.0	100.0	ns	-

Table continues on the next page...

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.
7. Pin 1 thru hole shall be centered within foot area.
8. 23.2 mm maximum package assembly (lid + laminate) X and Y.

7 Security fuse processor

This chip implements trust architecture 3.0, which supports capabilities such as secure boot. Use of the trust architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8 V to the TA_PROG_SFP pin per Power sequencing. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times, TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Power sequencing. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

NOTE

Users not implementing the QorIQ platform's trust architecture features should connect TA_PROG_SFP to GND.

8 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

8.1 Part numbering nomenclature

This table provides the NXP Layerscape platform part numbering nomenclature.