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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	8 Core, 64-Bit
Speed	1.2GHz
Co-Processors/DSP	-
RAM Controllers	DDR4
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	10GbE (2), 1GbE (8)
SATA	SATA 6Gbps (1)
USB	USB 3.0 (2) + PHY
Voltage - I/O	-
Operating Temperature	-40°C ~ 105°C
Security Features	Secure Boot, TrustZone®
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088axe7mqa

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD2_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AE13	I	SV_{DD}	---
SD2_REF_CLK1_P	SerDes PLL 1 Reference Clock	AD13	I	SV_{DD}	---
SD2_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AB19	I	SV_{DD}	---
SD2_REF_CLK2_P	SerDes PLL 2 Reference Clock	AB18	I	SV_{DD}	---
SD2_RX0_N	SerDes Receive Data (negative)	AH15	I	SV_{DD}	---
SD2_RX0_P	SerDes Receive Data (positive)	AG15	I	SV_{DD}	---
SD2_RX1_N	SerDes Receive Data (negative)	AH16	I	SV_{DD}	---
SD2_RX1_P	SerDes Receive Data (positive)	AG16	I	SV_{DD}	---
SD2_RX2_N	SerDes Receive Data (negative)	AH18	I	SV_{DD}	---
SD2_RX2_P	SerDes Receive Data (positive)	AG18	I	SV_{DD}	---
SD2_RX3_N	SerDes Receive Data (negative)	AH19	I	SV_{DD}	---
SD2_RX3_P	SerDes Receive Data (positive)	AG19	I	SV_{DD}	---
SD2_TX0_N	SerDes Transmit Data (negative)	AE15	O	XV_{DD}	---
SD2_TX0_P	SerDes Transmit Data (positive)	AD15	O	XV_{DD}	---
SD2_TX1_N	SerDes Transmit Data (negative)	AE16	O	XV_{DD}	---
SD2_TX1_P	SerDes Transmit Data (positive)	AD16	O	XV_{DD}	---
SD2_TX2_N	SerDes Transmit Data (negative)	AE18	O	XV_{DD}	---
SD2_TX2_P	SerDes Transmit Data (positive)	AD18	O	XV_{DD}	---
SD2_TX3_N	SerDes Transmit Data (negative)	AE19	O	XV_{DD}	---
SD2_TX3_P	SerDes Transmit Data (positive)	AD19	O	XV_{DD}	---
USB PHY 1					
USB1_D_M	USB PHY HS Data (-)	E6	IO	-	---
USB1_D_P	USB PHY HS Data (+)	F6	IO	-	---
USB1_ID	USB PHY ID Detect	F5	I	-	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND119	Core, Platform and PLL Ground	R18	---	---	---
GND120	Core, Platform and PLL Ground	R20	---	---	---
GND121	Core, Platform and PLL Ground	R23	---	---	---
GND122	Core, Platform and PLL Ground	R26	---	---	---
GND123	Core, Platform and PLL Ground	T2	---	---	---
GND124	Core, Platform and PLL Ground	T4	---	---	---
GND125	Core, Platform and PLL Ground	T6	---	---	---
GND126	Core, Platform and PLL Ground	T9	---	---	---
GND127	Core, Platform and PLL Ground	T11	---	---	---
GND128	Core, Platform and PLL Ground	T13	---	---	---
GND129	Core, Platform and PLL Ground	T15	---	---	---
GND130	Core, Platform and PLL Ground	T17	---	---	---
GND131	Core, Platform and PLL Ground	T19	---	---	---
GND132	Core, Platform and PLL Ground	T21	---	---	---
GND133	Core, Platform and PLL Ground	T23	---	---	---
GND134	Core, Platform and PLL Ground	T26	---	---	---
GND135	Core, Platform and PLL Ground	U6	---	---	---
GND136	Core, Platform and PLL Ground	U8	---	---	---
GND137	Core, Platform and PLL Ground	U10	---	---	---
GND138	Core, Platform and PLL Ground	U12	---	---	---
GND139	Core, Platform and PLL Ground	U14	---	---	---
GND140	Core, Platform and PLL Ground	U16	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND46	SerDes core logic, transceiver, and PLL ground	AE20	---	---	18
SD_GND47	SerDes core logic, transceiver, and PLL ground	AF6	---	---	18
SD_GND48	SerDes core logic, transceiver, and PLL ground	AF7	---	---	18
SD_GND49	SerDes core logic, transceiver, and PLL ground	AF8	---	---	18
SD_GND50	SerDes core logic, transceiver, and PLL ground	AF9	---	---	18
SD_GND51	SerDes core logic, transceiver, and PLL ground	AF10	---	---	18
SD_GND52	SerDes core logic, transceiver, and PLL ground	AF11	---	---	18
SD_GND53	SerDes core logic, transceiver, and PLL ground	AF15	---	---	18
SD_GND54	SerDes core logic, transceiver, and PLL ground	AF16	---	---	18
SD_GND55	SerDes core logic, transceiver, and PLL ground	AF17	---	---	18
SD_GND56	SerDes core logic, transceiver, and PLL ground	AF18	---	---	18
SD_GND57	SerDes core logic, transceiver, and PLL ground	AF19	---	---	18
SD_GND58	SerDes core logic, transceiver, and PLL ground	AG5	---	---	18
SD_GND59	SerDes core logic, transceiver, and PLL ground	AG7	---	---	18
SD_GND60	SerDes core logic, transceiver, and PLL ground	AG9	---	---	18
SD_GND61	SerDes core logic, transceiver, and PLL ground	AG12	---	---	18
SD_GND62	SerDes core logic, transceiver, and PLL ground	AG14	---	---	18
SD_GND63	SerDes core logic, transceiver, and PLL ground	AG17	---	---	18
SD_GND64	SerDes core logic, transceiver, and PLL ground	AG20	---	---	18
SD_GND65	SerDes core logic, transceiver, and PLL ground	AH5	---	---	18
SD_GND66	SerDes core logic, transceiver, and PLL ground	AH7	---	---	18
SD_GND67	SerDes core logic, transceiver, and PLL ground	AH9	---	---	18

Table continues on the next page...

Table 26. DDR4 SDRAM interface DC electrical characteristics (GV_{DD} = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
6. Internal Vref for data bus must be set to 0.7 x GV_{DD}.					
7. For recommended operating conditions, see Table 3.					

3.10.2 DDR4 SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR4 memories. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.10.2.1 DDR4 SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 27. DDR4 SDRAM interface input AC timing specifications (GV_{DD} = 1.2 V ± 5%)$_1$

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage ≤ 2133 MT/s data rate	V_{ILAC}	—	0.7 x GV_{DD} - 0.175	V	—
AC input high voltage ≤ 2133 MT/s data rate	V_{IHAC}	0.7 x GV_{DD} + 0.175	—	V	—
Note: 1. For recommended operating conditions, see Table 3.					

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 28. DDR4 SDRAM interface input AC timing specifications (GV_{DD} = 1.2 V ± 5% for DDR4)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS-MDQ/MECC	t_{CISKEW}	—	—	ps	1
2100 MT/s data rate		-80	80		
1800 MT/s data rate		-93	93		
1600 MT/s data rate		-112	112		
1333 MT/s data rate		-125	125		
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}	—	—	ps	2
2100 MT/s data rate		-154	154		
1800 MT/s data rate		-175	175		

Table continues on the next page...

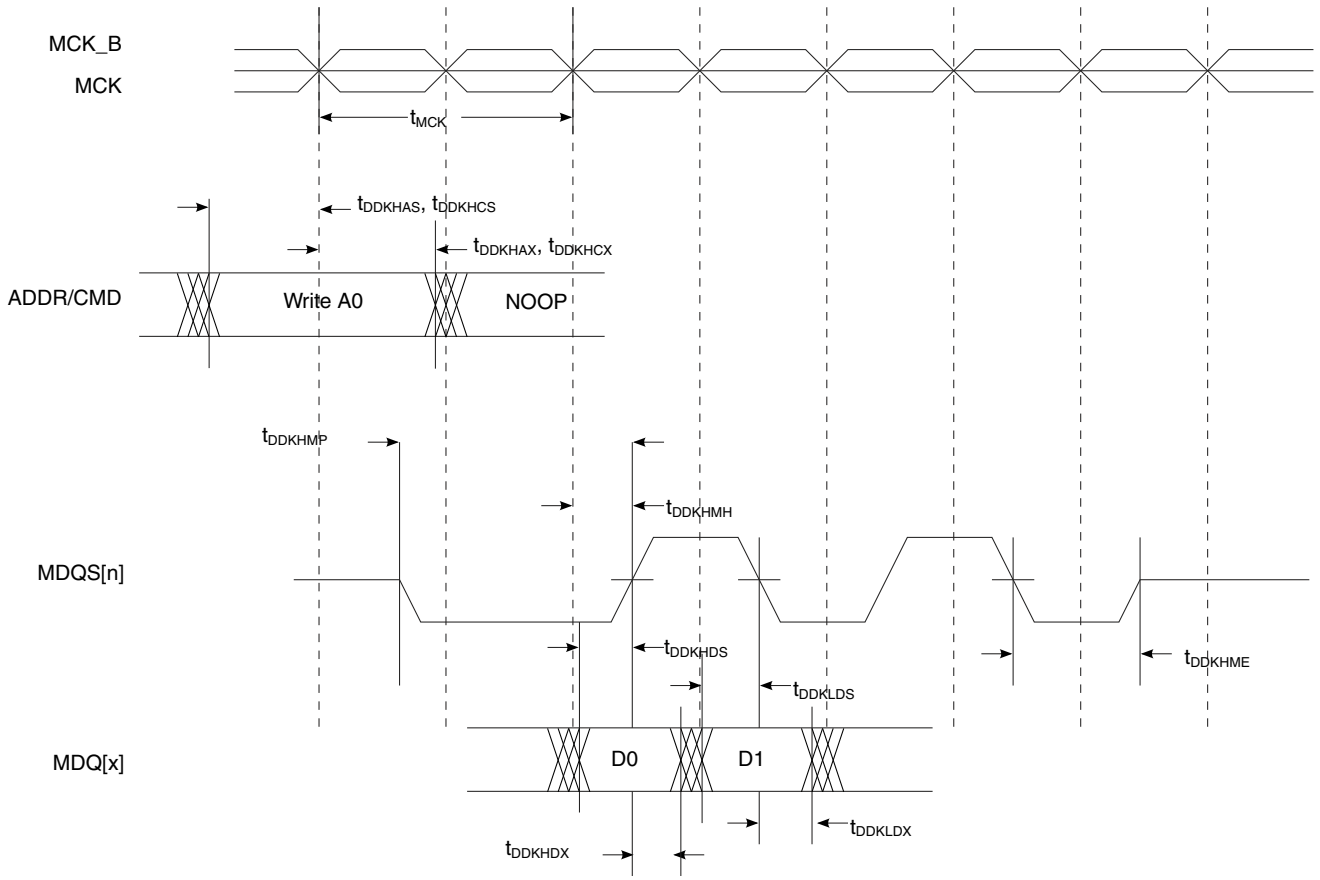


Figure 13. DDR4 output timing diagram

3.11 Dual universal asynchronous receiver/transmitter (DUART) interface

This section describes the DC and AC electrical characteristics for the DUART interface.

3.11.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface when operating at DV_{DD} = 3.3 V.

Table 30. DUART DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x DVDD	V	2

Table continues on the next page...

3.12 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.12.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 33. eSDHC interface DC electrical characteristics (E/DV_{DD}=3.3 V)[3]

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x E/DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.25 x E/DV_{DD}	V	1
Output high voltage (I_{OH} = -100 µA at E/DV_{DD} min)	V_{OH}	0.75 x E/DV_{DD}	-	V	-
Output low voltage (I_{OL} = 100 µA at E/DV_{DD} min)	V_{OL}	-	0.125 x E/DV_{DD}	V	-
Output high voltage (I_{OH} = -100 µA)	V_{OH}	E/DV_{DD} - 0.2	-	V	2
Output low voltage (I_{OL} = 2 mA)	V_{OL}	-	0.3	V	2
Input/output leakage current	(I_{IN}/I_{OZ})	-10	10	µA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max EV_{IN} values found in the Table 3.
2. Open-drain mode is for MMC cards only.
3. At recommended operating conditions with E/DV_{DD} = 3.3 V.

Table 34. eSDHC interface DC electrical characteristics ($E/D/OV_{DD}$=1.8 V)[3]

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $E/D/OV_{DD}$	-	V	1
Input low voltage	V_{IL}	-	0.3 x $E/D/OV_{DD}$	V	1
Output high voltage (I_{OH} = -2 mA at $E/D/OV_{DD}$ min)	V_{OH}	$E/D/OV_{DD}$ - 0.45	-	V	-
Output low voltage (I_{OL} = 2 mA at EV_{DD} min)	V_{OL}	-	0.45	V	-
Output high voltage (I_{OH} = -100 µA)	V_{OH}	$E/D/OV_{DD}$ - 0.2	-	V	2
Output low voltage (I_{OL} = 2 mA)	V_{OL}	-	0.3	V	2

Table continues on the next page...

Table 34. eSDHC interface DC electrical characteristics (E/D/OV_{DD}=1.8 V)[3] (continued)

Characteristic	Symbol	Min	Max	Unit	Notes
Input/output leakage current	(I_{IN}/I_{OZ})	-10	10	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max E/D/OV_{IN} values found in the Table 3.
2. Open-drain mode is for MMC cards only.
3. At recommended operating conditions with E/D/OV_{DD} = 1.8 V.

3.12.2 eSDHC AC timing specifications

This section provides the AC timing specifications.

This table provides the eSDHC AC timing specifications as defined in Figure 14, Figure 15, and Figure 16.

Table 35. eSDHC AC timing specifications (full-speed/high-speed mode)[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency: • SD/SDIO (full-speed/high-speed mode) • MMC (full-speed/high-speed mode)	f_{SHSCK}	0	25/50 20/52	MHz	2, 4
SDHC_CLK clock low time (full-speed/high-speed mode)	t_{SHSCKL}	10/7	-	ns	4
SDHC_CLK clock high time (full-speed/high-speed mode)	t_{SHSCKH}	10/7	-	ns	4
SDHC_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK	$t_{SHSIVKH}$	2.5	-	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK	$t_{SHSIXKH}$	2.5	-	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOX}$	-3	-	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOV}$	-	3	ns	4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC high-speed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0-25MHz for an SD/SDIO card and 0-20MHz for an MMC card. In high-speed mode, the clock frequency value can be 0-50MHz for an SD/SDIO card and 0-52MHz for an MMC card.

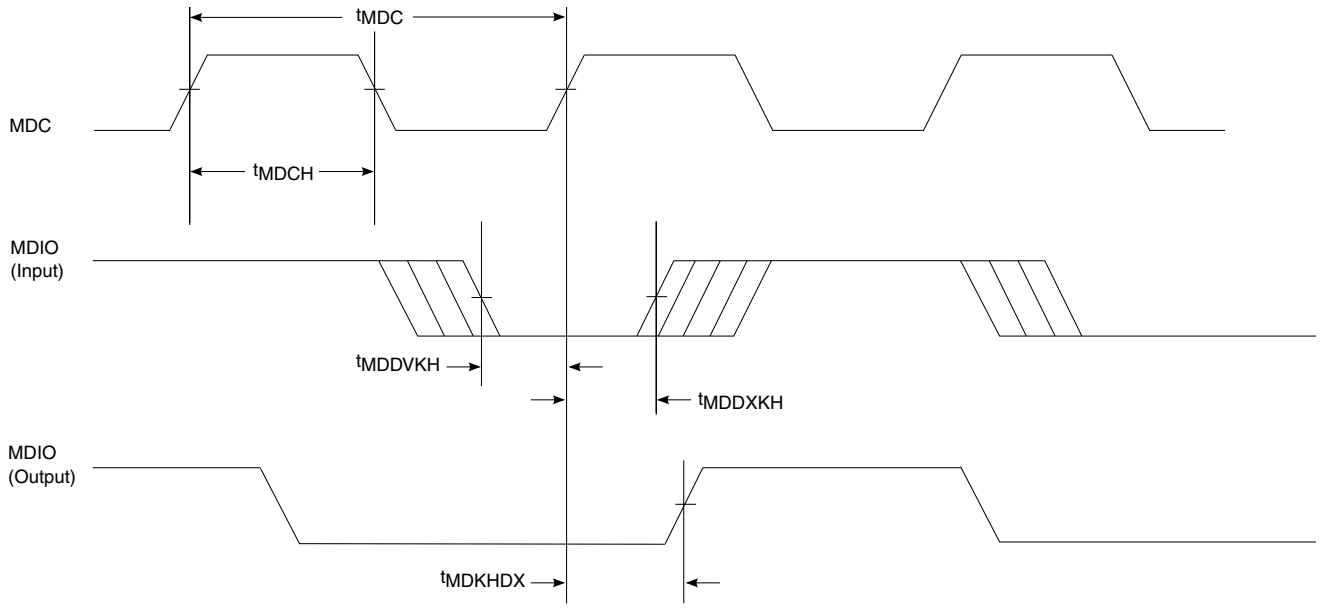


Figure 23. Ethernet management interface 1 timing diagram

3.13.1.2 Ethernet management interface 2 (EMI2)

This section describes the electrical characteristics for the EMI2 interface.

The EMI2 interface timing is compatible with IEEE Std 802.3™ clause 45.

3.13.1.2.1 EMI2 DC electrical characteristics

This section describes the DC electrical characteristics for EMI2_MDIO and EMI2_MDC. The pins are available on TV_{DD}. For operating voltages, see Table 3.

This table provides the EMI2 DC electrical characteristics when operating at TV_{DD} = 2.5 V.

Table 42. EMI2 DC electrical characteristics (TV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TVDD	-	-	2
Input low voltage	V_{IL}	-	0.2 x TVDD	-	2
Input current (V_{IN} = 0 or V_{IN} = TV_{DD})	I_{IN}	-50.0	50.0	-	3, 4
Output high voltage (TV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.0	-	-	4
Output low voltage (TV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	-	0.4	-	4

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3.

- PCI Express
- Serial ATA (SATA) interface
- SGMII interface
- QSGMII interface
- XFI interface

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.16.4 PCI Express

This section describes the clocking dependencies, as well as the DC and AC electrical specifications for the PCI Express bus.

3.16.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.16.4.2 PCI Express clocking requirements for SD2_REF_CLK*n*_P and SD2_REF_CLK*n*_N

SerDes 2 (SD2_REF_CLK[1:2]_P and SD2_REF_CLK[1:2]_N) may be used for various SerDes PCI Express configurations based on the RCW configuration field SRDS_PRTCL. PCI Express is supported on SerDes 2.

For more information on these specifications, see SerDes reference clocks.

3.16.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.16.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

This table defines the AC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 78. PCI Express 3.0 (8 GT/s) differential receiver input AC specifications[5]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. See Note 1.
Eye Width at TP2P	$T_{RX-SV-8G}$	0.3	—	0.35	UI	See Note 1
Differential mode interference	$V_{RX-SV-DIFF-8G}$	14	—	—	mV	Frequency = 2.1GHz. See Note 2.
Sinusoidal Jitter at 100 MHz	$T_{RX-SV-SJ-8G}$	—	—	0.1	UI p-p	Fixed at 100 MHz. See Note 3.
Random Jitter	$T_{RX-SV-RJ-8G}$	—	—	2.0	ps RMS	Random jitter spectrally flat before filtering. See Note 4.

Note:

1. $T_{RX-SV-8G}$ is referenced to TP2P and obtained after post processing data captured at TP2. $T_{RX-SV-8G}$ includes the effects of applying the behavioral receiver model and receiver behavioral equalization.
2. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.
3. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency as shown in Figure 37.
4. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. See Figure 37 for details. Rj may be adjusted to meet the 0.3 UI value for $T_{RX-SV-8G}$.
5. For recommended operating conditions, see Table 3.

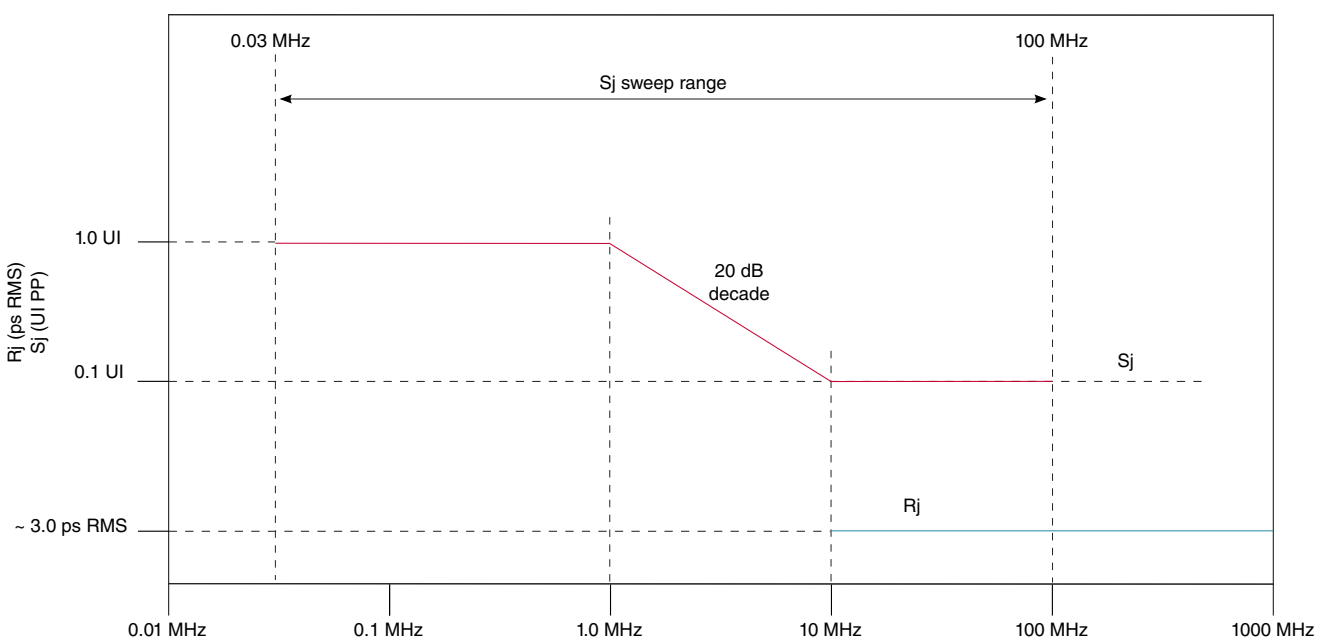


Figure 37. Swept sinusoidal jitter mask

3.16.8.3 XFI AC timing specifications

NOTE

The AC specifications do not include RefClk jitter.

This table defines the XFI transmitter AC timing specifications.

Table 104. XFI transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud Rate	T_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter tolerance	T_J	-	-	0.3	UI p-p

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 105. XFI receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	-	96.96	-	ps	-
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s	-
Total non-EQJ jitter	$T_{NON-EQJ}$	-	-	0.45	UI p-p	1
Total jitter tolerance	T_J	-	-	0.65	UI p-p	1, 2

1. The total jitter (TJ) consists of Random Jitter (RJ), Duty Cycle Distortion (DCD), Periodic Jitter (PJ), and Inter-Symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (RJ), and periodic jitter (PJ). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = TJ - ISI = RJ + DCD + PJ.

2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.

This figure shows the sinusoidal jitter tolerance of XFI receiver.

Table 113. 10GBase-KR receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Total jitter tolerance	R_{TJ}	-	-	Per IEEE Std 802.3ap-2007, Annex 69a.	UI p-p
Random jitter	R_{RJ}	-	-	0.13	UI p-p
Sinusoidal jitter (maximum)	R_{SJ-max}	-	-	0.115	UI p-p
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p

3.17 I²C interface

This section describes the DC and AC electrical characteristics for the I²C interface.

3.17.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interface when operating at DV_{DD} = 3.3 V.

Table 114. I²C DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	2
Output low voltage (DV_{DD} = min, IOL = 3 mA, DV_{DD} > 2V)	V_{OL}	-	0.4	V	3
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	4
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} (min) and 0.9 x DV_{DD} (max))	I_I	-50.0	50.0	µA	5
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.

3. The output voltage (open drain or open collector) condition = 3 mA sink current.

4. See the chip reference manual for information about the digital filter used.

5. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.

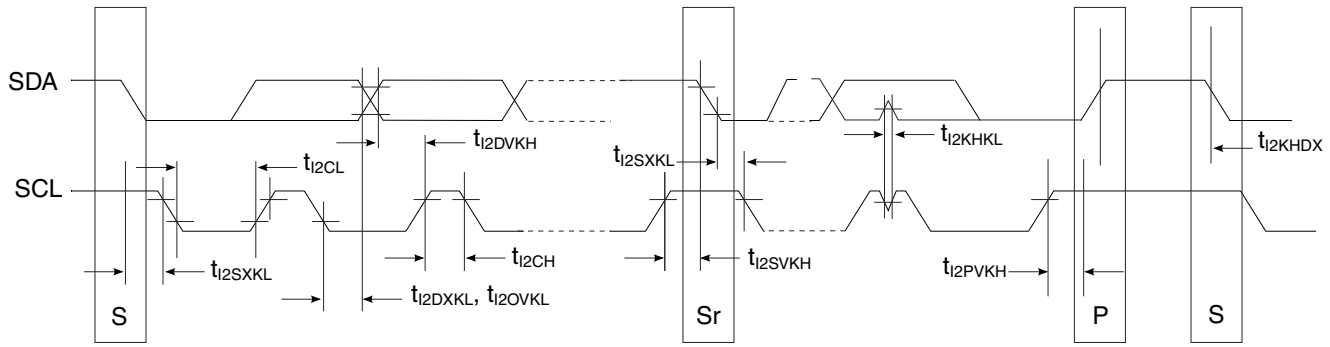


Figure 46. I²C bus AC timing diagram

3.18 Integrated Flash Controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.18.1 Integrated Flash Controller DC electrical characteristics

Table below provides the DC electrical characteristics for the integrated flash controller when operating at OV_{DD} = 1.8 V.

Table 117. Integrated Flash Controller DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.6	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.32	V	-

NOTE:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

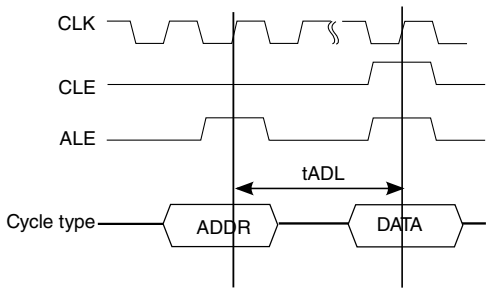


Figure 72. t_{ADL} timings

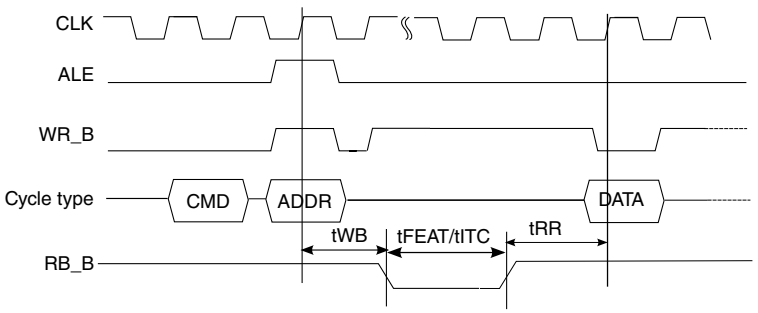


Figure 73. t_{WB}, t_{FEAT}, t_{ITC}, t_{RR} timings

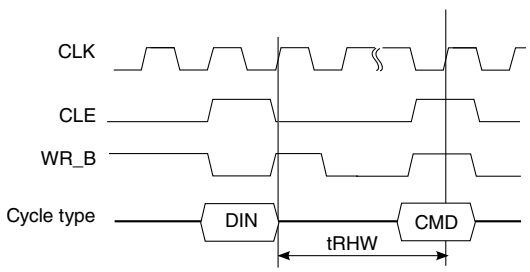


Figure 74. t_{RHW} timings

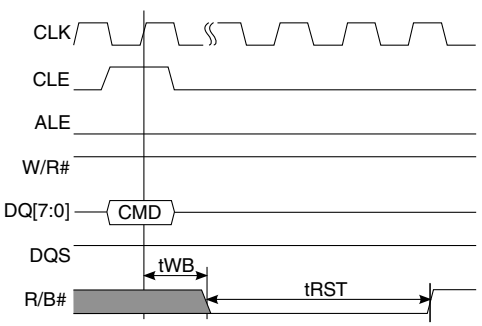


Figure 75. t_{WB} and t_{RST} timings

Table 129. QuadSPI SDR mode input and output timing (continued)

Parameter	Symbol	Min	Max	Unit
Setup time for incoming data	t_{NIIVKH}	5.0	-	ns
Hold time requirement for incoming data	t_{NIIXKH}	1.0	-	ns
Output data delay	t_{NIKHOV}	-	1.95	ns
Output data hold	t_{NIKHOX}	-1.45	-	ns

This table provides the QuadSPI input and output timing in SDR mode with internal DQS (MCR[DQS_EN]=1 with regard to the 1st sample point). Note that T represents the clock period, the value of i depends on qSPI_SMPR[xSDLY, xSPHS], j depends on qSPI_FLSHCR[TCSH], k depends on qSPI_FLSHCR[TCSS], Tcoars depends on SCLK_CONFIG[7:5], and Ttapx depends on SOCCFG[7:0]/SOCCFG[23:16].

Table 130. QuadSPI SDR mode input and output timing

Parameter	Symbol	Min	Max	Unit
Clock rise/fall time	T_{RISE}/T_{FALL}	1.0	-	ns
CS output hold time	$t_{NIKHOX2}$	-3.3 + j * T	-	ns
CS output delay	$t_{NIKHOV2}$	-3.0 + k * T	-	ns
Setup time for incoming data	t_{NIIVKH}	2.5 - T_{coars} - T_{tap}	-	ns
Hold time requirement for incoming data	t_{NIIXKH}	1 + T_{coars} + T_{tap}	-	ns
Output data delay	t_{NIKHOV}	-	1.45	ns
Output data hold	t_{NIKHOX}	-1.45	-	ns

This figure shows the QuadSPI AC timing in SDR mode.

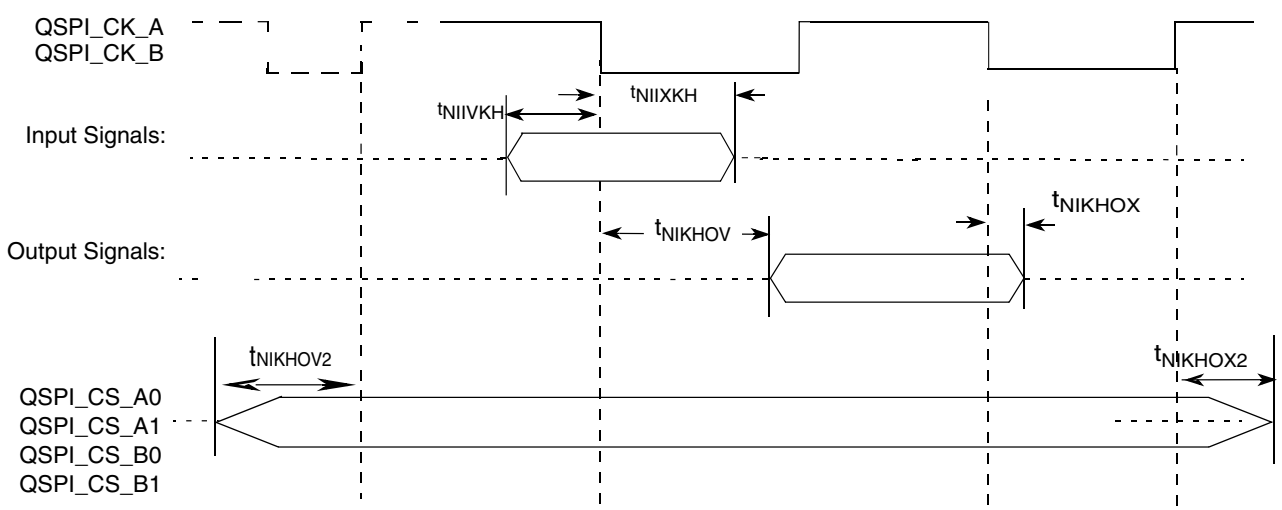


Figure 82. QuadSPI AC timing — SDR mode

Table 132. HDLC and synchronous UART DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x DVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	µA	3
Output high voltage (DV_{DD}=min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (DV_{DD}=min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
3. The symbol V_{IN} represents the input voltage of the supply referenced in Table 3.

This table provides the DC electrical characteristics for the HDLC and Synchronous UART protocols when DV_{DD} = 1.8 V.

Table 133. HDLC and synchronous UART DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.3 x DVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	µA	3
Output high voltage (DV_{DD}=min, I_{OH} = -2 mA)	V_{OH}	1.35	-	V	-
Output low voltage (DV_{DD}=min, I_{OL} = 2 mA)	V_{OL}	-	0.45	V	-

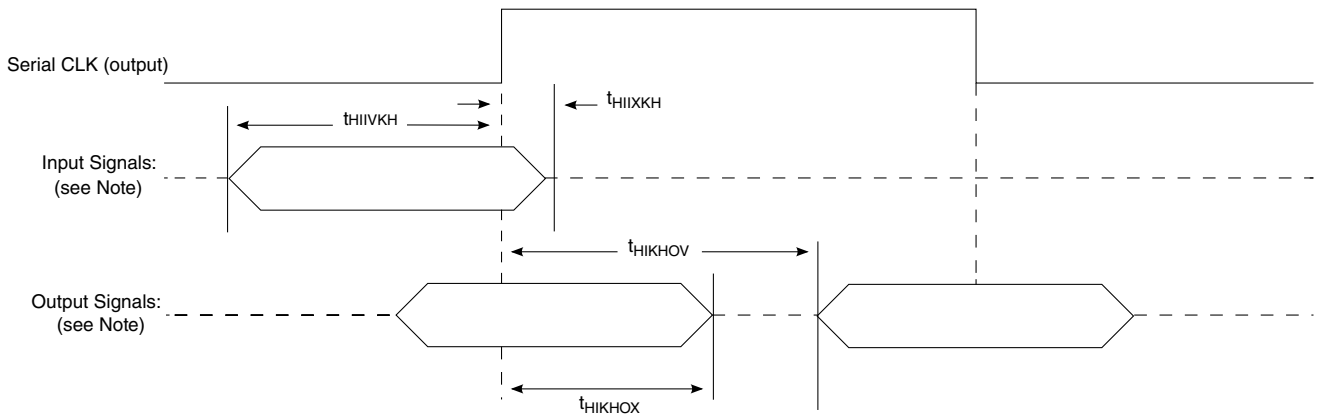
1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
3. The symbol V_{IN} represents the input voltage of the supply referenced in Table 3.

3.21.1.2 HDLC and synchronous UART AC timing specifications

NOTE

Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This table provides the input and output AC timing specifications for the HDLC and synchronous UART protocols.



Note: The clock edge is selectable.

Figure 89. AC timing (internal clock) diagram

3.21.2 Time division multiplexed/serial interface (TDM/SI)

This section describes the DC and AC electrical characteristics for the TDM/SI interface.

3.21.2.1 TDM/SI DC electrical characteristics

This table provides the DC electrical characteristics for the TDM/SI interface when operating at DV_{DD} = 3.3 V.

Table 136. TDM/SI DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x DVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	μA	3
Output high voltage (DV_{DD}=min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (DV_{DD}=min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.					
3. The symbol V_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the TDM/SI DC electrical characteristics when DV_{DD} = 1.8 V.

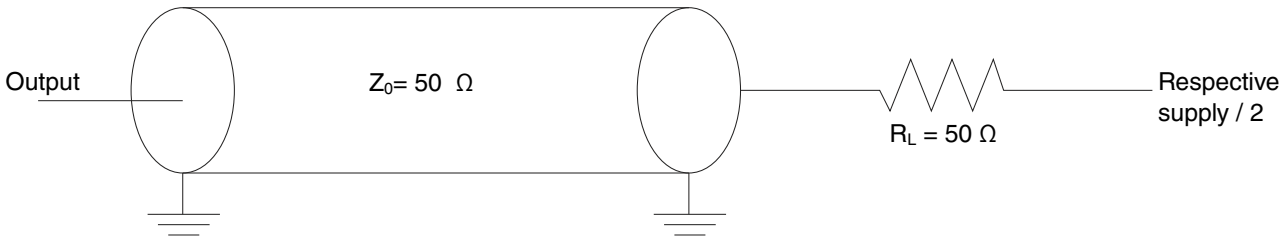
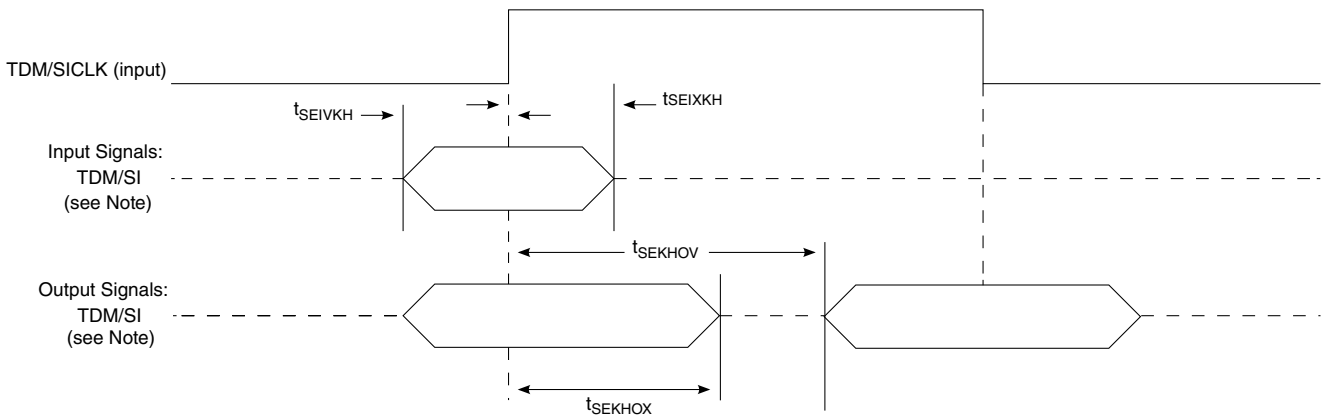


Figure 90. TDM/SI AC test load

This figure represents the AC timing from the TDM/SI AC timing specifications table. Note that, although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the TDM/SI timing with an external clock.



Note: The clock edge is selectable on TDM/SI.

Figure 91. TDM/SI AC timing (external clock) diagram

3.22 Serial peripheral interface (SPI)

This section describes the DC and AC electrical characteristics for the SPI interface.

3.22.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface operating at OV_{DD} = 1.8 V.

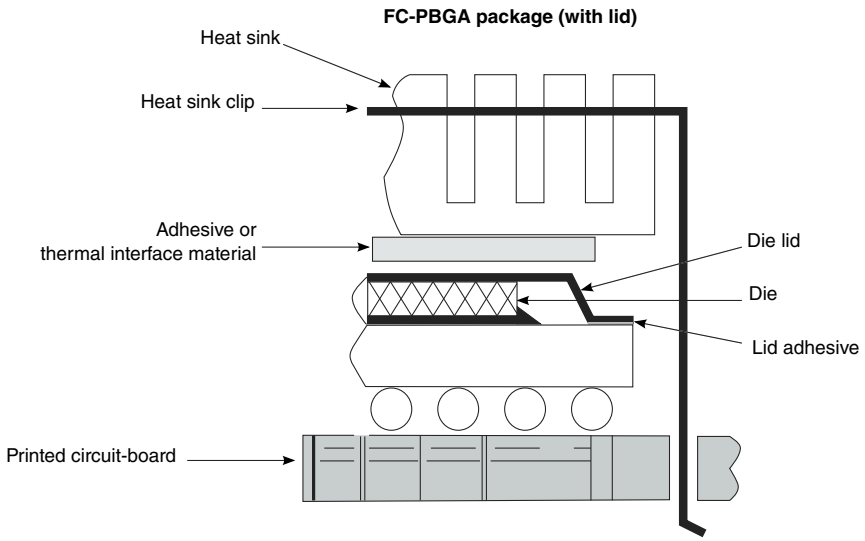


Figure 95. Package exploded, cross-sectional view-FC-PBGA (with lid)

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

5.3.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure shows the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

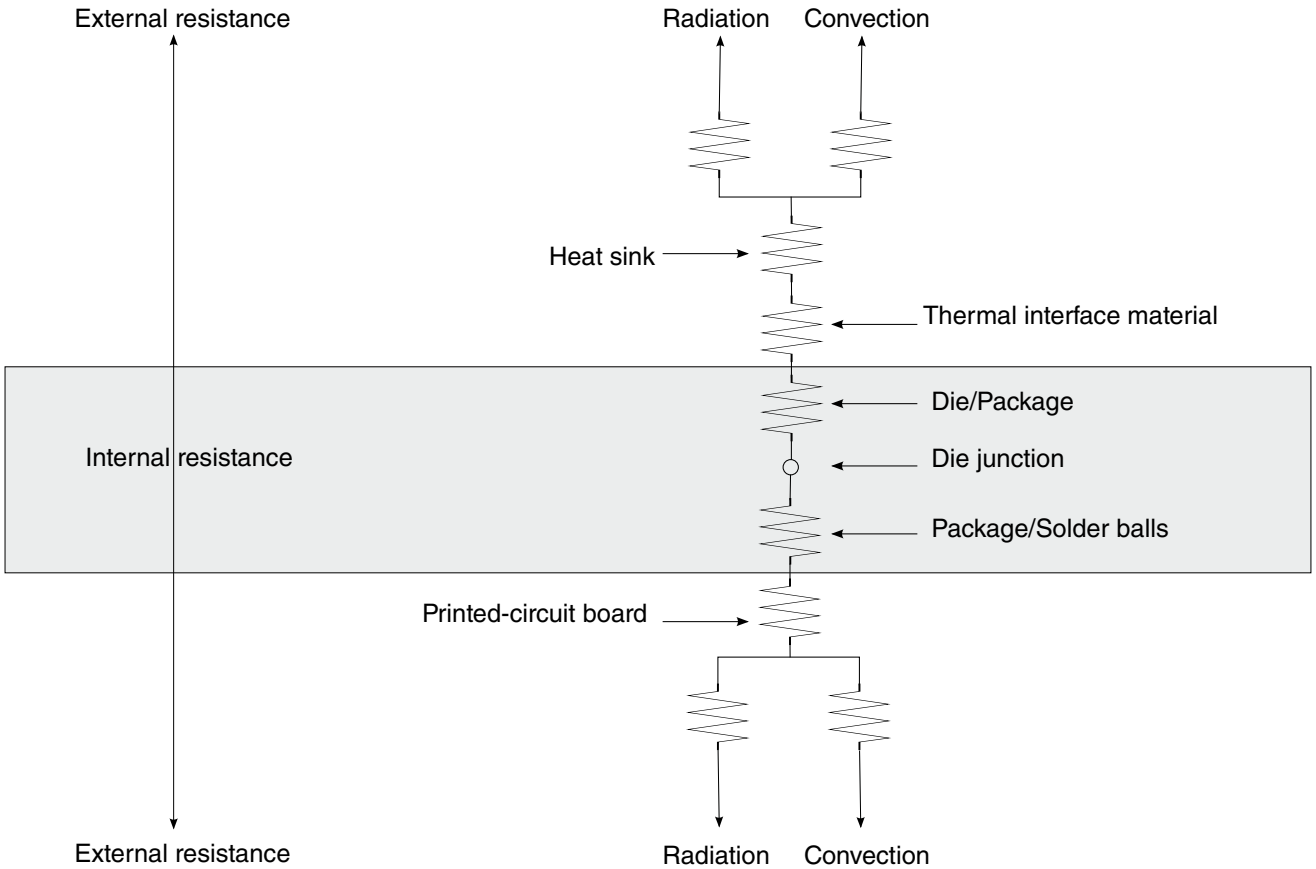


Figure 96. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

5.3.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 95).