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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	8 Core, 64-Bit
Speed	1.4GHz
Co-Processors/DSP	-
RAM Controllers	DDR4
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	10GbE (2), 1GbE (8)
SATA	SATA 6Gbps (1)
USB	USB 3.0 (2) + PHY
Voltage - I/O	-
Operating Temperature	-40°C ~ 105°C
Security Features	Secure Boot, TrustZone®
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088axe7pta

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IRQ07/GPIO4_05/ TDMA_TSYNC/ UC1_RTSB_TXEN	External Interrupt	L5	I	DV_{DD}	1
IRQ08/GPIO4_06/ TDMB_RXD/UC3_RXD7/ TDMB_TXD	External Interrupt	M5	I	DV_{DD}	1
IRQ09/GPIO4_07/ TDMB_RSYNC/ UC3_CTSB_RXDV	External Interrupt	N5	I	DV_{DD}	1
IRQ10/GPIO4_08/ TDMB_RXD_EXC/ TDMB_TXD/UC3_TXD7	External Interrupt	P4	I	DV_{DD}	1
IRQ11/GPIO4_09	External Interrupt	W3	I	LV_{DD}	1
		Debug			
ASLEEP/GPIO1_28/ cfg_soc_use	Asleep	E9	O	OV_{DD}	1, 4
CKSTP_OUT_B	Checkstop Out	G15	O	OV_{DD}	1, 6, 7
CLK_OUT	Clock Out	G16	O	OV_{DD}	2
EVT0_B	Event 0	E10	IO	OV_{DD}	9
EVT1_B	Event 1	E13	IO	OV_{DD}	9
EVT2_B	Event 2	E8	IO	OV_{DD}	9
EVT3_B	Event 3	E12	IO	OV_{DD}	9
EVT4_B	Event 4	E11	IO	OV_{DD}	9
EVT5_B/**IIC3_SCL**/GPIO4_28/ USB2_DRVVBUS/BRGO4/ CLK11	Event 5	L4	IO	DV_{DD}	---
EVT6_B/**IIC3_SDA**/GPIO4_29/ USB2_PWRFAULT/BRGO1/ CLK12_CLK8	Event 6	M4	IO	DV_{DD}	---
EVT7_B/**IIC4_SCL**/GPIO4_30/ TDMA_RQ/UC1_CDB_RXER	Event 7	M3	IO	DV_{DD}	---
EVT8_B/**IIC4_SDA**/GPIO4_31/ TDMB_RQ/UC3_CDB_RXER	Event 8	N3	IO	DV_{DD}	---
		Trust			
TA_BB_TMP_DETECT_B	Battery Backed Tamper Detect	H12	I	$TA\_BB\_V_{DD}$	---
TA_TMP_DETECT_B	Tamper Detect	H20	I	OV_{DD}	---
		System Control			
HRESET_B	Hard Reset	F8	IO	OV_{DD}	6, 7
PORESET_B	Power On Reset	F9	I	OV_{DD}	---
RESET_REQ_B	Reset Request (POR or Hard)	F10	O	OV_{DD}	1, 5
		Clocking			
DIFF_SYSCLK	Single Source System Clock Differential (positive)	AA13	I	SV_{DD}	20

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
QSPI_A_DQS/**IFC_A10**/ GPIO2_04/IFC_RB3_B/ IFC_CS_B5	DQS	D14	I	OV_{DD}	1
QSPI_A_SCK/**IFC_A02**/ GPIO1_18	SCK	C9	O	OV_{DD}	1, 5
QSPI_B_CS0/**IFC_A03**/ GPIO1_19	Chip Select	D10	O	OV_{DD}	1, 5
QSPI_B_CS1/**IFC_A04**/ GPIO1_20	CS1	C10	O	OV_{DD}	1, 5
QSPI_B_DATA0/**IFC_PAR0**/ GPIO2_06/QSPI_A_DATA4	DATA0	B18	IO	OV_{DD}	---
QSPI_B_DATA1/**IFC_PAR1**/ GPIO2_07/QSPI_A_DATA5	DATA1	D17	IO	OV_{DD}	---
QSPI_B_DATA2/ **IFC_PERR_B**/GPIO2_16/ QSPI_A_DATA6	DATA2	E17	IO	OV_{DD}	---
QSPI_B_DATA3/**IFC_CS3_B**/ GPIO2_11/QSPI_A_DATA7	DATA3	C20	IO	OV_{DD}	---
QSPI_B_DQS/**IFC_A11**/ GPIO2_05/IFC_CS_B6	DQS	C14	I	OV_{DD}	1
QSPI_B_SCK/**IFC_A05**/ GPIO1_21/cfg_dram_type	SCK	C11	O	OV_{DD}	1, 4
QUICC Engine					
BRGO1/**IIC3_SDA**/GPIO4_29/ EVT6_B/USB2_PWRFAULT/ CLK12_CLK8	Baud Rate Generator Output	M4	O	DV_{DD}	1
BRGO2/**IIC2_SCL**/GPIO3_12/ SDHC_CD_B/CLK9	Baud Rate Generator Output	K3	O	DV_{DD}	1
BRGO3/**IIC2_SDA**/GPIO3_13/ SDHC_WP/CLK10	Baud Rate Generator Output	L3	O	DV_{DD}	1
BRGO4/**IIC3_SCL**/GPIO4_28/ EVT5_B/USB2_DRVVBUS/ CLK11	Baud Rate Generator Output	L4	O	DV_{DD}	1
CLK10/**IIC2_SDA**/GPIO3_13/ SDHC_WP/BRGO3	Clock	L3	I	DV_{DD}	1
CLK9/**IIC2_SCL**/GPIO3_12/ SDHC_CD_B/BRGO2	Clock	K3	I	DV_{DD}	1
TDMA_RQ/**IIC4_SCL**/ GPIO4_30/EVT7_B/ UC1_CDB_RXER	RQ	M3	O	DV_{DD}	1
TDMB_RQ/**IIC4_SDA**/ GPIO4_31/EVT8_B/ UC3_CDB_RXER	RQ	N3	O	DV_{DD}	1
UC1_CDB_RXER/**IIC4_SCL**/ GPIO4_30/EVT7_B/TDMA_RQ	Receive Error	M3	I	DV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND097	Core, Platform and PLL Ground	N10	---	---	---
GND098	Core, Platform and PLL Ground	N12	---	---	---
GND099	Core, Platform and PLL Ground	N14	---	---	---
GND100	Core, Platform and PLL Ground	N16	---	---	---
GND101	Core, Platform and PLL Ground	N18	---	---	---
GND102	Core, Platform and PLL Ground	N20	---	---	---
GND103	Core, Platform and PLL Ground	N23	---	---	---
GND104	Core, Platform and PLL Ground	N26	---	---	---
GND105	Core, Platform and PLL Ground	P6	---	---	---
GND106	Core, Platform and PLL Ground	P9	---	---	---
GND107	Core, Platform and PLL Ground	P11	---	---	---
GND108	Core, Platform and PLL Ground	P13	---	---	---
GND109	Core, Platform and PLL Ground	P15	---	---	---
GND110	Core, Platform and PLL Ground	P17	---	---	---
GND111	Core, Platform and PLL Ground	P19	---	---	---
GND112	Core, Platform and PLL Ground	P23	---	---	---
GND113	Core, Platform and PLL Ground	R5	---	---	---
GND114	Core, Platform and PLL Ground	R8	---	---	---
GND115	Core, Platform and PLL Ground	R10	---	---	---
GND116	Core, Platform and PLL Ground	R12	---	---	---
GND117	Core, Platform and PLL Ground	R14	---	---	---
GND118	Core, Platform and PLL Ground	R16	---	---	---

Table continues on the next page...

4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.

5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or, if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.

7. This pin is an open-drain signal.

8. Recommend that a pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.

9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

10. These are test signals for factory use only and must be pulled up (100 Ω to 1 kΩ) to the respective power supply for normal operation.

11. This pin requires a 200 Ω pull-up to the respective power supply.

12. Do not connect. These pins should be left floating.

13. These pins must be pulled up to TV_{DD} through a 180 Ω ± 1% resistor for MDC and a 330 Ω ± 1% resistor for MDIO.

14. This pin requires an external 1 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

15. These pins must be pulled to ground (GND).

16. This pin requires a 698 Ω pull-up to the respective power supply.

17. These pins should be tied to ground if the diode is not utilized for temperature monitoring.

18. SD_GND must be directly connected to GND.

19. For proper clock selection, terminate cfg_eng_use0 with a pull up or pull down of 4.7 kΩ to ensure that the signal will have a valid state as soon as the IO voltage reaches its operating condition.

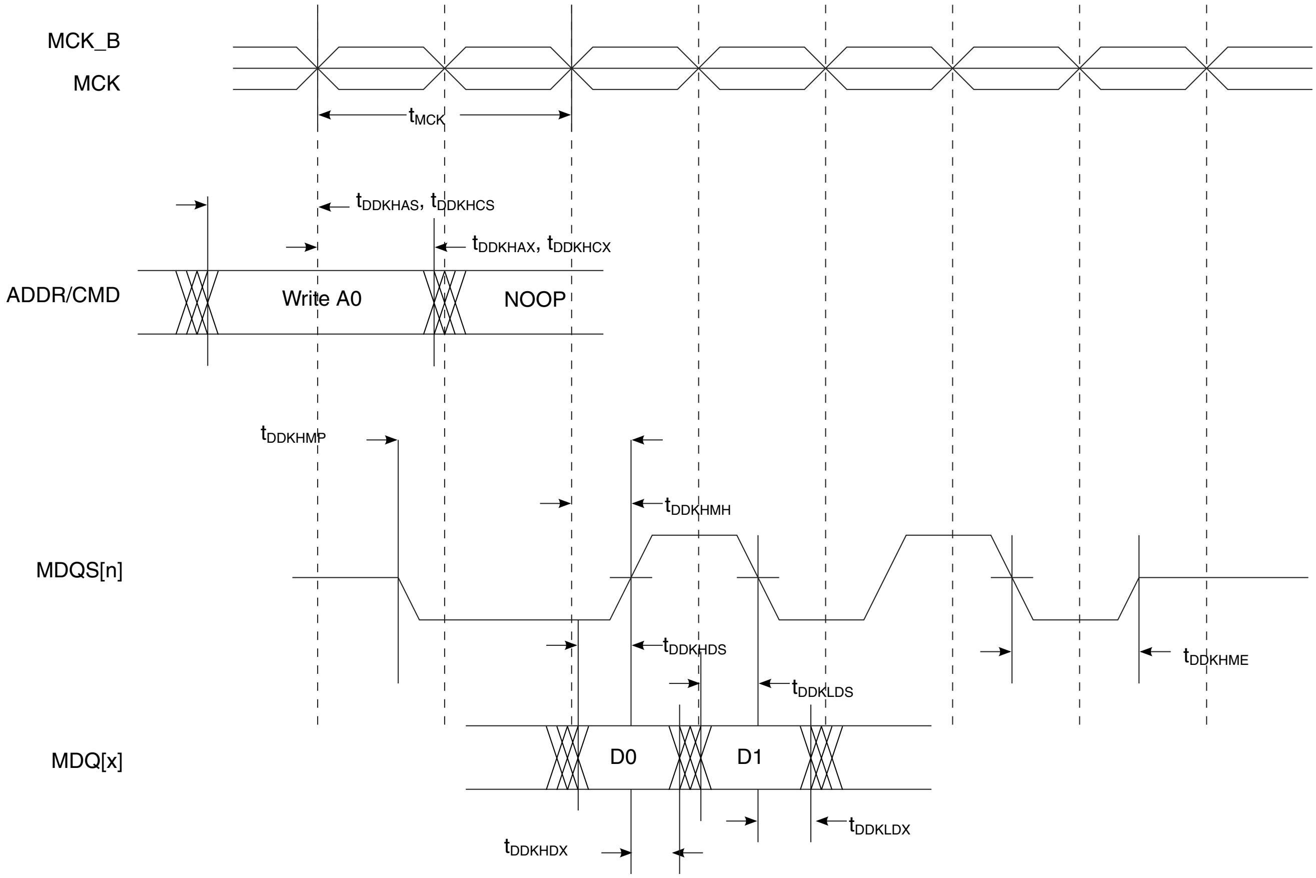


Figure 13. DDR4 output timing diagram

3.11 Dual universal asynchronous receiver/transmitter (DUART) interface

This section describes the DC and AC electrical characteristics for the DUART interface.

3.11.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface when operating at DV_{DD} = 3.3 V.

Table 30. DUART DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x DVDD	V	2

Table continues on the next page...

Table 30. DUART DC electrical characteristics (DV_{DD} = 3.3 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	μA	3
Output high voltage (I_{OH} = -2.0 mA)	V_{OH}	2.4	-	V	-
Output low voltage (I_{OL} = 2.0 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.

2. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in the Recommended Operating Conditions table.

3. Note that the symbol DV_{IN} represents the input voltage of the supply referenced in the Recommended Operating Conditions table.

This table provides the DC electrical characteristics for the DUART interface when operating at DV_{DD} = 1.8 V.

Table 31. DUART DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x DV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	μA	3
Output high voltage (I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.

2. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in the Recommended Operating Conditions table.

3. Note that the symbol DV_{IN} represents the input voltage of the supply referenced in the Recommended Operating Conditions table.

3.11.2 DUART AC timing specifications

This table provides the AC timing specifications for the DUART interface.

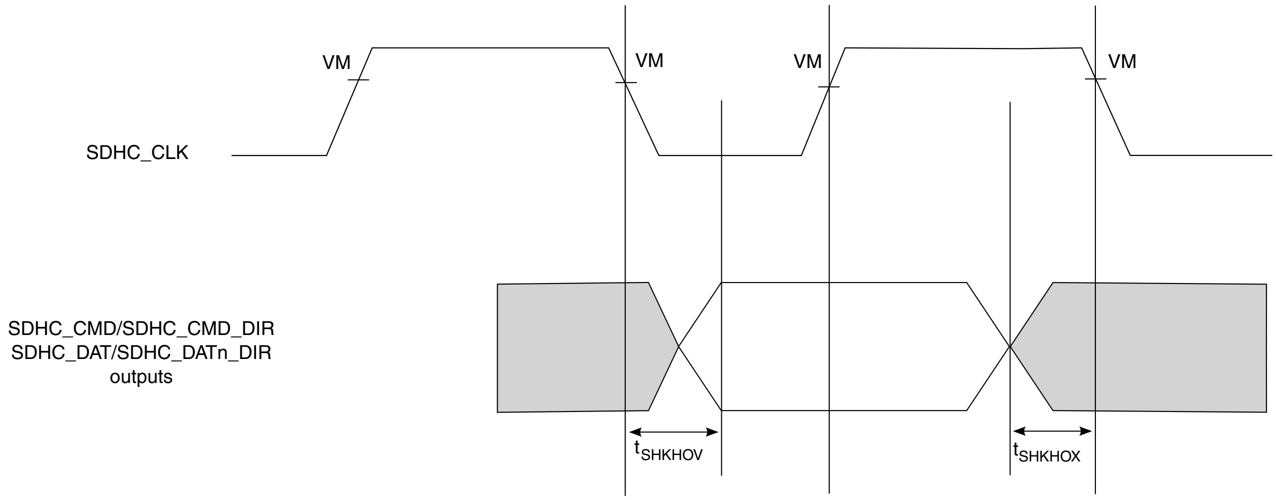
Table 32. DUART AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Minimum baud rate	baud	f_{PLAT}/(2 x 1,048,576)	-	baud	1, 2
Maximum baud rate	baud	-	f_{PLAT}/(2 x 16)	baud	1, 3

1. f_{PLAT} refers to the internal platform clock.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

3. The actual attainable baud rate is limited by the latency of interrupt processing.



VM = Midpoint voltage ($EV_{DD}/2$)

Figure 16. eSDHC high-speed mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR50 mode.

Table 36. eSDHC AC timing specifications (SDR50)[2]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency	f_{SHSCK}	0	100	MHz	-
SDHC_CLK clock rise and fall times	$t_{SHSCKR/}$ t_{SHSCKF}	-	2	ns	1
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK	t_{SHSCSK}	-0.1	0.1	ns	1
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	$t_{SHSIVKH}$	2.1	-	ns	1
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	$t_{SHSIXKH}$	1.1	-	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	$t_{SHSKHOX}$	1.7	-	ns	1
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	$t_{SHSKHOV}$	-	6.1	ns	1
Notes: 1. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 30$ pF. 2. For recommended operating conditions, see Table 3.					

This figure provides the eSDHC clock input timing diagram for SDR50 mode.

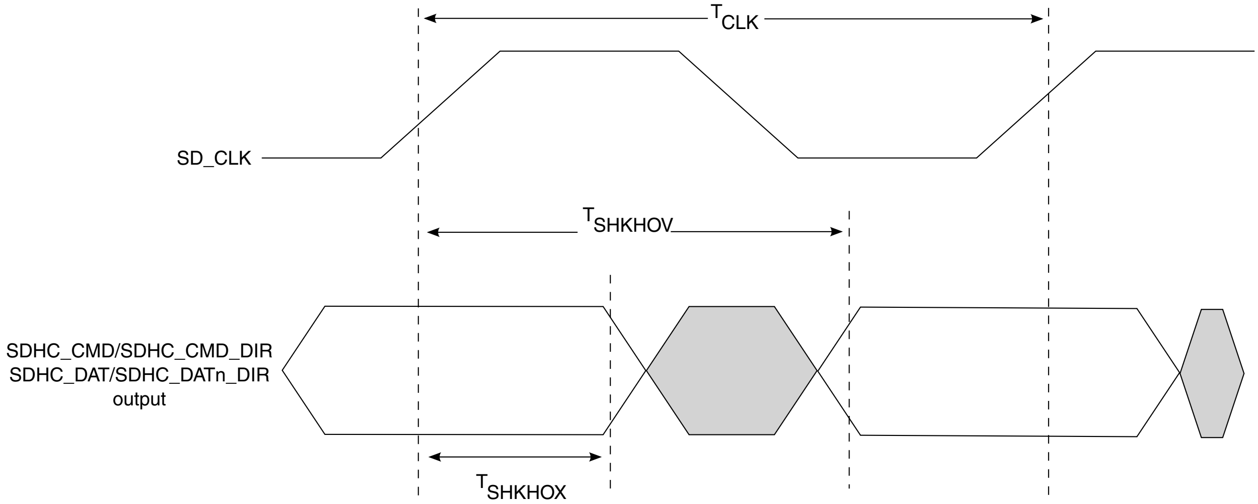


Figure 19. eSDHC SDR50 mode output timing diagram

This table provides the eSDHC AC timing specifications for DDR50/DDR mode.

Table 37. eSDHC AC timing specifications (DDR50/DDR)[3]

Parameter		Symbol	Min	Max	Units	Notes
SDHC_CLK clock frequency	SD/SDIO DDR50 mode	f_{SHCK}	—	50	MHz	—
	eMMC DDR mode			52		
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK		t_{SHSCSK}	-0.1	0.1	ns	—
SDHC_CLK clock rise and fall times	SD/SDIO DDR50 mode	t_{SHCKR}/	—	4	ns	1, 2
	eMMC DDR mode	t_{SHCKF}		2		1, 2
Input setup times: SDHC_DATx to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHDIVKH}$	2.0	—	ns	1
	eMMC DDR mode		1.6			2
Input hold times: SDHC_DATx to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHDIXKH}$	1.3	—	ns	1
	eMMC DDR mode		1.3			2, 4
Output hold time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	SD/SDIO DDR50 mode	$t_{SHDKHOX}$	1.7	—	ns	1
	eMMC DDR mode		3.4			2
Output delay time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	SD/SDIO DDR50 mode	$t_{SHDKHOV}$	—	6.1	ns	1
	eMMC DDR mode			6.2		2
Input setup times: SDHC_CMD to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHCIVKH}$	5.3	—	ns	1
	eMMC DDR mode		5			2
Input hold times: SDHC_CMD to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHCIXKH}$	1.2	—	ns	1
	eMMC DDR mode		1.2			2, 5
Output hold time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	SD/SDIO DDR50 mode	$t_{SHCKHOX}$	1.7	—	ns	1
	eMMC DDR mode		3.9			2
Output delay time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	SD/SDIO DDR50 mode	$t_{SHCKHOV}$	—	15.3	ns	1
	eMMC DDR mode			15.3		2

Table continues on the next page...

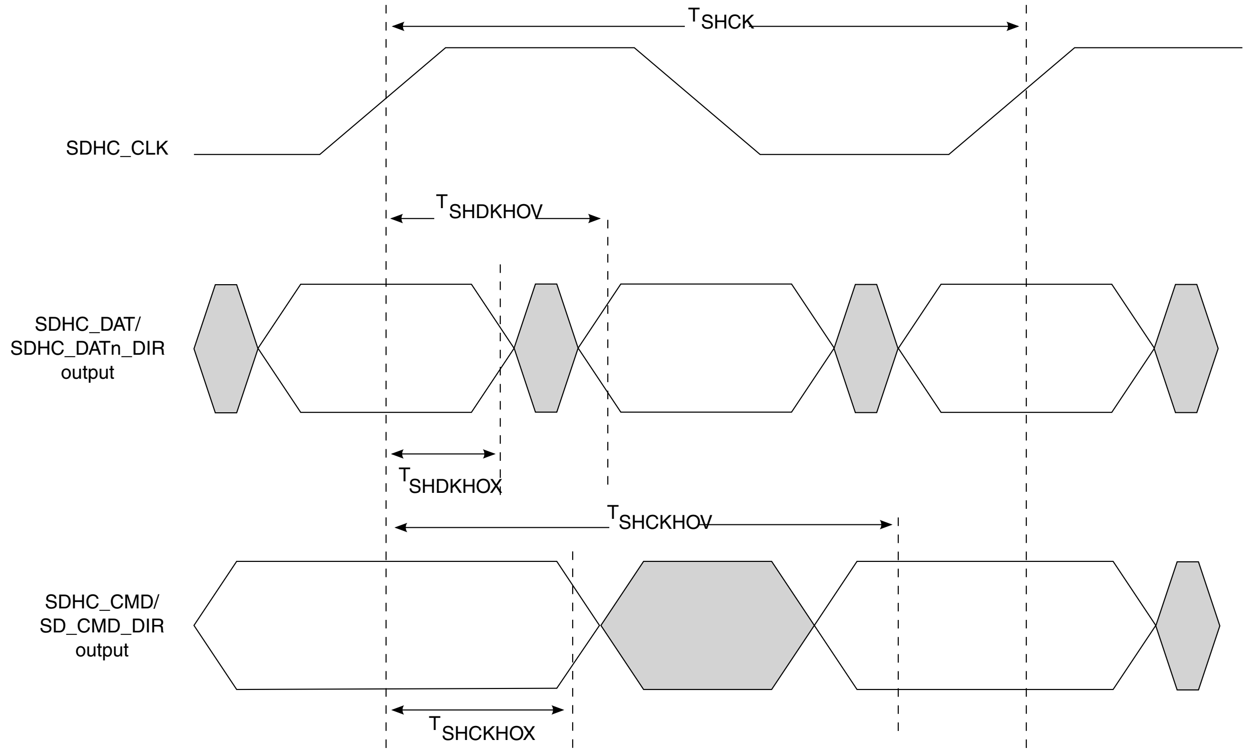


Figure 21. eSDHC DDR50/DDR mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode.

Table 38. eSDHC AC timing specifications (SDR104/eMMC HS200)

Parameter		Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency	SD/SDIO SDR104 mode	f_{SHCK}	-	167	MHz	-
	eMMC HS200 mode			167		-
SDHC_CLK clock rise and fall times		t_{SHCKR}/t_{SHCKF}	-	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOX}	1.58	-	ns	1
	eMMC HS200 mode		1.6			
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOV}	-	3.94	ns	1
	eMMC HS200 mode			3.92		
Input data window (UI)	SD/SDIO SDR104 mode	t_{SHIDV}	0.5	-	Unit Interval	1
	eMMC HS200 mode		0.475			

Notes:

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.

2. For recommended operating conditions, see Table 3.

3.13.1.2.2 EMI2 AC timing specifications

This table provides the AC timing specifications for the EMI2 interface.

Table 45. EMI2 AC timing specifications[4]

Parameter	Symbol	Min	Max	Unit	Notes
MDC frequency	f_{MDC}	-	2.5	MHz	1
MDC clock pulse width high	t_{MDCH}	160.0	-	ns	-
MDC to MDIO delay	t_{MDKHDX}	(5 x t_{enet_clk}) - 3	(5 x t_{enet_clk}) + 3	ns	2, 3
MDIO to MDC setup time	t_{MDDVKH}	8.0	-	ns	-
MDIO to MDC hold time	t_{MDDXKH}	2	-	ns	5

1. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.

2. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods ± 3 ns. For example, with an Ethernet clock of 400 MHz, the min/max delay is 12.5 ns ± 3 ns.

3. t_{enet_clk} is the Ethernet clock period (Frame Manager clock period x 2).

4. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.

5. See "AN5144, LS1088A Design Checklist" for more details.

This figure shows the Ethernet management interface 2 timing diagram.

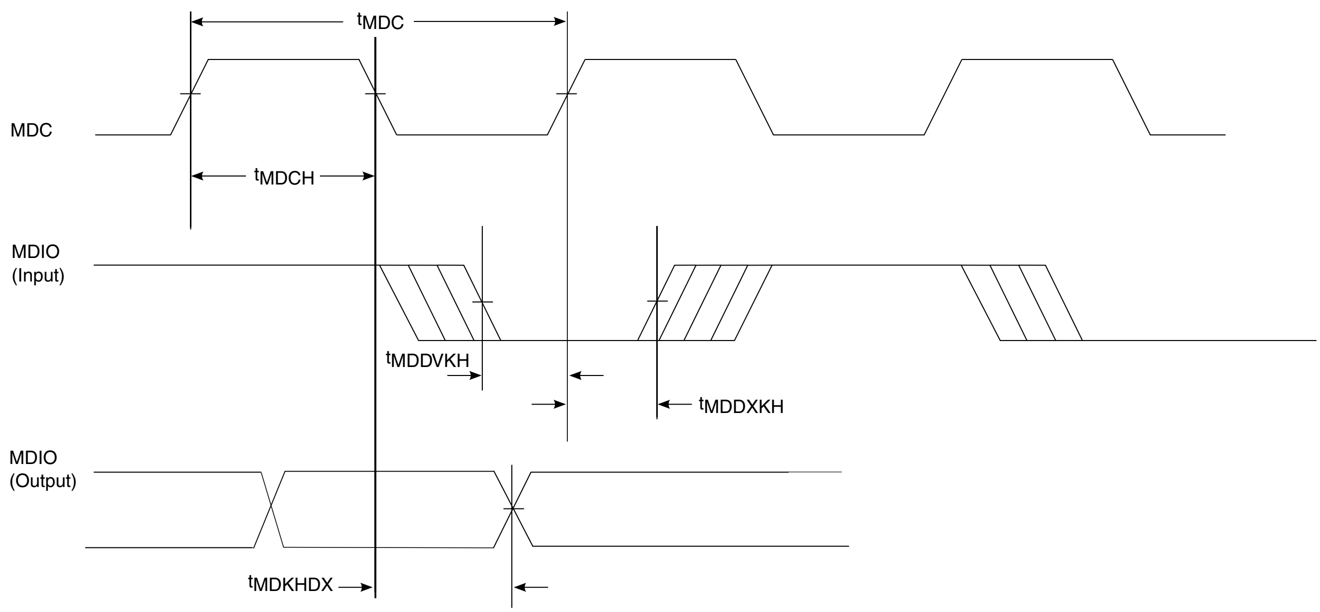


Figure 24. Ethernet management interface 2 timing diagram

3.13.2 IEEE 1588 interface

This section describes the DC and AC electrical characteristics for the IEEE 1588 interface.

3.13.2.1 IEEE 1588 DC electrical characteristics

This table provides the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 46. IEEE 1588 DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	-	V	2
Input low voltage	V_{IL}	-	-	0.2 x LVDD	V	2
Input current (V_{IN} = 0 or V_{IN} = LV_{DD})	I_{IN}	-50.0	-	50.0	μA	3
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.0	-	-	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	-	-	0.4	V	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.

This table provides the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 1.8 V supply.

Table 47. IEEE 1588 DC electrical characteristics (LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	-	V	2
Input low voltage	V_{IL}	-	-	0.3 x LVDD	V	2
Input current (V_{IN} = 0 or V_{IN} = LV_{DD})	I_{IN}	-50.0	-	50.0	μA	3
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	-	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	-	0.4	V	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.

Table 51. RGMII AC timing specifications[7]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
7. In general, the clock reference symbol representation is based on the symbol RGT, which represents RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).						

This figure shows the RGMII AC timing and multiplexing diagrams.

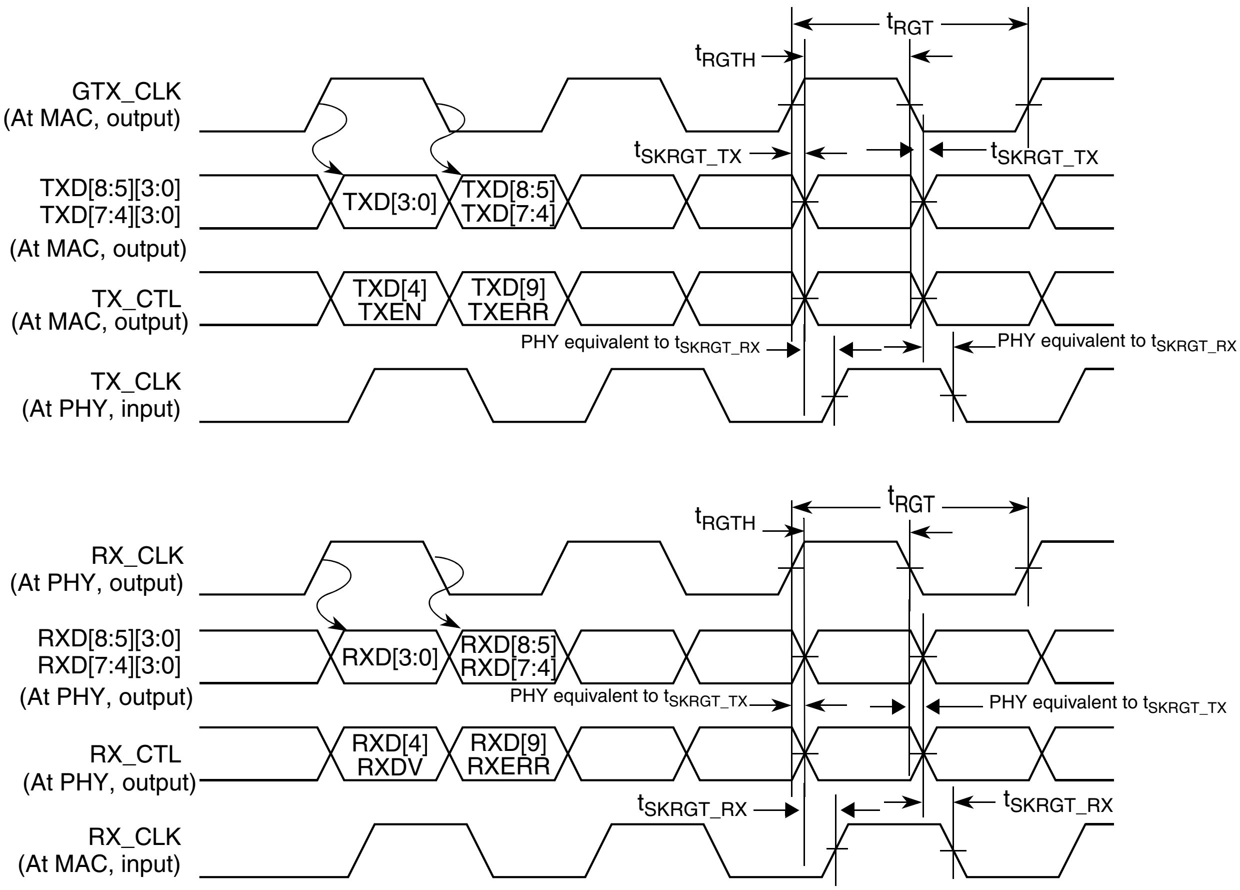


Figure 27. RGMII AC timing and multiplexing diagrams

NOTE

NXP guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

3.14 General purpose input/output (GPIO) interface

This section describes the DC and AC electrical characteristics for the GPIO interface.

Table 89. Gen 1i/1m 1.5 G receiver AC specifications[2] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Deterministic jitter, data-data 5 UI	$U_{SATA\_RXDJ5UI}$	—	—	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_RXDJ250UI}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at the receiver.

2. For recommended operating conditions, see Table 3.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 90. Gen 2i/2m 3 G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_RXTJfB/1667}$	—	—	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_RXDJfB/1667}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at the receiver.

2. For recommended operating conditions, see Table 3.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen 3i transmission The AC timing specifications do not include RefClk jitter.

Table 91. Gen 3i receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Total jitter after compliance interconnect channel	J_T	—	—	0.60	UI p-p	1
Random jitter before compliance interconnect channel	J_R	—	—	0.18	UI p-p	1
Unit interval: 6.0 Gb/s	UI	166.6083	166.6667	167.5583	ps	—

Notes:

1. Measured at the receiver.

2. The AC specifications do not include RefClk jitter.

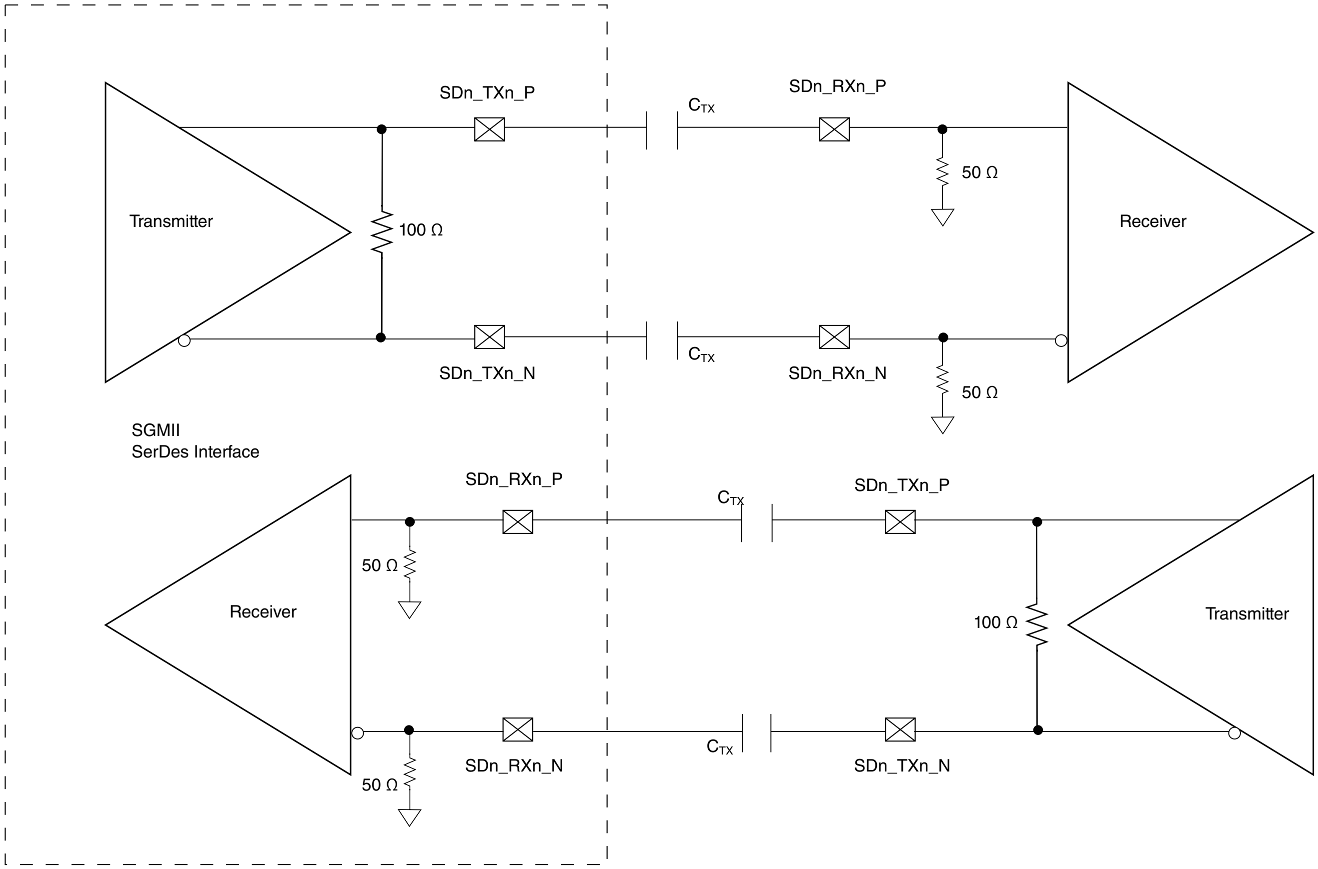


Figure 39. 4-wire AC-coupled SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

Table 101. QSGMII receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000-100ppm	5.0	5.000+100ppm	Gb/s	-
Uncorrelated bounded high probability jitter	R_{DJ}	-	-	0.15	UI p-p	-
Correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.3	UI p-p	The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example, by a PCB trace.
Bounded high probability jitter	R_{BHPJ}	-	-	0.45	UI p-p	-
Sinusoidal jitter, maximum	$R_{SJ\text{-}max}$	-	-	5.0	UI p-p	-
Sinusoidal jitter, high frequency	$R_{SJ\text{-}hf}$	-	-	0.05	UI p-p	-
Total jitter (does not include sinusoidal jitter)	R_{TJ}	-	-	0.6	UI p-p	-

The sinusoidal jitter may have any amplitude and frequency in the unshaded region of this figure.

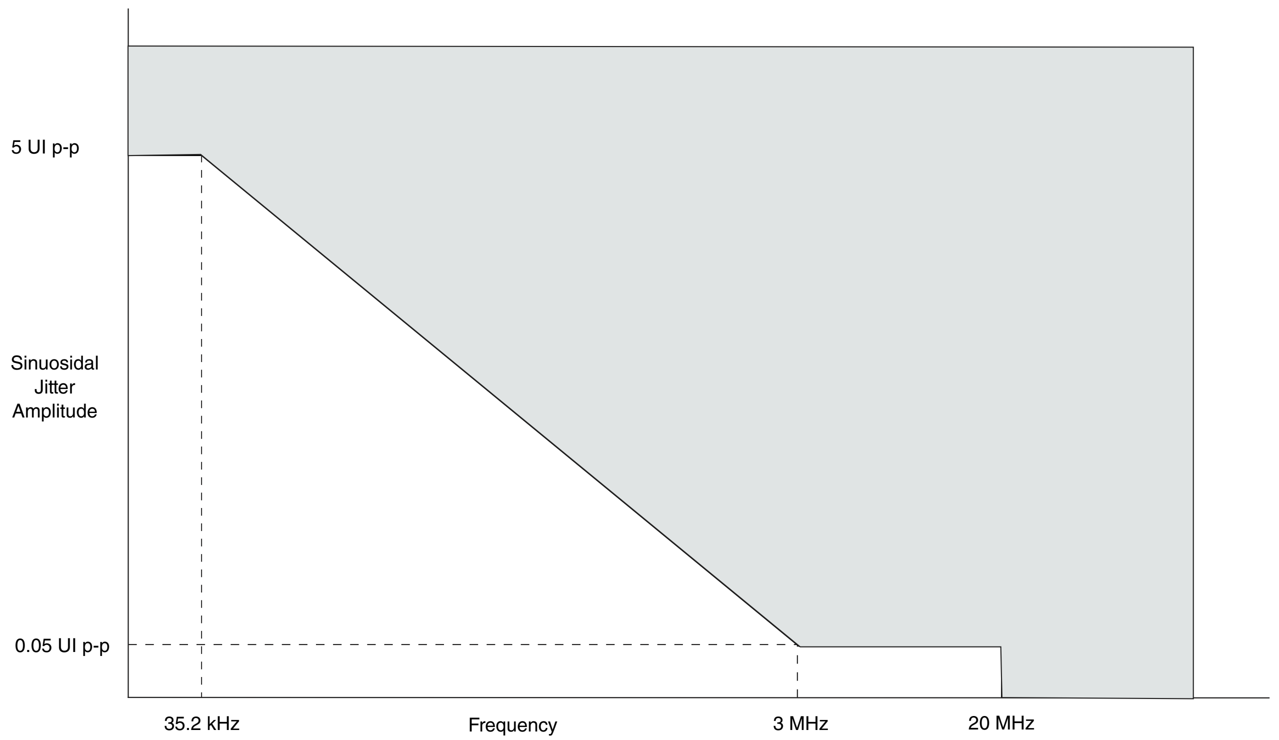


Figure 43. QSGMII single-frequency sinusoidal jitter limits

Table 113. 10GBase-KR receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Total jitter tolerance	R_{TJ}	-	-	Per IEEE Std 802.3ap-2007, Annex 69a.	UI p-p
Random jitter	R_{RJ}	-	-	0.13	UI p-p
Sinusoidal jitter (maximum)	R_{SJ-max}	-	-	0.115	UI p-p
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p

3.17 I²C interface

This section describes the DC and AC electrical characteristics for the I²C interface.

3.17.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interface when operating at DV_{DD} = 3.3 V.

Table 114. I²C DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	2
Output low voltage (DV_{DD} = min, IOL = 3 mA, DV_{DD} > 2V)	V_{OL}	-	0.4	V	3
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	4
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} (min) and 0.9 x DV_{DD} (max))	I_I	-50.0	50.0	μA	5
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
3. The output voltage (open drain or open collector) condition = 3 mA sink current.
4. See the chip reference manual for information about the digital filter used.
5. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.

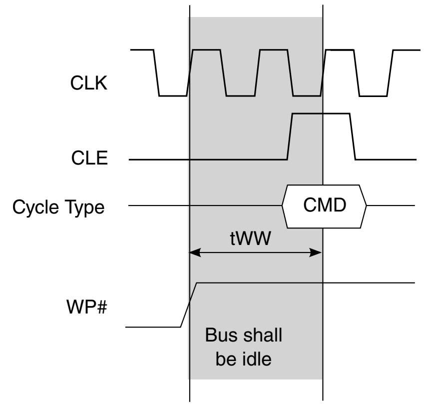


Figure 66. t_{WW} timings

This figure shows the $t_{IBIXKH4}$ timings.

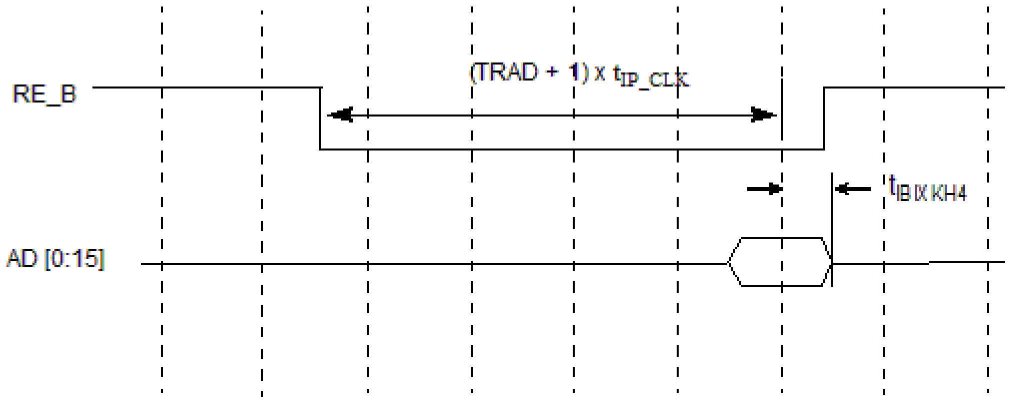


Figure 67. $t_{IBIXKH4}$ timings

3.18.2.6 IFC-NAND NVDDR AC timing specification

The table below describes the AC timing specifications for the IFC-NAND NVDDR interface. These specifications are compliant to NVDDR mode of ONFI specification revision 3.0.

Table 125. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Access window of DQ[7:0] from CLK	t_{AC}	I	3 - 150 (ps)	20 + 150 (ps)	ns	Figure 71
Address cycle to data loading time	t_{ADL}	I	TADL	-	t_{IP_CLK}	Figure 72

Table continues on the next page...

Table 125. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
WP# transition to command cycle	t_{WW}	O	TWW - 150 (ps)	TWW + 150 (ps)	t_{IP_CLK}	Figure 77
NOTE: 1. t_{IP_CLK} is the clock period of IP clock (on which IFC IP is running). Note that that the IFC IP clcok doesn't come out of device.						

The following diagrams show the AC timing for the IFC-NAND NVDDR interface.

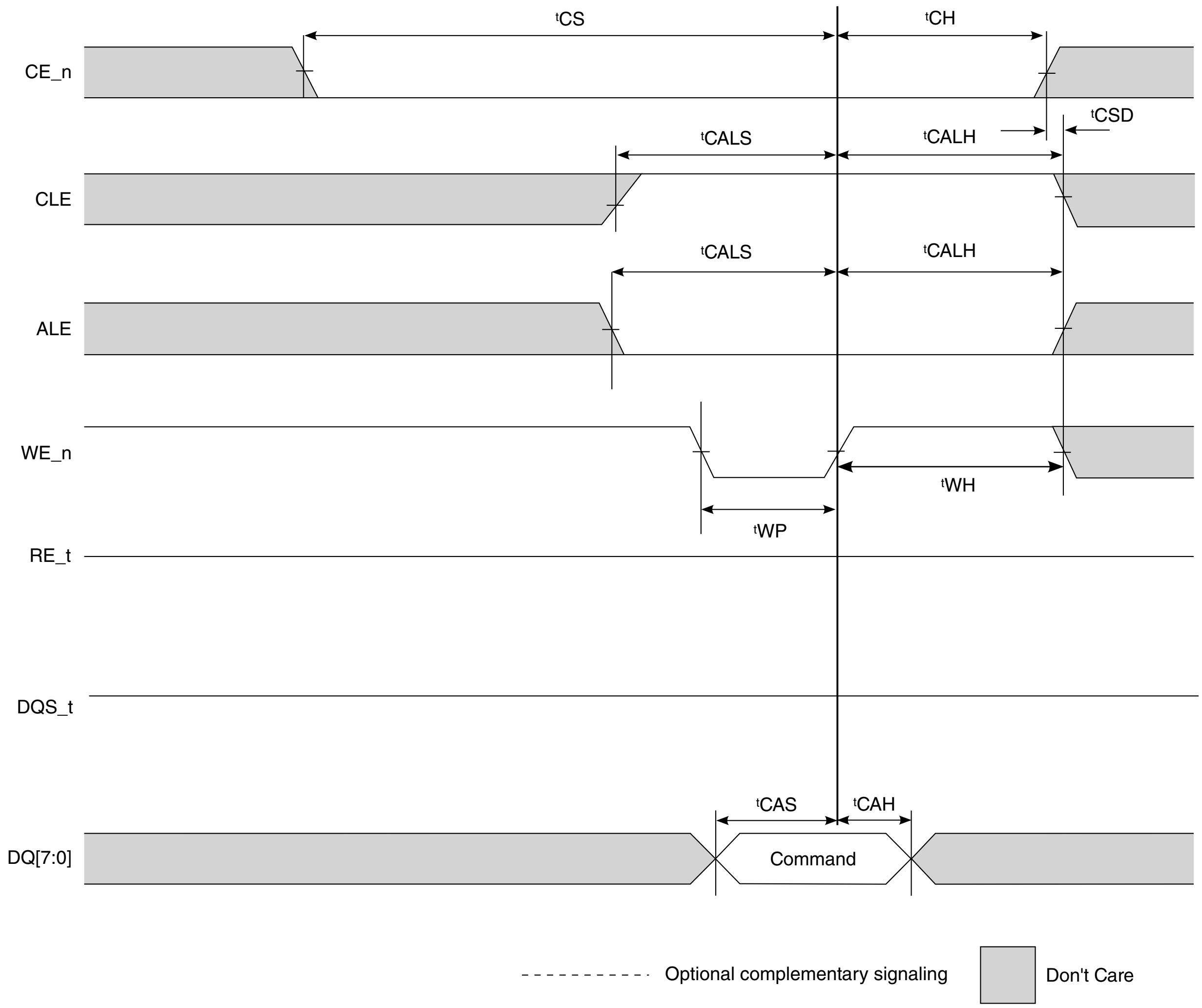


Figure 68. Command cycle

Table 126. JTAG DC electrical characteristics (OV_{DD} = 1.8 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. For recommended operating conditions, see Table 3.					
2. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in the Recommended Operating Conditions table.					
3. Note that the symbol V_{IN}, in this case, represents the OVIN symbol found in the Recommended Operating Conditions table.					
4. TDI, TMS, and TRST_B have internal pull-ups per the IEEE Std. 1149.1 specification.					

3.19.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 78, Figure 79, Figure 80, and Figure 81.

Table 127. JTAG AC timing specifications[1]

Parameter	Symbol	Min	Max	Unit	Notes
JTAG external clock frequency of operation	F_{JTG}	0.0	33.3	MHz	-
JTAG external clock cycle time	t_{JTG}	30.0	-	ns	-
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15.0	-	ns	-
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0.0	2.0	ns	-
TRST_B assert time	t_{TRST}	25.0	-	ns	TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.
Input setup times	t_{JTDVKH}	4.0	-	ns	TA_BB_TMP_DETECT pin requires 13.5ns input setup time for the board JTAG test to go through runTESTIdle.
Input hold times	t_{JTDXKH}	10.0	-	ns	-
Output valid times: boundary-scan data	t_{JTKLDV}	-	15.0	ns	All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
Output valid times: TDO	t_{JTKLDV}	-	10.0	ns	All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in

Table continues on the next page...

5.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

5.2 Temperature diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A). These devices feature series resistance cancellation using three current measurements, where up to 1.5 kΩ of resistance can be automatically cancelled from the temperature result, allowing noise filtering and a more accurate reading.

The following are the specifications of the chip's on-board temperature diode:

Operating range: TBD

Ideality factor TBD; Temperature range TBD

5.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 95. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 15 pounds force.