
**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-A53 |
| Number of Cores/Bus Width | 8 Core, 64-Bit |
| Speed | 1.6GHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR4 |
| Graphics Acceleration | - |
| Display & Interface Controllers | - |
| Ethernet | 10GbE (2), 1GbE (8) |
| SATA | SATA 6Gbps (1) |
| USB | USB 3.0 (2) + PHY |
| Voltage - I/O | - |
| Operating Temperature | -40°C ~ 105°C |
| Security Features | Secure Boot, TrustZone® |
| Package / Case | 780-BFBGA, FCBGA |
| Supplier Device Package | 780-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088axe7q1a |

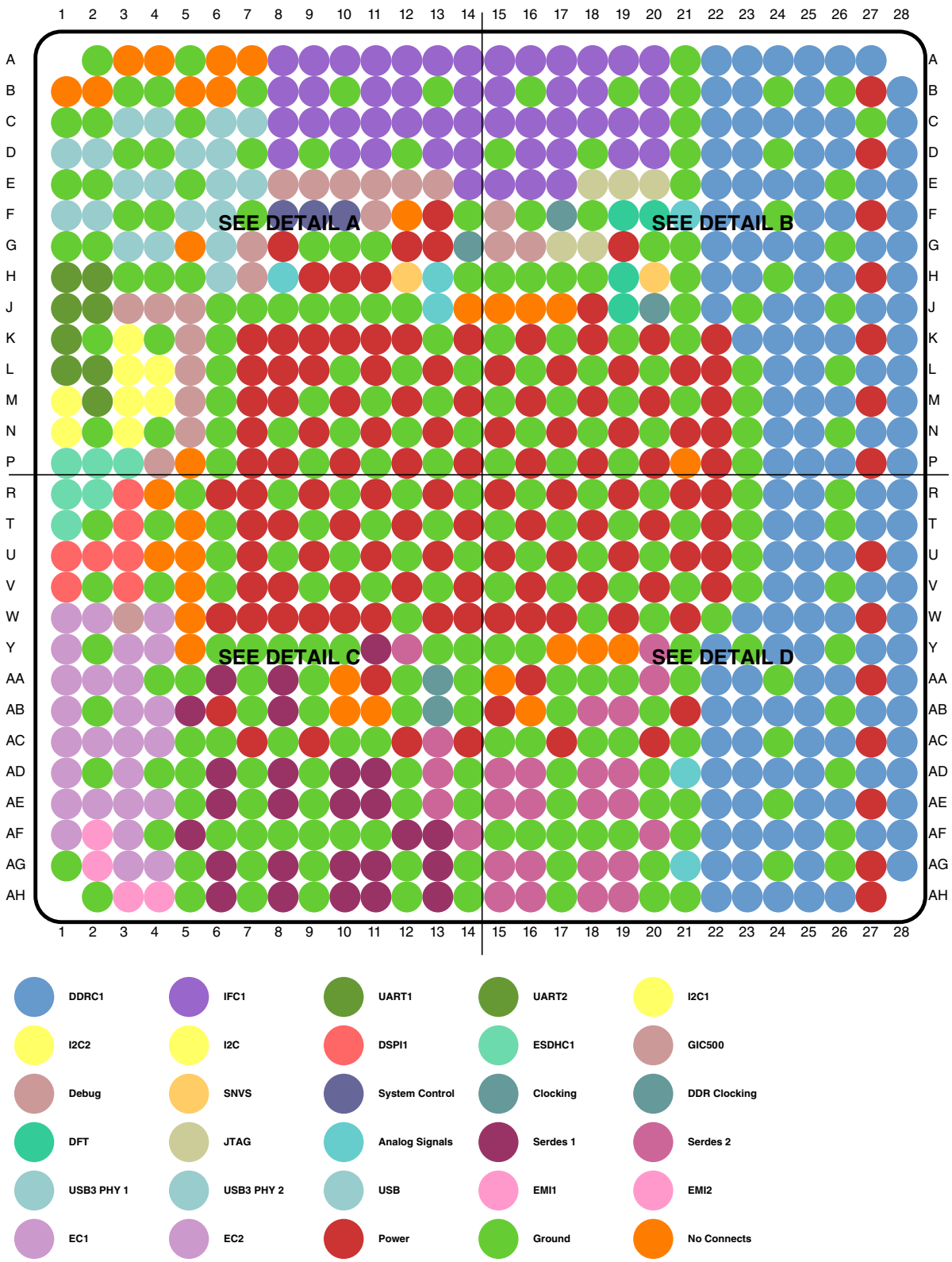


**Figure 2. Complete BGA Map for the LS1088A**

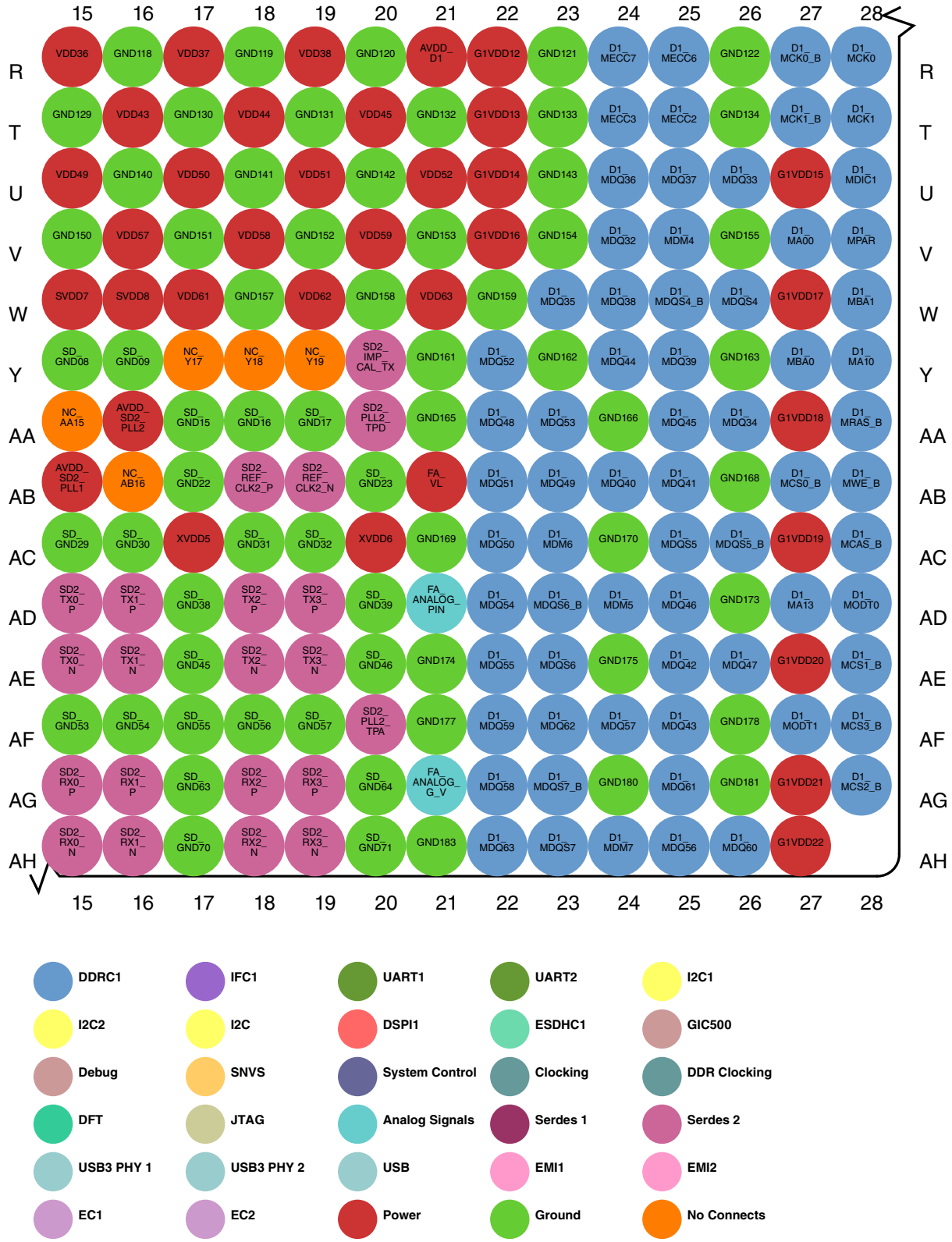


**Figure 6. Detail D**

## Table 1. Pinout list by bus (continued)

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| **D1_MCS3_B** | Chip Select | AF28 | O | $G1V_{DD}$ | 1 |
| **D1_MDIC0** | Driver Impedence Calibration | P28 | IO | $G1V_{DD}$ | 3 |
| **D1_MDIC1** | Driver Impedence Calibration | U28 | IO | $G1V_{DD}$ | 3 |
| **D1_MDM0** | Data Mask | B23 | O | $G1V_{DD}$ | --- |
| **D1_MDM1** | Data Mask | H22 | O | $G1V_{DD}$ | --- |
| **D1_MDM2** | Data Mask | E25 | O | $G1V_{DD}$ | --- |
| **D1_MDM3** | Data Mask | J25 | O | $G1V_{DD}$ | --- |
| **D1_MDM4** | Data Mask | V25 | O | $G1V_{DD}$ | --- |
| **D1_MDM5** | Data Mask | AD24 | O | $G1V_{DD}$ | --- |
| **D1_MDM6** | Data Mask | AC23 | O | $G1V_{DD}$ | --- |
| **D1_MDM7** | Data Mask | AH24 | O | $G1V_{DD}$ | --- |
| **D1_MDM8** | Data Mask | P24 | O | $G1V_{DD}$ | --- |
| **D1_MDQ00** | Data | C22 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ01** | Data | A23 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ02** | Data | C26 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ03** | Data | A27 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ04** | Data | B22 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ05** | Data | A22 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ06** | Data | B25 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ07** | Data | A26 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ08** | Data | E22 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ09** | Data | D22 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ10** | Data | F23 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ11** | Data | G23 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ12** | Data | G22 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ13** | Data | F22 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ14** | Data | C24 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ15** | Data | E23 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ16** | Data | D26 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ17** | Data | E24 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ18** | Data | G24 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ19** | Data | H25 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ20** | Data | C25 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ21** | Data | D25 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ22** | Data | G25 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ23** | Data | H26 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ24** | Data | K23 | IO | $G1V_{DD}$ | --- |
| **D1_MDQ25** | Data | J24 | IO | $G1V_{DD}$ | --- |

*Table continues on the next page...*

## Table 1. Pinout list by bus (continued)

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| **DIFF_SYSCLK_B** | Single Source System Clock Differential (negative) | AB13 | I | $SV_{DD}$ | 20 |
| **RTC**/GPIO3_30 | Real Time Clock | F17 | I | $OV_{DD}$ | 1 |
| **SYSCLK** | System Clock | G14 | I | $OV_{DD}$ | --- |
| **DDR Clocking** | | | | | |
| **DDRCLK** | DDR Controller Clock | J20 | I | $OV_{DD}$ | --- |
| **DFT** | | | | | |
| **JTAG_BSR_VSEL** | Reserved | J19 | I | $OV_{DD}$ | 15 |
| **SCAN_MODE_B** | Reserved | H19 | I | $OV_{DD}$ | 10 |
| **TBSCAN_EN_B** | Test Boundary Scan Enable | F19 | I | $OV_{DD}$ | 6 |
| **TEST_SEL_B** | Reserved | F20 | I | $OV_{DD}$ | 10 |
| **JTAG** | | | | | |
| **TCK** | Test Clock | E18 | I | $OV_{DD}$ | --- |
| **TDI** | Test Data In | G17 | I | $OV_{DD}$ | 9 |
| **TDO** | Test Data Out | E20 | O | $OV_{DD}$ | 2 |
| **TMS** | Test Mode Select | G18 | I | $OV_{DD}$ | 9 |
| **TRST_B** | Test Reset | E19 | I | $OV_{DD}$ | 9 |
| **Analog Signals** | | | | | |
| **D1_TPA** | Reserved | F21 | IO | | 12 |
| **FA_ANALOG_G_V** | Reserved | AG21 | IO | | 15 |
| **FA_ANALOG_PIN** | Reserved | AD21 | IO | | 15 |
| **TD1_ANODE** | Thermal diode anode | J13 | IO | | 17 |
| **TD1_CATHODE** | Thermal diode cathode | H13 | IO | | 17 |
| **TH_TPA** | Reserved | H8 | - | - | 12 |
| **SerDes 1** | | | | | |
| **SD1_IMP_CAL_RX** | SerDes Receive Impedence Calibration | Y11 | I | $SV_{DD}$ | 11 |
| **SD1_IMP_CAL_TX** | SerDes Transmit Impedance Calibration | AA6 | I | $XV_{DD}$ | 16 |
| **SD1_PLL1_TPA** | SerDes PLL 1 Test Point Analog | AF12 | O | AVDD_SD1_PLL1 | 12 |
| **SD1_PLL1_TPD** | SerDes Test Point Digital | AF13 | O | $XV_{DD}$ | 12 |
| **SD1_PLL2_TPA** | SerDes PLL 2 Test Point Analog | AF5 | O | AVDD_SD1_PLL2 | 12 |
| **SD1_PLL2_TPD** | SerDes Test Point Digital | AB5 | O | $XV_{DD}$ | 12 |
| **SD1_REF_CLK1_N** | SerDes PLL 1 Reference Clock Complement | AH13 | I | $SV_{DD}$ | --- |
| **SD1_REF_CLK1_P** | SerDes PLL 1 Reference Clock | AG13 | I | $SV_{DD}$ | --- |
| **SD1_REF_CLK2_N** | SerDes PLL 2 Reference Clock Complement | AB8 | I | $SV_{DD}$ | --- |

*Table continues on the next page...*

## Table 1. Pinout list by bus (continued)

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| **EC1_RXD2**/GPIO2_30 | Receive Data | Y1 | I | $LV_{DD}$ | 1 |
| **EC1_RXD3**/GPIO2_29 | Receive Data | W2 | I | $LV_{DD}$ | 1 |
| **EC1_RX_CLK**/GPIO4_13 | Receive Clock | W1 | I | $LV_{DD}$ | 1 |
| **EC1_RX_DV**/GPIO4_14 | Receive Data Valid | AB1 | I | $LV_{DD}$ | 1 |
| **EC1_TXD0**/GPIO2_25 | Transmit Data | AB3 | O | $LV_{DD}$ | 1 |
| **EC1_TXD1**/GPIO2_24 | Transmit Data | AA3 | O | $LV_{DD}$ | 1 |
| **EC1_TXD2**/GPIO2_23 | Transmit Data | Y4 | O | $LV_{DD}$ | 1 |
| **EC1_TXD3**/GPIO2_22 | Transmit Data | Y3 | O | $LV_{DD}$ | 1 |
| **EC1_TX_EN**/GPIO2_26 | Transmit Enable | AB4 | O | $LV_{DD}$ | 1, 14 |
| **Ethernet Controller 2** | | | | | |
| **EC2_GTX_CLK**/GPIO4_20 | Transmit Clock Out | AC4 | O | $LV_{DD}$ | 1 |
| **EC2_GTX_CLK125**/GPIO4_21 | Reference Clock | AG4 | I | $LV_{DD}$ | 1 |
| **EC2_RXD0**/GPIO4_25/ TSEC_1588_TRIG_IN2 | Receive Data | AE2 | I | $LV_{DD}$ | 1 |
| **EC2_RXD1**/GPIO4_24/ TSEC_1588_PULSE_OUT1 | Receive Data | AE1 | I | $LV_{DD}$ | 1 |
| **EC2_RXD2**/GPIO4_23 | Receive Data | AD1 | I | $LV_{DD}$ | 1 |
| **EC2_RXD3**/GPIO4_22 | Receive Data | AC2 | I | $LV_{DD}$ | 1 |
| **EC2_RX_CLK**/GPIO4_26/ TSEC_1588_CLK_IN | Receive Clock | AC1 | I | $LV_{DD}$ | 1 |
| **EC2_RX_DV**/GPIO4_27/ TSEC_1588_TRIG_IN1 | Receive Data Valid | AF1 | I | $LV_{DD}$ | 1 |
| **EC2_TXD0**/GPIO4_18/ TSEC_1588_PULSE_OUT2 | Transmit Data | AF3 | O | $LV_{DD}$ | 1 |
| **EC2_TXD1**/GPIO4_17/ TSEC_1588_CLK_OUT | Transmit Data | AE4 | O | $LV_{DD}$ | 1 |
| **EC2_TXD2**/GPIO4_16/ TSEC_1588_ALARM_OUT1 | Transmit Data | AE3 | O | $LV_{DD}$ | 1 |
| **EC2_TXD3**/GPIO4_15/ TSEC_1588_ALARM_OUT2 | Transmit Data | AD3 | O | $LV_{DD}$ | 1 |
| **EC2_TX_EN**/GPIO4_19 | Transmit Enable | AG3 | O | $LV_{DD}$ | 1, 14 |
| **General Purpose Input/Output** | | | | | |
| GPIO1_00/**IFC_AD00**/ cfg_gpinput0 | General Purpose Input/Output | B12 | O | $OV_{DD}$ | 1, 4 |
| GPIO1_01/**IFC_AD01**/ cfg_gpinput1 | General Purpose Input/Output | A11 | O | $OV_{DD}$ | 1, 4 |
| GPIO1_02/**IFC_AD02**/ cfg_gpinput2 | General Purpose Input/Output | B11 | O | $OV_{DD}$ | 1, 4 |
| GPIO1_03/**IFC_AD03**/ cfg_gpinput3 | General Purpose Input/Output | A10 | O | $OV_{DD}$ | 1, 4 |
| GPIO1_04/**IFC_AD04**/ cfg_gpinput4 | General Purpose Input/Output | A9 | O | $OV_{DD}$ | 1, 4 |

*Table continues on the next page...*

## Table 1. Pinout list by bus (continued)

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| GND141 | Core, Platform and PLL Ground | U18 | --- | --- | --- |
| GND142 | Core, Platform and PLL Ground | U20 | --- | --- | --- |
| GND143 | Core, Platform and PLL Ground | U23 | --- | --- | --- |
| GND144 | Core, Platform and PLL Ground | V2 | --- | --- | --- |
| GND145 | Core, Platform and PLL Ground | V4 | --- | --- | --- |
| GND146 | Core, Platform and PLL Ground | V6 | --- | --- | --- |
| GND147 | Core, Platform and PLL Ground | V9 | --- | --- | --- |
| GND148 | Core, Platform and PLL Ground | V11 | --- | --- | --- |
| GND149 | Core, Platform and PLL Ground | V13 | --- | --- | --- |
| GND150 | Core, Platform and PLL Ground | V15 | --- | --- | --- |
| GND151 | Core, Platform and PLL Ground | V17 | --- | --- | --- |
| GND152 | Core, Platform and PLL Ground | V19 | --- | --- | --- |
| GND153 | Core, Platform and PLL Ground | V21 | --- | --- | --- |
| GND154 | Core, Platform and PLL Ground | V23 | --- | --- | --- |
| GND155 | Core, Platform and PLL Ground | V26 | --- | --- | --- |
| GND156 | Core, Platform and PLL Ground | W12 | --- | --- | --- |
| GND157 | Core, Platform and PLL Ground | W18 | --- | --- | --- |
| GND158 | Core, Platform and PLL Ground | W20 | --- | --- | --- |
| GND159 | Core, Platform and PLL Ground | W22 | --- | --- | --- |
| GND160 | Core, Platform and PLL Ground | Y2 | --- | --- | --- |
| GND161 | Core, Platform and PLL Ground | Y21 | --- | --- | --- |
| GND162 | Core, Platform and PLL Ground | Y23 | --- | --- | --- |

*Table continues on the next page...*

## Table 1. Pinout list by bus (continued)

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| SD_GND46 | SerDes core logic, transceiver, and PLL ground | AE20 | --- | --- | 18 |
| SD_GND47 | SerDes core logic, transceiver, and PLL ground | AF6 | --- | --- | 18 |
| SD_GND48 | SerDes core logic, transceiver, and PLL ground | AF7 | --- | --- | 18 |
| SD_GND49 | SerDes core logic, transceiver, and PLL ground | AF8 | --- | --- | 18 |
| SD_GND50 | SerDes core logic, transceiver, and PLL ground | AF9 | --- | --- | 18 |
| SD_GND51 | SerDes core logic, transceiver, and PLL ground | AF10 | --- | --- | 18 |
| SD_GND52 | SerDes core logic, transceiver, and PLL ground | AF11 | --- | --- | 18 |
| SD_GND53 | SerDes core logic, transceiver, and PLL ground | AF15 | --- | --- | 18 |
| SD_GND54 | SerDes core logic, transceiver, and PLL ground | AF16 | --- | --- | 18 |
| SD_GND55 | SerDes core logic, transceiver, and PLL ground | AF17 | --- | --- | 18 |
| SD_GND56 | SerDes core logic, transceiver, and PLL ground | AF18 | --- | --- | 18 |
| SD_GND57 | SerDes core logic, transceiver, and PLL ground | AF19 | --- | --- | 18 |
| SD_GND58 | SerDes core logic, transceiver, and PLL ground | AG5 | --- | --- | 18 |
| SD_GND59 | SerDes core logic, transceiver, and PLL ground | AG7 | --- | --- | 18 |
| SD_GND60 | SerDes core logic, transceiver, and PLL ground | AG9 | --- | --- | 18 |
| SD_GND61 | SerDes core logic, transceiver, and PLL ground | AG12 | --- | --- | 18 |
| SD_GND62 | SerDes core logic, transceiver, and PLL ground | AG14 | --- | --- | 18 |
| SD_GND63 | SerDes core logic, transceiver, and PLL ground | AG17 | --- | --- | 18 |
| SD_GND64 | SerDes core logic, transceiver, and PLL ground | AG20 | --- | --- | 18 |
| SD_GND65 | SerDes core logic, transceiver, and PLL ground | AH5 | --- | --- | 18 |
| SD_GND66 | SerDes core logic, transceiver, and PLL ground | AH7 | --- | --- | 18 |
| SD_GND67 | SerDes core logic, transceiver, and PLL ground | AH9 | --- | --- | 18 |

*Table continues on the next page...*

adjust the memory clocks by ½ applied cycle for data rates of 1866 MT/s or less and 9/16 applied cycle for data rates greater than 1866 MT/s. It is recommended that, during system validation, memory clocks are adjusted to best fit the particular system design.

This figure shows the DDR4 SDRAM interface output timing for the MCK to MDQS skew measurement ($t_{DDKHMH}$).

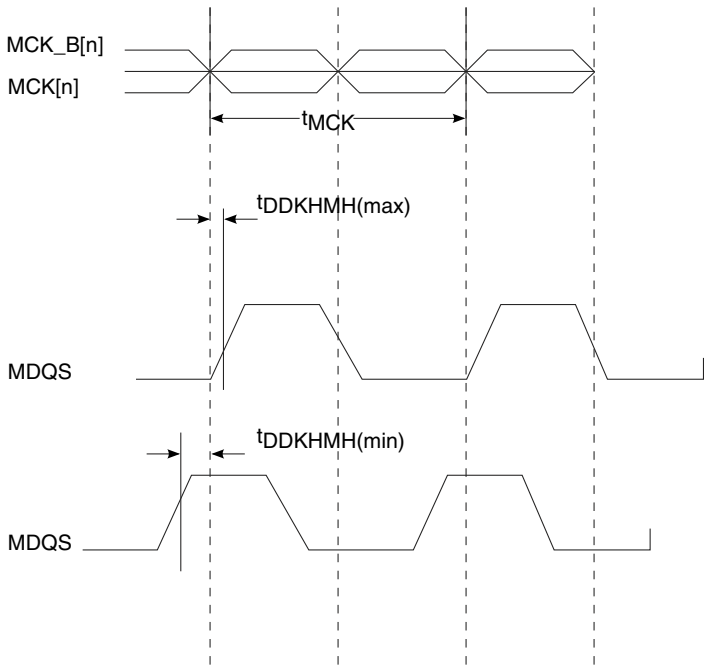


**Figure 12. $t_{DDKHMH}$ timing diagram**

This figure shows the DDR4 SDRAM output timing diagram.

## 3.12 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

### 3.12.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

**Table 33. eSDHC interface DC electrical characteristics ($E/DV_{DD}$=3.3 V)[3]**

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 0.7 x $E/DV_{DD}$ | - | V | 1 |
| Input low voltage | $V_{IL}$ | - | 0.25 x $E/DV_{DD}$ | V | 1 |
| Output high voltage ($I_{OH}$ = -100 µA at $E/DV_{DD}$ min) | $V_{OH}$ | 0.75 x $E/DV_{DD}$ | - | V | - |
| Output low voltage ( $I_{OL}$ = 100 µA at $E/DV_{DD}$ min) | $V_{OL}$ | - | 0.125 x $E/DV_{DD}$ | V | - |
| Output high voltage ($I_{OH}$ = -100 µA) | $V_{OH}$ | $E/DV_{DD}$ - 0.2 | - | V | 2 |
| Output low voltage ($I_{OL}$ = 2 mA) | $V_{OL}$ | - | 0.3 | V | 2 |
| Input/output leakage current | ($I_{IN}/I_{OZ}$) | -10 | 10 | µA | 2 |

**Notes:**

1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $EV_{IN}$ values found in the Table 3.
2. Open-drain mode is for MMC cards only.
3. At recommended operating conditions with $E/DV_{DD}$ = 3.3 V.

**Table 34. eSDHC interface DC electrical characteristics ($E/D/OV_{DD}$=1.8 V)[3]**

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 0.7 x $E/D/OV_{DD}$ | - | V | 1 |
| Input low voltage | $V_{IL}$ | - | 0.3 x $E/D/OV_{DD}$ | V | 1 |
| Output high voltage ($I_{OH}$ = -2 mA at $E/D/OV_{DD}$ min) | $V_{OH}$ | $E/D/OV_{DD}$ - 0.45 | - | V | - |
| Output low voltage ($I_{OL}$ = 2 mA at $EV_{DD}$ min) | $V_{OL}$ | - | 0.45 | V | - |
| Output high voltage ($I_{OH}$ = -100 µA) | $V_{OH}$ | $E/D/OV_{DD}$ - 0.2 | - | V | 2 |
| Output low voltage ($I_{OL}$ = 2 mA) | $V_{OL}$ | - | 0.3 | V | 2 |

*Table continues on the next page...*

### 3.14.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for the GPIO interface operating at $D/EV_{DD}$ = 3.3 V.

**Table 52. GPIO DC electrical characteristics ($D/EV_{DD}$ = 3.3 V)[1]**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 0.7 x $D/EV_{DD}$ | - | V | 2 |
| Input low voltage | $V_{IL}$ | - | 0.2 x $D/EV_{DD}$ | V | 2 |
| Input current ($V_{IN}$ = 0V or $V_{IN}$= $LV_{DD}$) | $I_{IN}$ | - | ±50 | μA | 3 |
| Output high voltage ($D/EV_{DD}$ = min, $I_{OH}$ = -2 mA) | $V_{OH}$ | 2.4 | - | V | - |
| Output low voltage ($D/EV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | - | 0.4 | V | - |
| 1. For recommended operating conditions, see Table 3.<br>2. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $DV_{IN}/EV_{IN}$ values found in Table 3.<br>3. The symbol $DV_{IN}/EV_{IN}$ represents the input voltage of the supply referenced in Table 3. | | | | | |

This table provides the DC electrical characteristics for the GPIO interface operating at $TV_{DD}$ = 2.5 V.

**Table 53. GPIO DC electrical characteristics ($TV_{DD}$ = 2.5 V)[1]**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 0.7 x $TV_{DD}$ | - | V | 2 |
| Input low voltage | $V_{IL}$ | - | 0.2 x $TV_{DD}$ | V | 2 |
| Input current ($V_{IN}$ = 0V or $V_{IN}$= $LV_{DD}$) | $I_{IN}$ | - | ±50 | μA | 3 |
| Output high voltage ($TV_{DD}$ = min, $I_{OH}$ = -1 mA) | $V_{OH}$ | 2.0 | - | V | - |
| Output low voltage ($TV_{DD}$ = min, $I_{OL}$ = 1 mA) | $V_{OL}$ | - | 0.4 | V | - |
| 1. For recommended operating conditions, see Table 3.<br>2. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $TV_{IN}$ values found in Table 3.<br>3. The symbol $TV_{IN}$ represents the input voltage of the supply referenced in Table 3. | | | | | |

This table provides the DC electrical characteristics for the GPIO interface operating at $D/E/TV_{DD}$ = 1.8 V.

**Table 54. GPIO DC electrical characteristics ($D/E/TV_{DD}$ = 1.8 V)[1]**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 0.7 x $D/E/TV_{DD}$ | - | V | 2 |

*Table continues on the next page...*

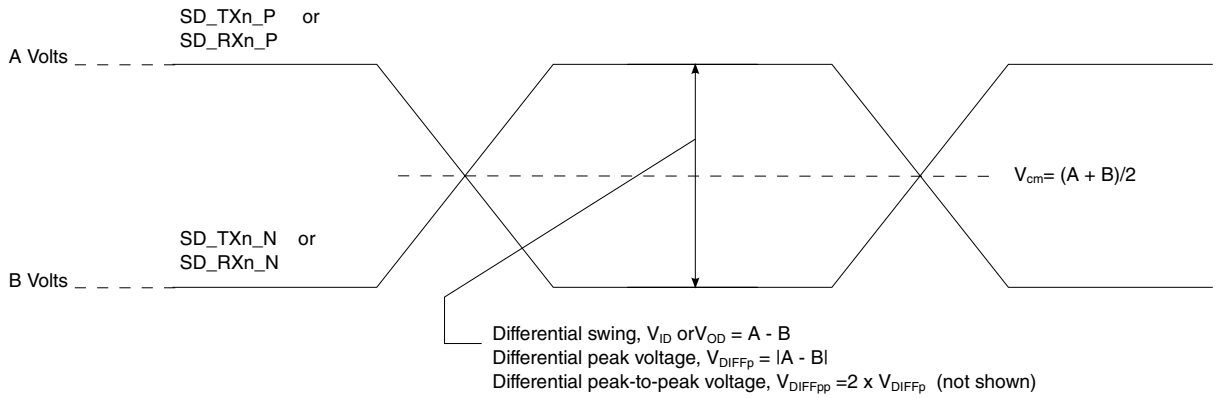


**Figure 29. Differential voltage definitions for transmitter or receiver**

Using this waveform, the definitions are as described in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

**Single-Ended Swing**

The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred to as each signal wire's single-ended swing.

**Differential Output Voltage, $V_{OD}$ (or Differential Output Swing)**

The differential output voltage (or swing) of the transmitter, $V_{OD}$, is defined as the difference of the two complementary output voltages: $V_{SD\_TXn\_P}$ - $V_{SD\_TXn\_N}$. The $V_{OD}$ value can be either positive or negative.

**Differential Input Voltage, $V_{ID}$ (or Differential Input Swing)**

The differential input voltage (or swing) of the receiver, $V_{ID}$, is defined as the difference of the two complementary input voltages: $V_{SD\_RXn\_P}$- $V_{SD\_RXn\_N}$. The $V_{ID}$ value can be either positive or negative.

**Differential Peak Voltage, $V_{DIFFp}$**

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp}$ = |A - B| volts.

**Differential Peak-to-Peak, $V_{DIFFp-p}$**

Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 x $V_{DIFFp}$ = 2 x |(A - B)| volts, which is twice the differential swing in amplitude, or twice the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p}$ = 2 x |$V_{OD}$|.

**Differential Waveform**

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example)

**Table 69. PCI Express 3.0 (8 GT/s) differential transmitter output DC characteristics ($XV_{DD}$ = 1.35 V)[3]**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Full swing transmitter voltage with no TX Eq | $V_{TX-FS-NO-EQ}$ | 800 | — | 1300 | mVp-p | See Note 1. |
| Reduced swing transmitter voltage with no TX Eq | $V_{TX-RS-NO-EQ}$ | 400 | — | 1300 | mV | See Note 1. |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO-3.5dB}$ | 3.0 | 3.5 | 4.0 | dB | — |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO-6.0dB}$ | 5.5 | 6.0 | 6.5 | dB | — |
| Minimum swing during EIEOS for full swing | $V_{TX-EIEOS-FS}$ | 250 | — | — | mVp-p | See Note 2 |
| Minimum swing during EIEOS for reduced swing | $V_{TX-EIEOS-RS}$ | 232 | — | — | mVp-p | See Note 2 |
| DC differential transmitter impedance | $Z_{TX-DIFF-DC}$ | 80 | 100 | 120 | Ω | Transmitter DC differential mode low impedance |
| Transmitter DC Impedance | $Z_{TX-DC}$ | 40 | 50 | 60 | Ω | Required transmitter D+ as well as D- DC impedance during all states |

**Notes:**

1. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.

2. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 $mV_{P-P}$ at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.

3. For recommended operating conditions, see Table 3.

### 3.16.4.3.2 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

**Table 70. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications ($SV_{DD}$ = 0.9V/1.0 V)[4]**

| Parameter | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Differential input peak-to-peak voltage | $V_{RX-DIFFp-p}$ | 175 | 1000 | 1200 | mV | $V_{RX-DIFFp-p}$ = 2 x $\|V_{RX-D+}$ - $V_{RX-D-}\|$ See Note 1. |

*Table continues on the next page...*

### 3.16.8.3 XFI AC timing specifications

**NOTE**

The AC specifications do not include RefClk jitter.

This table defines the XFI transmitter AC timing specifications.

**Table 104. XFI transmitter AC timing specifications**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Transmitter baud Rate | $T_{BAUD}$ | 10.3125-100ppm | 10.3125 | 10.3125+100ppm | Gb/s |
| Unit Interval | UI | - | 96.96 | - | ps |
| Deterministic jitter | $D_J$ | - | - | 0.15 | UI p-p |
| Total jitter tolerance | $T_J$ | - | - | 0.3 | UI p-p |

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

**Table 105. XFI receiver AC timing specifications**

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Unit Interval | UI | - | 96.96 | - | ps | - |
| Receiver baud rate | $R_{BAUD}$ | 10.3125-100ppm | 10.3125 | 10.3125+100ppm | Gb/s | - |
| Total non-EQJ jitter | $T_{NON-EQJ}$ | - | - | 0.45 | UI p-p | 1 |
| Total jitter tolerance | $T_J$ | - | - | 0.65 | UI p-p | 1, 2 |

1. The total jitter (TJ) consists of Random Jitter (RJ), Duty Cycle Distortion (DCD), Periodic Jitter (PJ), and Inter-Symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (RJ), and periodic jitter (PJ). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = TJ - ISI = RJ + DCD + PJ.

2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.

This figure shows the sinusoidal jitter tolerance of XFI receiver.

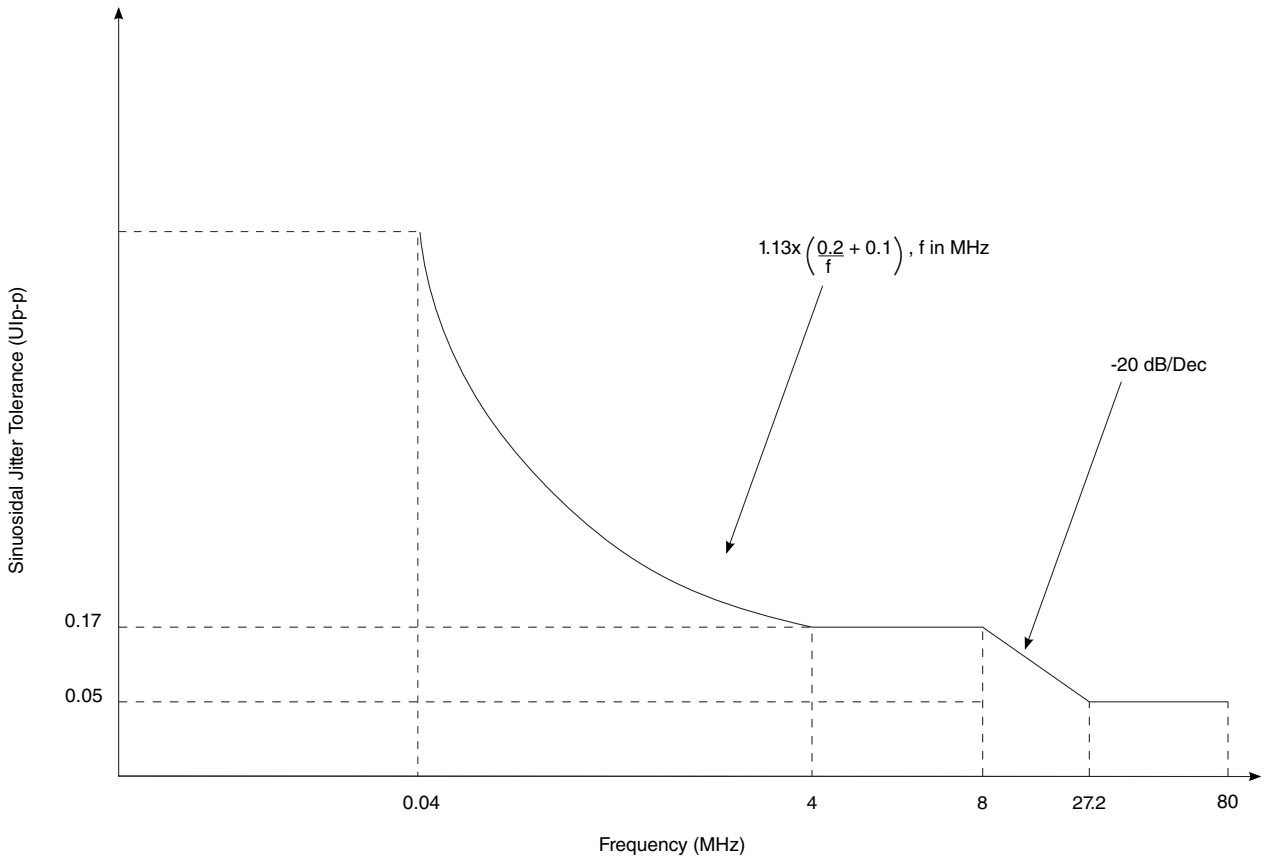


**Figure 44. XFI host receiver input sinusoidal jitter tolerance**

## 3.16.9 1000Base-KX interface

This section describes the electrical characteristics for the 1000Base-KX interface. Only AC-coupled operation is supported.

### 3.16.9.1 1000Base-KX DC electrical characteristics

This table describes the 1000Base-KX SerDes transmitter DC electrical characteristics at TP1 per IEEE Std 802.3ap-2007. Transmitter DC electrical characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N).

**Table 106. 1000Base-KX transmitter DC electrical characteristics[1]**

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Output differential voltage | $V_{TX\text{-}DIFFp\text{-}p}$ | 800.0 | - | 1600.0 | mV | 2 |

*Table continues on the next page...*

## Table 125. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V) (continued)

| Parameter | Symbol | I/O | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) Fast | tCADf | O | TCAD - 150 (ps) | TCAD + 150 (ps) | $t_{IP\_CLK}$ | Figure 68 |
| Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) slow | tCADs | O | TCAD - 150 (ps) | TCAD + 150 (ps) | $t_{IP\_CLK}$ | Figure 68 |
| Command/address DQ hold time | $t_{CAH}$ | O | 2 + 150 (ps) | - | ns | Figure 68 |
| CLE and ALE hold time | $t_{CALH}$ | O | 2 + 150 (ps) | - | ns | Figure 68 |
| CLE and ALE setup time | $t_{CALS}$ | O | 2 + 150 (ps) | - | ns | Figure 68 |
| Command/address DQ setup time | $t_{CAS}$ | O | 2 + 150 (ps) | - | ns | Figure 68 |
| CE# hold time | $t_{CH}$ | O | 2 + 150 (ps) | - | ns | Figure 68 |
| Average clock cycle time, also known as tCK | $t_{CK}$(avg) or $t_{CK}$ | O | 10 | - | ns | Figure 68 |
| Absolute clock period, measured from rising edge to the next consecutive rising edge | $t_{CK}$(abs) | O | tCK(avg) + tJIT(per) min | tCK(avg) + tJIT(per) max | ns | Figure 68 |
| Clock cycle high | $t_{CKH}$(abs) | O | 0.45 | 0.55 | tCK | Figure 68 |
| Clock cycle low | $t_{CKL}$(abs) | O | 0.45 | 0.55 | tCK | Figure 68 |
| Data input end to W/R# high B16 | $t_{CKWR}$ | O | TCKWR - 150 (ps) | TCKWR + 150 (ps) | $t_{IP\_CLK}$ | Figure 71 |
| CE# setup time | $t_{CS}$ | O | TCS - 150 (ps) | TCS + 150 (ps) | $t_{IP\_CLK}$ | Figure 70 |
| Data DQ hold time | $t_{DH}$ | O | 1050 | - | ps | Figure 70 |
| Access window of DQS from CLK | $t_{DQSCK}$ | I | - | 20 + 150 (ps) | ns | Figure 71 |
| W/R# low to DQS/DQ driven by device | $t_{DQSD}$ | I | -150 (ps) | 18 + 150 (ps) | ns | Figure 71 |
| DQS output high pulse width | $t_{DQSH}$ | O | 0.45 | 0.55 | tCK | Figure 70 |
| W/R# high to DQS/DQ tri-state by device | $t_{DQSHZ}$ | O | RHZ - 150 (ps) | RHZ + 150 (ps) | $t_{IP\_CLK}$ | Figure 68 |
| DQS output low pulse width | $t_{DQSL}$ | O | 0.45 | 0.55 | tCK | Figure 70 |

*Table continues on the next page...*

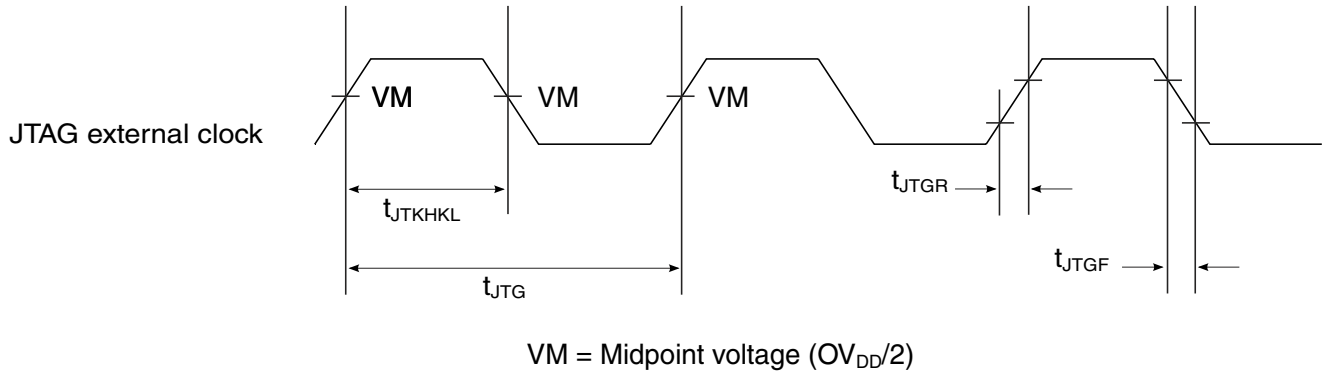


**Figure 79. JTAG clock input timing diagram**

This figure shows the TRST_B timing diagram.

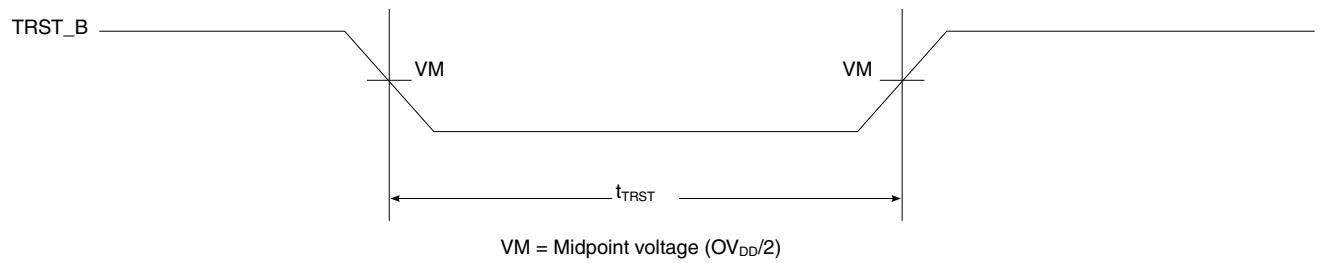


**Figure 80. TRST_B timing diagram**

This figure shows the boundary-scan timing diagram.

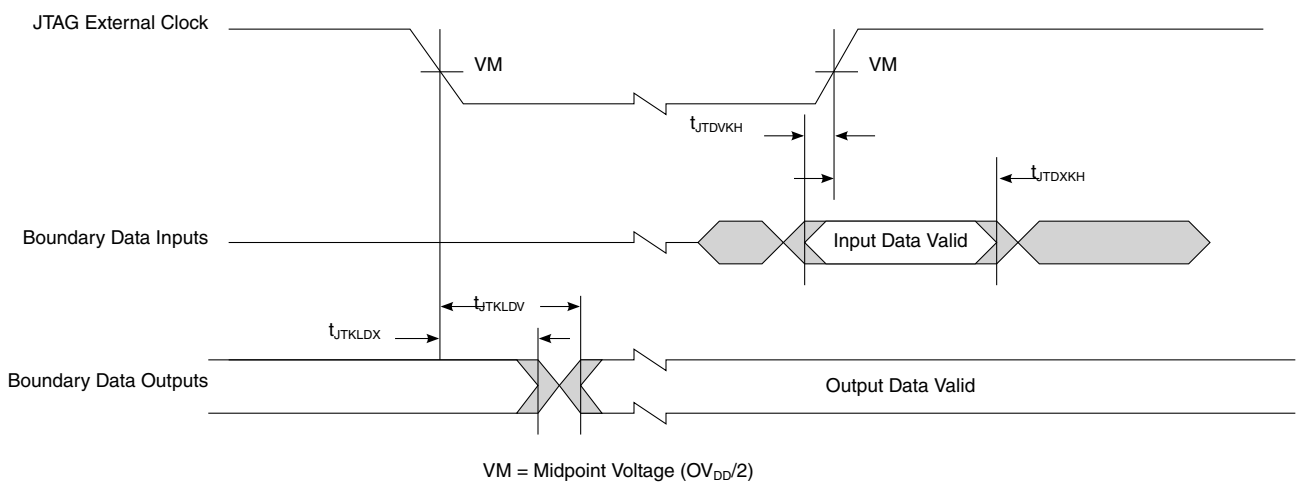


**Figure 81. Boundary-scan timing diagram**

# 3.20 Quad serial peripheral interface (QuadSPI)

This section describes the DC and AC electrical characteristics for the QuadSPI interface.

## 3.20.1 QuadSPI DC electrical characteristics

This table provides the DC electrical characteristics for the QuadSPI interface operating at $OV_{DD}$ = 1.8V.

**Table 128. QuadSPI DC electrical characteristics[1]**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 0.7 x $OV_{DD}$ | - | V | 2 |
| Input low voltage | $V_{IL}$ | - | 0.3 x $OV_{DD}$ | V | 2 |
| Input current (0V ≤ $V_{IN}$ ≤ $OV_{DD}$) | $I_{IN}$ | - | ±50 | μA | 3 |
| Output high voltage ($OV_{DD}$ = min, $I_{OH}$ = -100 μA) | $V_{OH}$ | $OV_{DD}$ - 0.2 | - | V | - |
| Output low voltage ($OV_{DD}$ = min, $I_{OL}$ = 100 μA) | $V_{OL}$ | - | 0.2 | V | - |

1. For recommended operating conditions, see Table 3.

2. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $OV_{IN}$ values found in Table 3.

3. Note that the symbol $OV_{IN}$ represents the input voltage of the supply referenced in the Recommended Operating Conditions table.

## 3.20.2 QuadSPI AC timing specifications

This section describes the QuadSPI timing specifications in both SDR and DDR modes. All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing figures in this section.

This table provides the QuadSPI input and output timing in SDR mode (MCR[DQS_EN] = 0, regarding to the 1st sample point. See qSPI_SMPR[xSDLY, xSPHS] in the corresponding chip reference manual for different sampling points). Note that T represents the clock period, j represents qSPI_FLSHCR[TCSH], and k depends on qSPI_FLSHCR[TCSS].

**Table 129. QuadSPI SDR mode input and output timing**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Clock rise/fall time | $T_{RISE}/T_{FALL}$ | 1.0 | - | ns |
| CS output hold time | $t_{NIKHOX2}$ | -3.3 + j * T | - | ns |
| CS output delay | $t_{NIKHOV2}$ | -3.0 + k * T | - | ns |

*Table continues on the next page...*

This table provides the QuadSPI input and output timing in DDR mode with external DQS/delay chain (MCR[DQS_EN] = 1, regarding to the 1st sample point). Note that T represents the clock period, j depends on the value of qSPI_FLSHCR[TCSH], k depends on qSPI_FLSHCR[TCSS], and m depends on QSPI_FLSHCR[TDH].

**Table 131. QuadSPI DDR mode input and output timing**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Clock rise/fall time | $T_{RISE}/T_{FALL}$ | 1.0 | - | ns |
| CS output hold time | $t_{NIKHOX2}$ | 3.3 + T * j | - | ns |
| CS output delay | $t_{NIKHOV2}$ | -3.0 + k * T | | ns |
| DQS to data skew | $t_{NIDSH}/t_{NIIDSL}$ | -0.9 | 0.9 | ns |
| Output data valid | $t_{NIKHOV}$ | - | 0.9 + m * T/8 | ns |
| Output data hold | $t_{NIKHOX}$ | -0.9 + m * T/8 | - | ns |

This figure shows the QuadSPI AC timing in DDR mode.

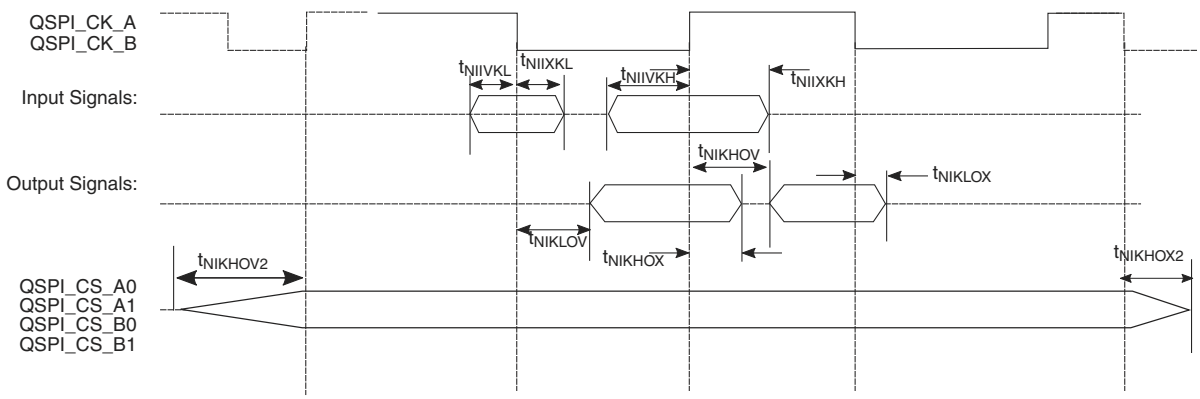


**Figure 83. QuadSPI AC timing — DDR mode**

This figure shows the QuadSPI data input timing in DDR mode with an external DQS.

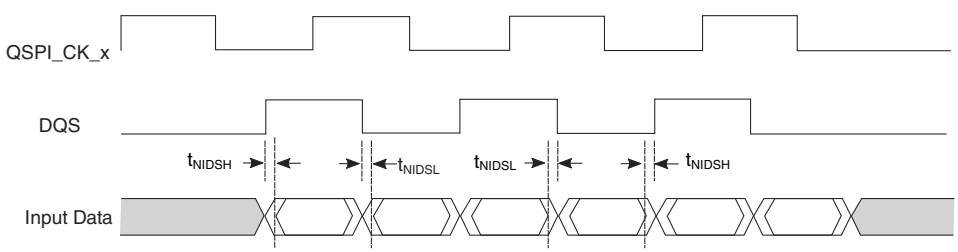


**Figure 84. QuadSPI input AC timing — DDR mode with an external DQS**

**Table 147. Processor, platform, and memory clocking specifications**

| Characteristic | Maximum processor core frequency | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | 1200 MHz | | 1400 MHz | | 1600 MHz | | | |
| | Min | Max | Min | Max | Min | Max | | |
| Core cluster group PLL frequency | 600 | 1200 | 600 | 1400 | 600 | 1600 | MHz | 1 |
| Platform clock frequency | 400 | 500 | 400 | 600 | 400 | 700 | MHz | 1 |
| Memory bus clock frequency | 650 | 800 | 650 | 900 | 650 | 1050 | MHz | 1, 2 |
| IFC clock frequency | - | 100 | - | 100 | - | 100 | MHz | 3 |

1. **Caution:**The coherency domain clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, coherency domain and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock speed is half the DDR4 data rate.

3. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the platform clock divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.

## 4.2 Power supply design

For additional details on the power supply design, see AN5144, QorIQ LS1088A Design Checklist.

### 4.2.1 Voltage ID (VID) controllable supply

To guarantee performance and power specifications, a specific method of selecting the optimum voltage-level must be implemented when the chip is used. As part of the chip's boot process, software must read the VID efuse values stored in the Fuse Status register (FUSESR) and then configure the external voltage regulator based on this information. This method requires a point of load voltage regulator for each chip. When VID option is used, the $V_{DD}$ supply should be separated from the SerDes 1.0 V supply $SnV_{DD}$. It is required in order to control the $V_{DD}$ supply only.

**NOTE**

During the power-on reset process, the fuse values are read and stored in the FUSESR. It is expected that the chip's boot code reads the FUSESR value very early in the boot sequence and updates the regulator accordingly.

The default voltage regulator setting that is safe for the system to boot is the recommended operating $V_{DD}$ at initial start-up of 1.025 V. It is highly recommended to select a regulator with a Vout range of at least 0.9 V to 1.1 V, with a resolution of 12.5 mV or better, when implementing a VID solution.

## 5.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

## 5.2 Temperature diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A). These devices feature series resistance cancellation using three current measurements, where up to 1.5 kΩ of resistance can be automatically cancelled from the temperature result, allowing noise filtering and a more accurate reading.

The following are the specifications of the chip's on-board temperature diode:

Operating range: TBD

Ideality factor TBD; Temperature range TBD

## 5.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 95. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 15 pounds force.