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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	8 Core, 64-Bit
Speed	1.2GHz
Co-Processors/DSP	-
RAM Controllers	DDR4
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	10GbE (2), 1GbE (8)
SATA	SATA 6Gbps (1)
USB	USB 3.0 (2) + PHY
Voltage - I/O	-
Operating Temperature	-40°C ~ 105°C
Security Features	Secure Boot, TrustZone®
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088axn7mqa

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQS0	Data Strobe	A25	IO	$G1V_{DD}$	---
D1_MDQS0_B	Data Strobe	A24	IO	$G1V_{DD}$	---
D1_MDQS1	Data Strobe	D23	IO	$G1V_{DD}$	---
D1_MDQS1_B	Data Strobe	C23	IO	$G1V_{DD}$	---
D1_MDQS2	Data Strobe	F25	IO	$G1V_{DD}$	---
D1_MDQS2_B	Data Strobe	F26	IO	$G1V_{DD}$	---
D1_MDQS3	Data Strobe	K26	IO	$G1V_{DD}$	---
D1_MDQS3_B	Data Strobe	K25	IO	$G1V_{DD}$	---
D1_MDQS4	Data Strobe	W26	IO	$G1V_{DD}$	---
D1_MDQS4_B	Data Strobe	W25	IO	$G1V_{DD}$	---
D1_MDQS5	Data Strobe	AC25	IO	$G1V_{DD}$	---
D1_MDQS5_B	Data Strobe	AC26	IO	$G1V_{DD}$	---
D1_MDQS6	Data Strobe	AE23	IO	$G1V_{DD}$	---
D1_MDQS6_B	Data Strobe	AD23	IO	$G1V_{DD}$	---
D1_MDQS7	Data Strobe	AH23	IO	$G1V_{DD}$	---
D1_MDQS7_B	Data Strobe	AG23	IO	$G1V_{DD}$	---
D1_MDQS8	Data Strobe	P25	IO	$G1V_{DD}$	---
D1_MDQS8_B	Data Strobe	P26	IO	$G1V_{DD}$	---
D1_MECC0	Error Correcting Code	M26	IO	$G1V_{DD}$	---
D1_MECC1	Error Correcting Code	N25	IO	$G1V_{DD}$	---
D1_MECC2	Error Correcting Code	T25	IO	$G1V_{DD}$	---
D1_MECC3	Error Correcting Code	T24	IO	$G1V_{DD}$	---
D1_MECC4	Error Correcting Code	M25	IO	$G1V_{DD}$	---
D1_MECC5	Error Correcting Code	N24	IO	$G1V_{DD}$	---
D1_MECC6	Error Correcting Code	R25	IO	$G1V_{DD}$	---
D1_MECC7	Error Correcting Code	R24	IO	$G1V_{DD}$	---
D1_MODT0	On Die Termination	AD28	O	$G1V_{DD}$	1
D1_MODT1	On Die Termination	AF27	O	$G1V_{DD}$	1
D1_MPAR	Address Parity Out	V28	O	$G1V_{DD}$	1
D1_MRAS_B	Row Address Strobe / MA[16]	AA28	O	$G1V_{DD}$	1
D1_MWE_B	Write Enable / MA[14]	AB28	O	$G1V_{DD}$	1
Integrated Flash Controller					
IFC_A00/GPIO1_16/ QSPI_A_CS0	IFC Address	D8	O	OV_{DD}	1, 5
IFC_A01/GPIO1_17/ QSPI_A_CS1	IFC Address	C8	O	OV_{DD}	1, 5
IFC_A02/GPIO1_18/ QSPI_A_SCK	IFC Address	C9	O	OV_{DD}	1, 5

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_CMD/GPIO3_21	Command/Response	P2	IO	EV_{DD}	6
SDHC_CMD_DIR/**SPI_PCS1**/ GPIO3_18/SDHC_DAT5	DIR	R3	O	OV_{DD}	1
SDHC_DAT0/GPIO3_22	Data	P1	IO	EV_{DD}	6
SDHC_DAT0_DIR/**SPI_PCS2**/ GPIO3_19/SDHC_DAT6	DIR	T3	O	OV_{DD}	1
SDHC_DAT1/GPIO3_23	Data	R2	IO	EV_{DD}	6
SDHC_DAT123_DIR/ **SPI_PCS3**/GPIO3_20/ SDHC_DAT7	DIR	V1	O	OV_{DD}	1
SDHC_DAT2/GPIO3_24	Data	R1	IO	EV_{DD}	6
SDHC_DAT3/GPIO3_25	Data	T1	IO	EV_{DD}	6
SDHC_DAT4/**SPI_PCS0**/ GPIO3_17/SDHC_VS	Data	U1	IO	OV_{DD}	---
SDHC_DAT5/**SPI_PCS1**/ GPIO3_18/SDHC_CMD_DIR	Data	R3	IO	OV_{DD}	---
SDHC_DAT6/**SPI_PCS2**/ GPIO3_19/SDHC_DAT0_DIR	Data	T3	IO	OV_{DD}	---
SDHC_DAT7/**SPI_PCS3**/ GPIO3_20/ SDHC_DAT123_DIR	Data	V1	IO	OV_{DD}	---
SDHC_GATE_IN/**SPI_SCK**/ GPIO3_16	IN	U2	I	OV_{DD}	1
SDHC_VS/**SPI_PCS0**/ GPIO3_17/SDHC_DAT4	VS	U1	O	OV_{DD}	1
SDHC_WP/**IIC2_SDA**/ GPIO3_13/CLK10/BRGO3	Write Protect	L3	I	DV_{DD}	1
Interrupt Controller					
EVT9_B/GPIO4_10	Interrupt Output	G7	IO	OV_{DD}	7, 9
IRQ00	External Interrupt	F11	I	OV_{DD}	1
IRQ01	External Interrupt	F15	I	OV_{DD}	1
IRQ02	External Interrupt	H7	I	OV_{DD}	1
IRQ03/GPIO3_27/ TDMB_TSYNC/ UC3_RTSB_TXEN	External Interrupt	J3	I	DV_{DD}	1
IRQ04/GPIO3_28/ TDMA_RXD/UC1_RXD7/ TDMA_TXD	External Interrupt	J4	I	DV_{DD}	1
IRQ05/GPIO3_29/ TDMA_RSYNC/ UC1_CTSB_RXDV	External Interrupt	J5	I	DV_{DD}	1
IRQ06/GPIO4_04/ TDMA_RXD_EXC/ TDMA_TXD/UC1_TXD7	External Interrupt	K5	I	DV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND46	SerDes core logic, transceiver, and PLL ground	AE20	---	---	18
SD_GND47	SerDes core logic, transceiver, and PLL ground	AF6	---	---	18
SD_GND48	SerDes core logic, transceiver, and PLL ground	AF7	---	---	18
SD_GND49	SerDes core logic, transceiver, and PLL ground	AF8	---	---	18
SD_GND50	SerDes core logic, transceiver, and PLL ground	AF9	---	---	18
SD_GND51	SerDes core logic, transceiver, and PLL ground	AF10	---	---	18
SD_GND52	SerDes core logic, transceiver, and PLL ground	AF11	---	---	18
SD_GND53	SerDes core logic, transceiver, and PLL ground	AF15	---	---	18
SD_GND54	SerDes core logic, transceiver, and PLL ground	AF16	---	---	18
SD_GND55	SerDes core logic, transceiver, and PLL ground	AF17	---	---	18
SD_GND56	SerDes core logic, transceiver, and PLL ground	AF18	---	---	18
SD_GND57	SerDes core logic, transceiver, and PLL ground	AF19	---	---	18
SD_GND58	SerDes core logic, transceiver, and PLL ground	AG5	---	---	18
SD_GND59	SerDes core logic, transceiver, and PLL ground	AG7	---	---	18
SD_GND60	SerDes core logic, transceiver, and PLL ground	AG9	---	---	18
SD_GND61	SerDes core logic, transceiver, and PLL ground	AG12	---	---	18
SD_GND62	SerDes core logic, transceiver, and PLL ground	AG14	---	---	18
SD_GND63	SerDes core logic, transceiver, and PLL ground	AG17	---	---	18
SD_GND64	SerDes core logic, transceiver, and PLL ground	AG20	---	---	18
SD_GND65	SerDes core logic, transceiver, and PLL ground	AH5	---	---	18
SD_GND66	SerDes core logic, transceiver, and PLL ground	AH7	---	---	18
SD_GND67	SerDes core logic, transceiver, and PLL ground	AH9	---	---	18

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Characteristic		Symbol	Min	Max	Unit	Notes
DUART1/2, I^2C, DMA, QE, GPIO3, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), USB control (DRVVBUS, PWRFAULT)		DV_{DD}	-0.3	3.63; 1.98	V	9
eSDHC[0-3]/CLK/CMD, GPIO3		EV_{DD}	-0.3	3.63; 1.98	V	—
DDR4 DRAM I/O voltage		$G1V_{DD}$	-0.3	1.32	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers and DIFF_SYSCLK		SV_{DD}	-0.3	1.1	V	—
Pad power supply for SerDes transmitter		XV_{DD}	-0.3	1.48	V	—
Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)		LV_{DD}	-0.3	2.75; 1.98	V	—
Ethernet management interface 2 (EMI2), GPIO2		TV_{DD}	-0.3	2.75; 1.98; 1.32	V	—
USB PHY Transceiver supply voltage		USB_HV_{DD}	-0.3	3.63	V	10
		USB_SDV_{DD}	-0.3	1.1	V	11
		USB_SV_{DD}	-0.3	1.1	V	12
Battery Backed Security Monitor supply		$TA\_BB\_V_{DD}$	-0.3	1.1	V	—
Input voltage	DDR4 DRAM signals	MV_{IN}	-0.3	$G1V_{DD}$ + 0.3	V	2
	SerDes interface and DIFF_SYSCLK	SV_{IN}	-0.3	-0.3 to (SV_{DD} + 0.3)	V	5
	Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)	LV_{IN}	-0.3	LV_{DD} + 0.3	V	4, 5
	IFC, SPI, GIC (IRQ 0/1/2), Tamper_Detect, System control and power management, SYSCLK, DDR_CLK, GPIO3, GPIO2, GPIO1, eSDHC[4-7]/VS/ DAT123_DIR/ DAT0_DIR/CMD_DIR/ SYNC), Debug, JTAG, RTC, POR signals	OV_{IN}	-0.3	OV_{DD} + 0.3	V	3, 5
	eSDHC[0-3]/CLK/ CMD, GPIO3	EV_{IN}	-0.3	EV_{DD} + 0.3	V	5, 6, 7
	DUART1/2, I^2C, DMA, QE, GPIO3, GPIO4, GIC (IRQ	DV_{IN}	-0.3	DV_{DD} + 0.3	V	5, 6, 9

Table continues on the next page...

Table 10. LS1044A VDD power dissipation for the thermal design

A53 frequency (MHz)	Platform frequency(MHz)	Main DDR data rate (MT/s)	V_{DD} (V)	Power (W)	Notes
2. Thermal power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform at 100% activity factor. 3. Thermal power are based on worst-case processed device. The above powers are measured at the junction temperature of 85C. 4. Refer to AN5144 "QorIQ LS1088A Design Checklist": Section "Maximum VDD Power and IO Power" for the power supply design and regulator sizing Section "Thermal Power" for the thermal power and thermal solution design					

3.6 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 11. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/DV_{DD}/$G1V_{DD}$/ SV_{DD}/XV_{DD}/LV_{DD}/EV_{DD}/TV_{DD} all core and platform V_{DD} supplies, TA_PROG_SFP, and all AV_{DD} supplies.)	—	25	V/ms	1, 2
Required ramp rate for PROG_SFP	---	25	V/ms	1,2
Required ramp rate for USB_HVDD	---	26.7	V/ms	1,2
Notes: 1. Ramp rate is specified as a linear ramp from 10% to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 mV to 500 mV is the most critical as this range might falsely trigger the ESD circuitry. 2. Over full recommended operating temperature range. See Table 3.				

3.7 Input clocks

3.7.1 System clock (SYSCLK)

This section describes the system clock DC electrical characteristics and AC timing specifications.

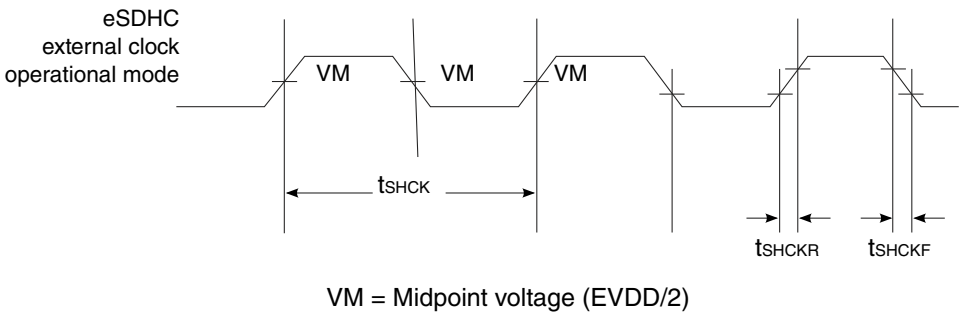


Figure 17. eSDHC SDR50 mode clock input timing diagram

This figure provides the eSDHC input AC timing diagram for SDR50 mode.

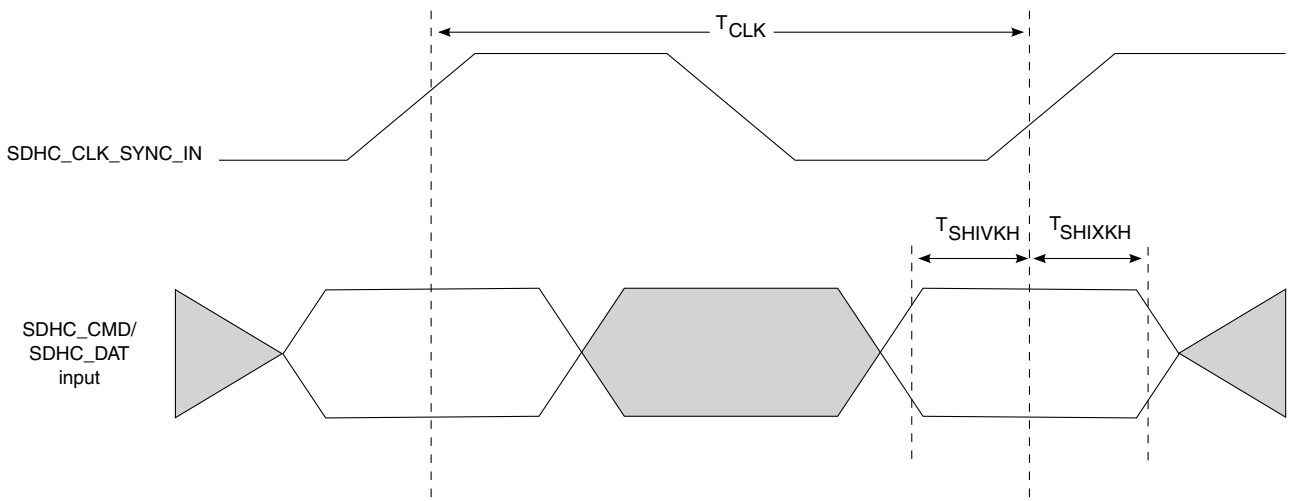


Figure 18. eSDHC SDR50 mode input AC timing diagram

This figure provides the eSDHC output timing diagram for SDR50 mode.

This figure provides the eSDHC SDR104/HS200 mode timing diagram.

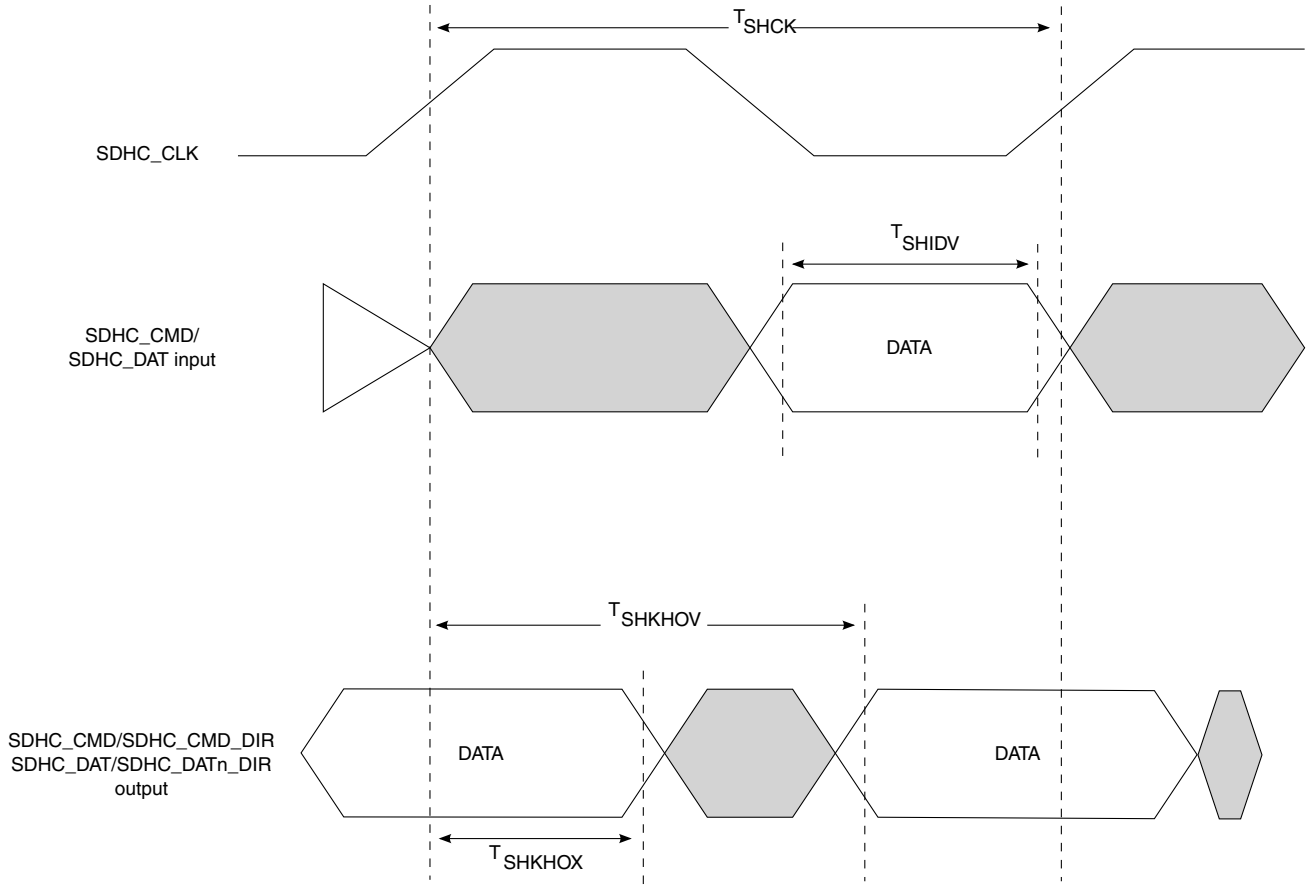


Figure 22. eSDHC SDR104/HS200 mode timing diagram

3.13 Ethernet interface (EMI, RGMII, and IEEE Std 1588™)

This section describes the DC and AC electrical characteristics for the Ethernet controller, Ethernet management, RGMII, and IEEE Std 1588 interfaces.

3.13.1 Ethernet management interface (EMI)

This section describes the electrical characteristics for the Ethernet management interface (EMI).

The EMI1 and EMI2 interface timings are compatible with IEEE Std 802.3™ clauses 22 and 45, respectively.

Table 40. EMI1 DC electrical characteristics (LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.					
4. The symbol LV_{DD} represents the input voltage of the supply referenced in Table 3.					

3.13.1.1.2 EMI1 AC timing specifications

This table provides the AC timing specifications for the EMI1 interface.

Table 41. EMI1 AC timing specifications[4]

Parameter	Symbol	Min	Max	Unit	Notes
MDC frequency	f_{MDC}	-	2.5	MHz	1
MDC clock pulse width high	t_{MDCH}	160.0	-	ns	-
MDC to MDIO delay	t_{MDKHDX}	(5 x t_{enet_clk}) - 3	(5 x t_{enet_clk}) + 3	ns	2, 3
MDIO to MDC setup time	t_{MDDVKH}	8.0	-	ns	-
MDIO to MDC hold time	t_{MDDXKH}	2	-	ns	-
1. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.					
2. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods ± 3 ns. For example, with an Ethernet clock of 400 MHz, the min/max delay is 12.5 ns ± 3 ns.					
3. t_{enet_clk} is the Ethernet clock period (Frame Manager clock period x 2).					
4. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.					

This figure shows the Ethernet management interface 1 timing diagram.

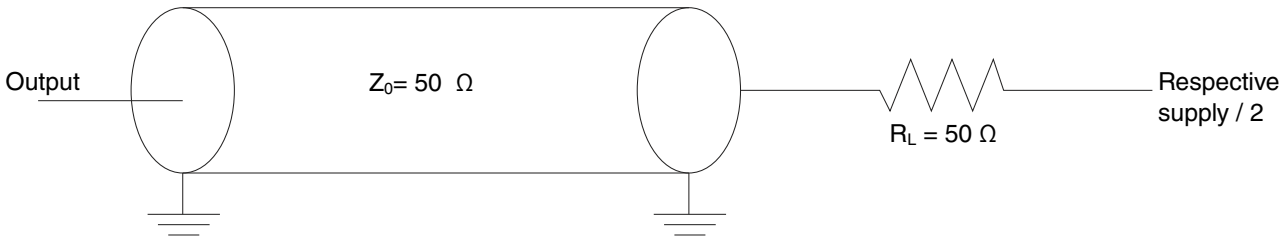


Figure 28. GPIO AC test load

3.15 Generic interrupt controller (GIC) interface

This section describes the DC and AC electrical characteristics for the GIC interface.

3.15.1 GIC DC electrical characteristics

This table provides the DC electrical characteristics for the GIC interface operating at DV_{DD} = 3.3 V.

Table 59. GIC DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= DV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (DV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (DV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
3. The symbol DV_{IN} represents the input voltage of the supply referenced in Table 3.

This table provides the DC electrical characteristics for the GIC interface operating at DV_{DD} = 1.8 V.

Table 60. GIC DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x DV_{DD}	V	2

Table continues on the next page...

Table 73. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Notes: 1. Specified at the measurement point into a timing and voltage test load as shown in Figure 38 and measured over any 250 consecutive transmitter UIs. 2. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. 3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required. 4. For recommended operating conditions, see Table 3.						

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 74. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. See Note 1.
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	ps	-
Transmitter RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	3.0	-	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.
Notes: 1. Specified at the measurement point into a timing and voltage test load as shown in Figure 38 and measured over any 250 consecutive transmitter UIs. 2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required. 3. For recommended operating conditions, see Table 3.						

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 82. Gen1i/1m 1.5 G receiver input DC specifications (SV_{DD} = 0.9 V / 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 3.

This table provides the Gen2i/2m or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 83. Gen2i/2m 3 G receiver input DC specifications (SV_{DD} = 0.9 V / 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 3.

This table provides the Gen 3i differential receiver input DC characteristics for the SATA interface.

Table 84. Gen 3i receiver input DC specifications (SV_{DD} = 0.9 V / 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	1000	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	—	75	120	200	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 3.

3.16.5.2 SATA AC timing specifications

This section describes the SATA AC timing specifications.

Table 101. QSGMII receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000-100ppm	5.0	5.000+100ppm	Gb/s	-
Uncorrelated bounded high probability jitter	R_{DJ}	-	-	0.15	UI p-p	-
Correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.3	UI p-p	The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example, by a PCB trace.
Bounded high probability jitter	R_{BHPJ}	-	-	0.45	UI p-p	-
Sinusoidal jitter, maximum	R_{SJ-max}	-	-	5.0	UI p-p	-
Sinusoidal jitter, high frequency	R_{SJ-hf}	-	-	0.05	UI p-p	-
Total jitter (does not include sinusoidal jitter)	R_{TJ}	-	-	0.6	UI p-p	-

The sinusoidal jitter may have any amplitude and frequency in the unshaded region of this figure.

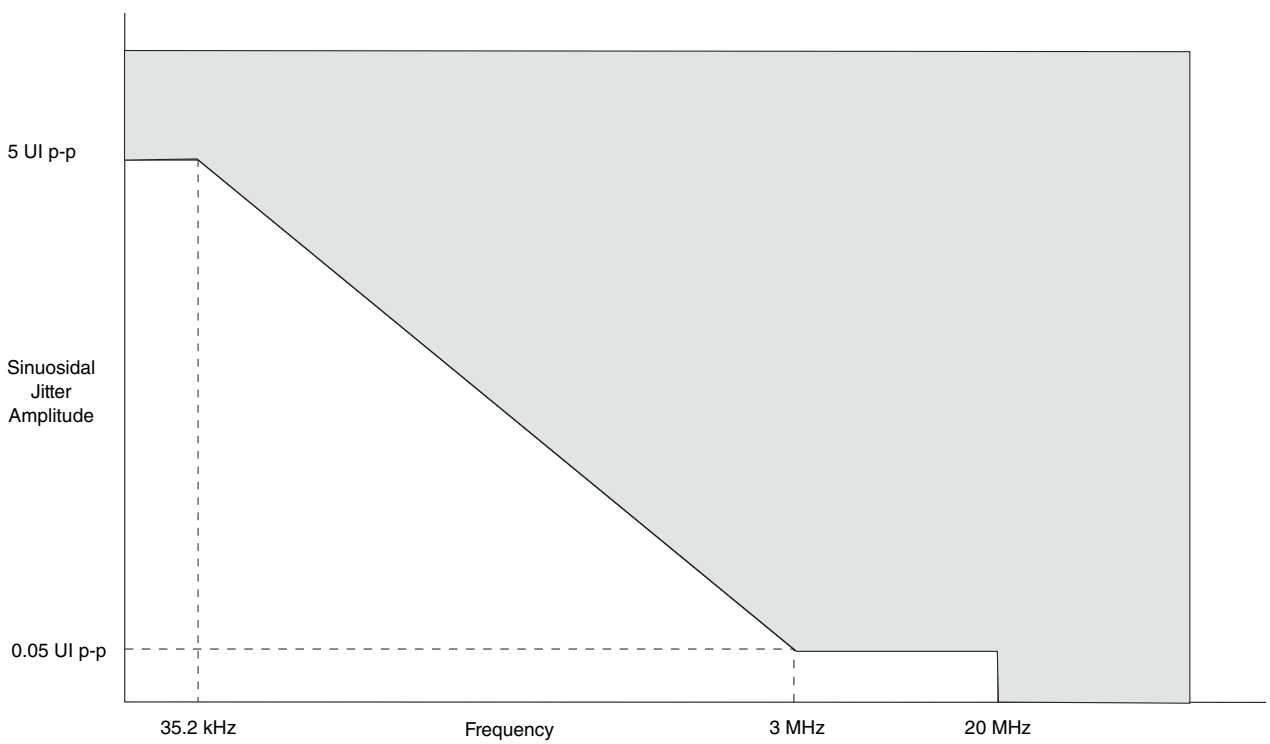


Figure 43. QSGMII single-frequency sinusoidal jitter limits

Table 106. 1000Base-KX transmitter DC electrical characteristics[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω	-
1. For recommended operating conditions, see Table 3. 2. SRDSxLNmTECR0[AMP_RED]=00_0000						

This table provides the 1000Base-KX receiver DC electrical characteristics.

Table 107. 1000Base-KX receiver DC electrical characteristics[1]

Parameter	Symbol	Min	Max	Unit
Input differential voltage	$V_{RX-DIFFp-p}$	-	1600.0	mV
Differential resistance	T_{RDIN}	80.0	120.0	Ω
1. For recommended operating conditions, see Table 3.				

3.16.9.2 1000Base-KX AC timing specifications

NOTE

The AC specifications do not include RefClk jitter.

This table provides the 1000Base-KX transmitter AC timing specifications.

Table 108. 1000Base-KX transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Baud rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Uncorrelated high probability jitter/Random Jitter	T_{UHPJ} / T_{RJ}	-	-	0.15	UI p-p	-
Deterministic jitter tolerance	T_{DJ}	-	-	0.1	UI p-p	-
Total jitter tolerance	T_{TJ}	-	-	0.25	UI p-p	Total jitter is specified at a BER of 10^{-12}.

This table provides the 1000Base-KX receiver AC timing specifications, which are based on the parameters defined in IEEE Std 802.3ap-2007.

Table 109. 1000Base-KX receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Baud rate	R_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-

Table continues on the next page...

Table 113. 10GBase-KR receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Total jitter tolerance	R_{TJ}	-	-	Per IEEE Std 802.3ap-2007, Annex 69a.	UI p-p
Random jitter	R_{RJ}	-	-	0.13	UI p-p
Sinusoidal jitter (maximum)	R_{SJ-max}	-	-	0.115	UI p-p
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p

3.17 I²C interface

This section describes the DC and AC electrical characteristics for the I²C interface.

3.17.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interface when operating at DV_{DD} = 3.3 V.

Table 114. I²C DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	2
Output low voltage (DV_{DD} = min, IOL = 3 mA, DV_{DD} > 2V)	V_{OL}	-	0.4	V	3
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	4
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} (min) and 0.9 x DV_{DD} (max))	I_I	-50.0	50.0	µA	5
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.

3. The output voltage (open drain or open collector) condition = 3 mA sink current.

4. See the chip reference manual for information about the digital filter used.

5. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.

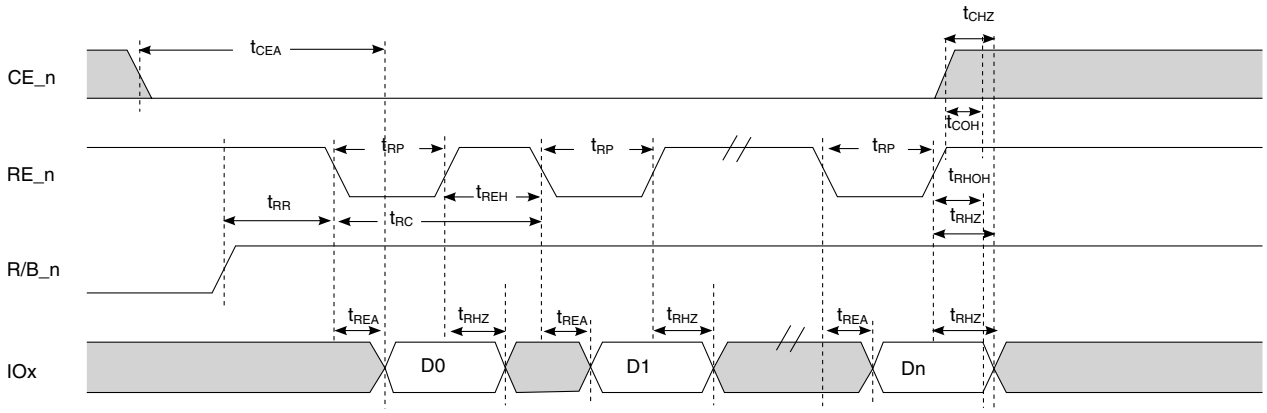


Figure 57. Data input cycle timings

This figure shows the t_{CLR} timings.

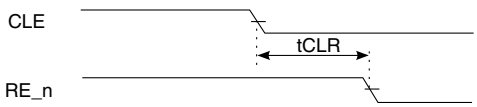


Figure 58. t_{CLR} timings

This figure shows the t_{WB}, t_{FEAT}, t_{ITC}, and t_{RR} timings.

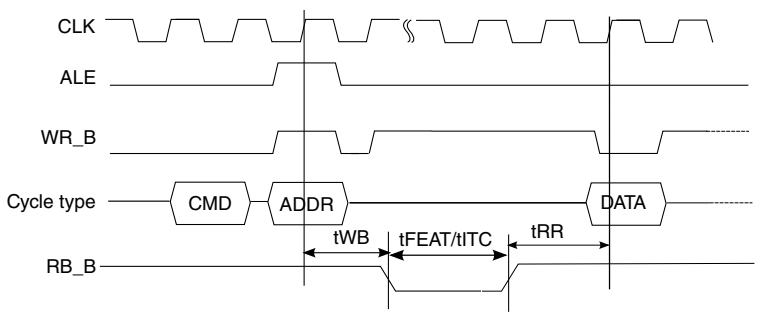


Figure 59. t_{WB}, t_{FEAT}, t_{ITC}, and t_{RR} timings

This figure shows the read status timings.

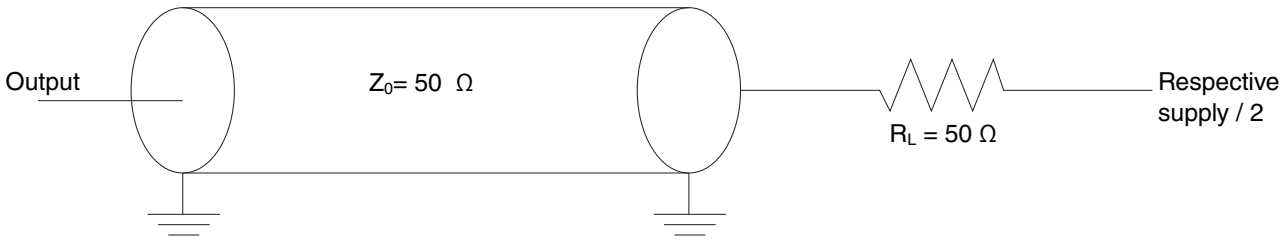
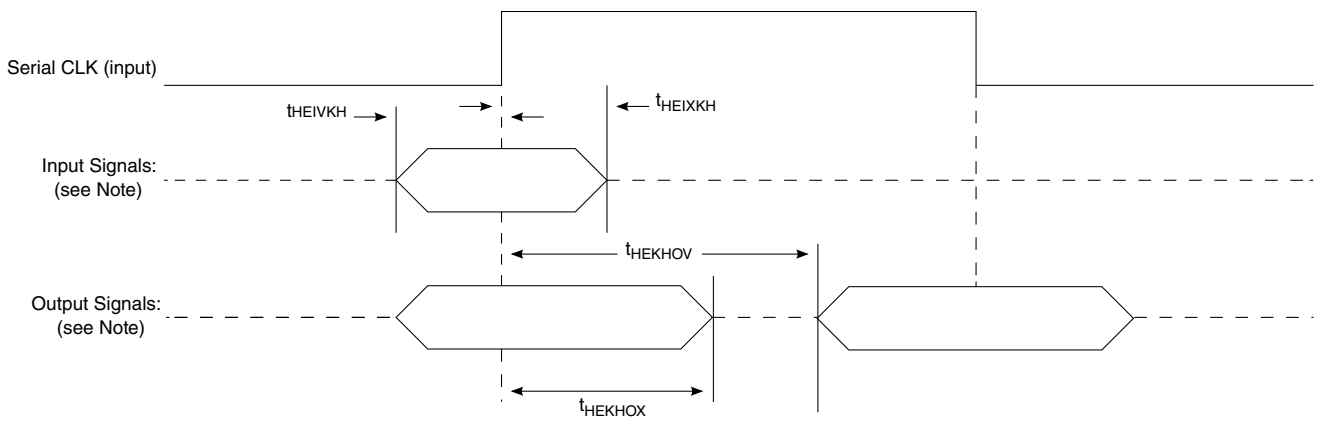


Figure 87. AC test load for HDLC

These figures represent the AC timing from the tables in section HDLC and synchronous UART AC timing specifications. Note that, although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the timing with an external clock.



Note: The clock edge is selectable.

Figure 88. AC timing (external clock) diagram

This figure shows the timing with an internal clock.

Table 143. USB 3.0 receiver DC electrical characteristics[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
LFPS detect threshold	$V_{TRX-IDLE-DET-DC-DIFFpp}$	100.0	-	300.0	mV	2
1. For recommended operating conditions, see Table 3.						
2. Below the minimum is noise. Must wake up above the maximum.						

3.23.1.2 USB 3.0 AC timing specifications

This table provides the USB 3.0 transmitter AC timing specifications at package pins.

Table 144. USB 3.0 transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Speed	-	-	5.0	-	Gb/s	-
Transmitter eye	T_{TX-EYE}	0.625	-	-	UI	-
Unit Interval	UI	199.94	-	200.06	ps	UI does not account for SSC-caused variations.
AC coupling capacitor	AC_{CAP}	75.0	-	200.0	nF	-

This table provides the USB 3.0 receiver AC timing specifications at receiver package pins.

Table 145. USB 3.0 receiver AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Unit Interval	UI	199.94	200.06	ps	UI does not account for SSC-caused variations.

3.23.1.3 USB 3.0 LFPS specifications

This table provides the key LFPS electrical specifications at the transmitter.

Table 146. LFPS electrical specifications at the transmitter

Parameter	Symbol	Min	Max	Unit	Notes
Period	t_{Period}	20.0	100.0	ns	-

Table continues on the next page...

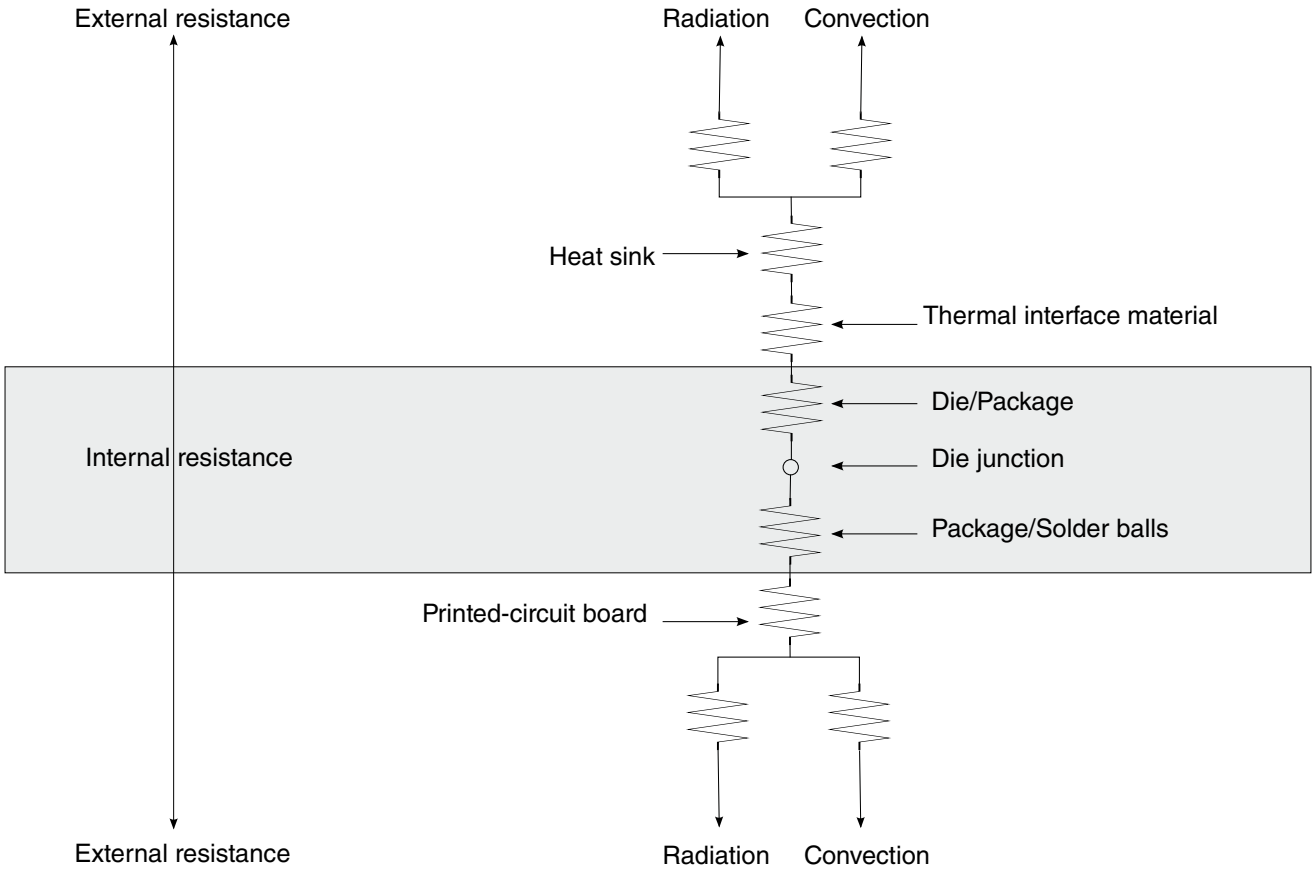
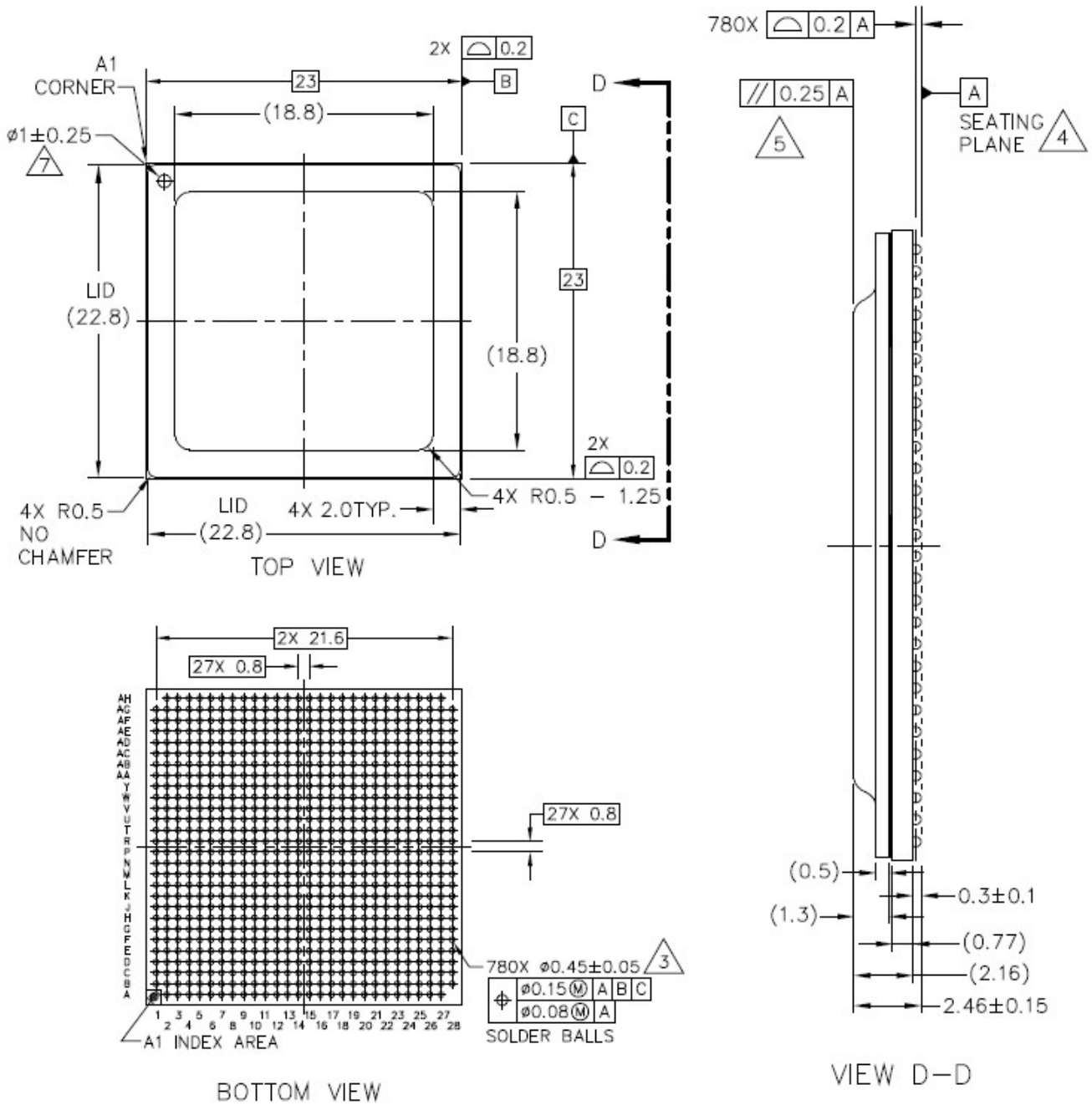


Figure 96. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

5.3.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 95).



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: FCPBGA, WITH LID, 23 X 23 X 2.46 PKG, 0.8 MM PITCH, 780 I/O	DOCUMENT NO: 98ASA00854D	REV: O
	STANDARD: NON–JEDEC	
	03 DEC 2014	

Figure 97. Mechanical dimensions of the FC-PBGA

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.
7. Pin 1 thru hole shall be centered within foot area.
8. 23.2 mm maximum package assembly (lid + laminate) X and Y.

7 Security fuse processor

This chip implements trust architecture 3.0, which supports capabilities such as secure boot. Use of the trust architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8 V to the TA_PROG_SFP pin per Power sequencing. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times, TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Power sequencing. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

NOTE

Users not implementing the QorIQ platform's trust architecture features should connect TA_PROG_SFP to GND.

8 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

8.1 Part numbering nomenclature

This table provides the NXP Layerscape platform part numbering nomenclature.