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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	8 Core, 64-Bit
Speed	1.4GHz
Co-Processors/DSP	-
RAM Controllers	DDR4
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	10GbE (2), 1GbE (8)
SATA	SATA 6Gbps (1)
USB	USB 3.0 (2) + PHY
Voltage - I/O	-
Operating Temperature	-40°C ~ 105°C
Security Features	Secure Boot, TrustZone®
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088axn7pta

1 Overview

A member of the Layerscape (LS1) series, the LS1088A is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) device featuring eight extremely power-efficient 64-bit ARM® Cortex®-A53 cores with ECC-protected L1 and L2 cache memories for high reliability, running up to 1.6 GHz.

The LS1088A family of devices can be used for enterprise and service provider routers, Virtual CPE, industrial communications, security appliance and military and aerospace applications.

This figure shows the LS1088A block diagram.

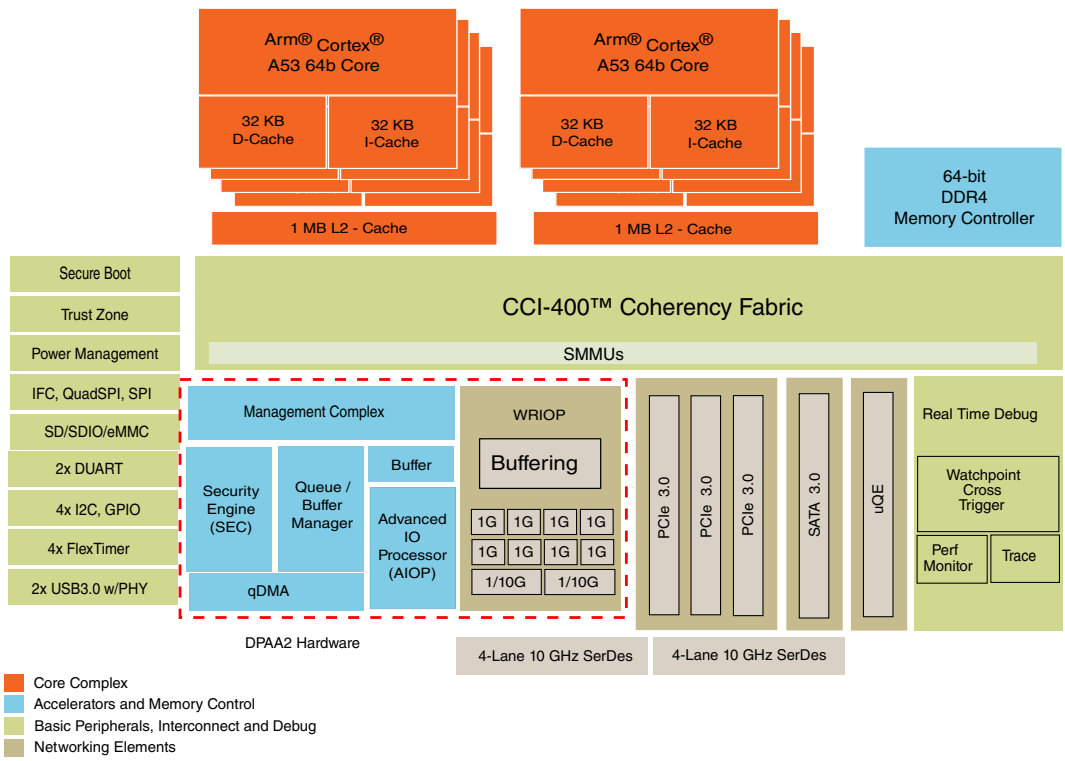

Figure 1. LS1088A block diagram

2 Pin assignments

NOTE: Information given in this section is preliminary and is subject to change.

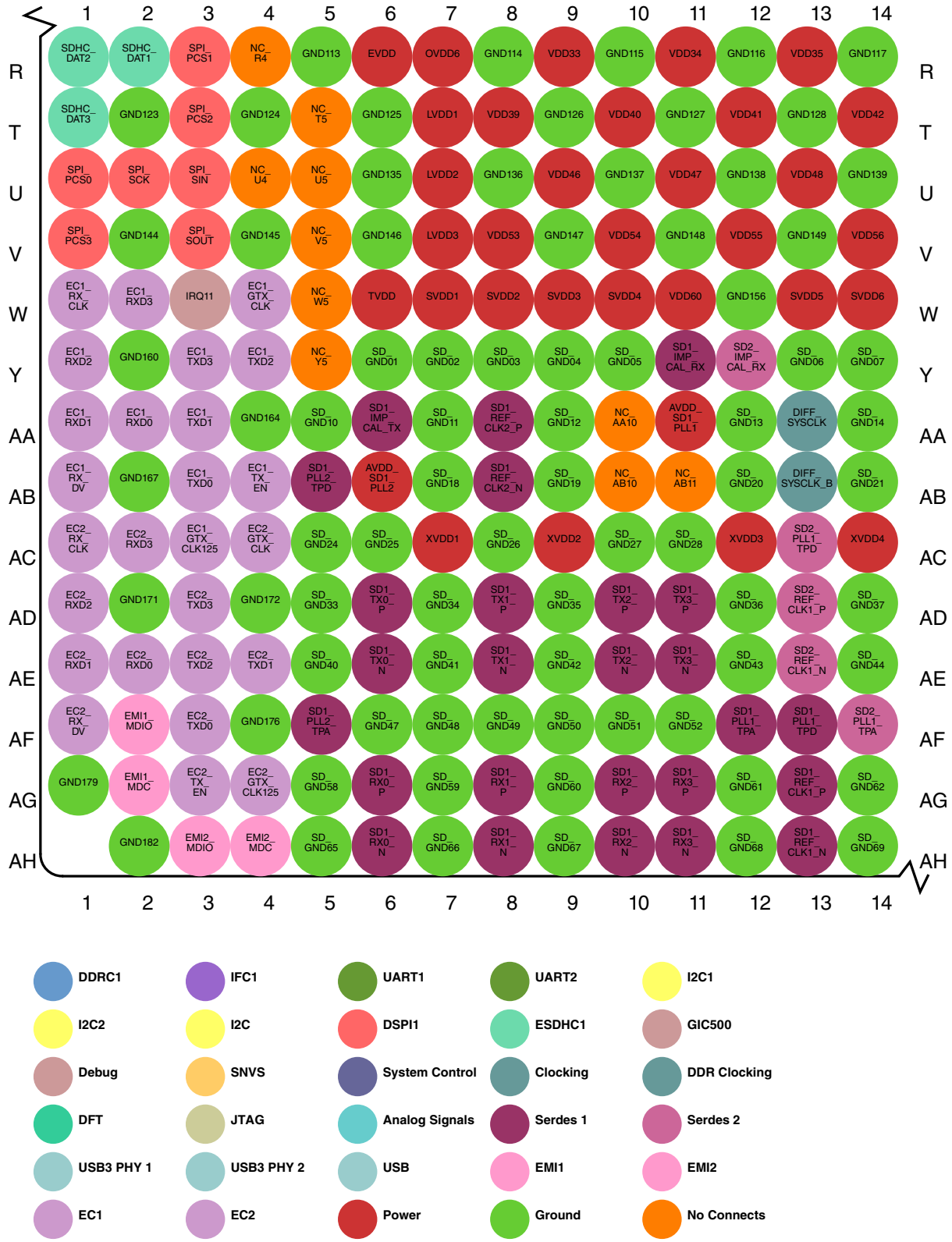

Figure 5. Detail C

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ26	Data	L24	IO	$G1V_{DD}$	---
D1_MDQ27	Data	M24	IO	$G1V_{DD}$	---
D1_MDQ28	Data	J22	IO	$G1V_{DD}$	---
D1_MDQ29	Data	H23	IO	$G1V_{DD}$	---
D1_MDQ30	Data	K24	IO	$G1V_{DD}$	---
D1_MDQ31	Data	L25	IO	$G1V_{DD}$	---
D1_MDQ32	Data	V24	IO	$G1V_{DD}$	---
D1_MDQ33	Data	U26	IO	$G1V_{DD}$	---
D1_MDQ34	Data	AA26	IO	$G1V_{DD}$	---
D1_MDQ35	Data	W23	IO	$G1V_{DD}$	---
D1_MDQ36	Data	U24	IO	$G1V_{DD}$	---
D1_MDQ37	Data	U25	IO	$G1V_{DD}$	---
D1_MDQ38	Data	W24	IO	$G1V_{DD}$	---
D1_MDQ39	Data	Y25	IO	$G1V_{DD}$	---
D1_MDQ40	Data	AB24	IO	$G1V_{DD}$	---
D1_MDQ41	Data	AB25	IO	$G1V_{DD}$	---
D1_MDQ42	Data	AE25	IO	$G1V_{DD}$	---
D1_MDQ43	Data	AF25	IO	$G1V_{DD}$	---
D1_MDQ44	Data	Y24	IO	$G1V_{DD}$	---
D1_MDQ45	Data	AA25	IO	$G1V_{DD}$	---
D1_MDQ46	Data	AD25	IO	$G1V_{DD}$	---
D1_MDQ47	Data	AE26	IO	$G1V_{DD}$	---
D1_MDQ48	Data	AA22	IO	$G1V_{DD}$	---
D1_MDQ49	Data	AB23	IO	$G1V_{DD}$	---
D1_MDQ50	Data	AC22	IO	$G1V_{DD}$	---
D1_MDQ51	Data	AB22	IO	$G1V_{DD}$	---
D1_MDQ52	Data	Y22	IO	$G1V_{DD}$	---
D1_MDQ53	Data	AA23	IO	$G1V_{DD}$	---
D1_MDQ54	Data	AD22	IO	$G1V_{DD}$	---
D1_MDQ55	Data	AE22	IO	$G1V_{DD}$	---
D1_MDQ56	Data	AH25	IO	$G1V_{DD}$	---
D1_MDQ57	Data	AF24	IO	$G1V_{DD}$	---
D1_MDQ58	Data	AG22	IO	$G1V_{DD}$	---
D1_MDQ59	Data	AF22	IO	$G1V_{DD}$	---
D1_MDQ60	Data	AH26	IO	$G1V_{DD}$	---
D1_MDQ61	Data	AG25	IO	$G1V_{DD}$	---
D1_MDQ62	Data	AF23	IO	$G1V_{DD}$	---
D1_MDQ63	Data	AH22	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND009	Core, Platform and PLL Ground	B16	---	---	---
GND010	Core, Platform and PLL Ground	B19	---	---	---
GND011	Core, Platform and PLL Ground	B21	---	---	---
GND012	Core, Platform and PLL Ground	B24	---	---	---
GND013	Core, Platform and PLL Ground	B26	---	---	---
GND014	Core, Platform and PLL Ground	C1	---	---	---
GND015	Core, Platform and PLL Ground	C2	---	---	---
GND016	Core, Platform and PLL Ground	C5	---	---	---
GND017	Core, Platform and PLL Ground	C21	---	---	---
GND018	Core, Platform and PLL Ground	C27	---	---	---
GND019	Core, Platform and PLL Ground	D3	---	---	---
GND020	Core, Platform and PLL Ground	D4	---	---	---
GND021	Core, Platform and PLL Ground	D7	---	---	---
GND022	Core, Platform and PLL Ground	D9	---	---	---
GND023	Core, Platform and PLL Ground	D12	---	---	---
GND024	Core, Platform and PLL Ground	D15	---	---	---
GND025	Core, Platform and PLL Ground	D18	---	---	---
GND026	Core, Platform and PLL Ground	D21	---	---	---
GND027	Core, Platform and PLL Ground	D24	---	---	---
GND028	Core, Platform and PLL Ground	E1	---	---	---
GND029	Core, Platform and PLL Ground	E2	---	---	---
GND030	Core, Platform and PLL Ground	E5	---	---	---

Table continues on the next page...

NOTE

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Characteristic	Symbol	Recommended value	Unit	Notes
VID core and platform supply voltage at initial start up	V_{DD}	1.025 V ± 30 mV	V	3, 4, 5, 9
VID core and platform supply voltage during normal operation		VID ± 30 mV	V	3, 4, 5, 9
0.9V core and platform supply voltage		0.9 V ± 30 mV	V	4, 5, 9
0.9V core and platform supply voltage at initial start up		1.025 V ± 30 mV or 0.9 V ± 30 mV	V	4, 5, 9
Battery backed security monitor supply (TA_BB_TMP_DETECT_B)	TA_BB_V_{DD}	1.0 V + 50 mV / - 30 mV	V	9
		0.9 V + 50 mV / - 30 mV	V	9
PLL supply voltage (core PLL, platform, DDR)	AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_PLAT, AV_{DD}_D1	1.8 V ± 90 mV	V	—
PLL supply voltage (SerDes, filtered from XV_{DD})	AV_{DD}_SD*n*_PLL1 AV_{DD}_SD*n*_PLL2	1.35 V ± 67 mV	V	—
SFP fuse programming	TA_PROG_SFP	1.8 V ± 90 mV	V	2
Thermal monitor unit supply	TH_V_{DD}	1.8 V ± 90 mV	V	—
IFC, SPI, GIC (IRQ 0/1/2), Tamper_Detect, System control and power management, SYSCLK, DDR_CLK, GPIO3, GPIO2, GPIO1, eSDHC[4-7]/VS/DAT123_DIR/ DAT0_DIR/CMD_DIR/SYNC), Debug, JTAG, RTC, POR signals	OV_{DD}	1.8 V ± 90 mV	V	—
DUART1/2, I^2C, DMA, QE, GPIO3, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), USB control (DRVVBUS, PWRFAULT)	DV_{DD}	3.3 V ± 165 mV 1.8 V ± 90 mV	V	6
eSDHC[0-3]/CLK/CMD, GPIO3	EV_{DD}	3.3 V ±165 mV 1.8 V ± 90 mV	V	—
DDR4 DRAM I/O voltage	$G1V_{DD}$	1.2V ± 60 mV	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers and DIFF_SYSCLK	SV_{DD}	1.0 V + 50 mV / - 30 mV	V	9
		0.9V +50 mV / -30 mV	V	9
Pad power supply for SerDes transmitters	XV_{DD}	1.35 V ± 67 mV	V	—
Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)	LV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
Ethernet management interface 2 (EMI2), GPIO2	TV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV 1.2V ± 60 mV	V	—
USB PHY 3.3 V high supply voltage	USB_HV_{DD}	3.3 V ± 165 mV	V	6

Table continues on the next page...

Table 28. DDR4 SDRAM interface input AC timing specifications (GV_{DD} = 1.2 V ± 5% for DDR4)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1600 MT/s data rate		-200	200		
1333 MT/s data rate		-250	250		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.

3. For recommended operating conditions, see Table 3.

This figure shows the DDR4 SDRAM interface input timing diagram.

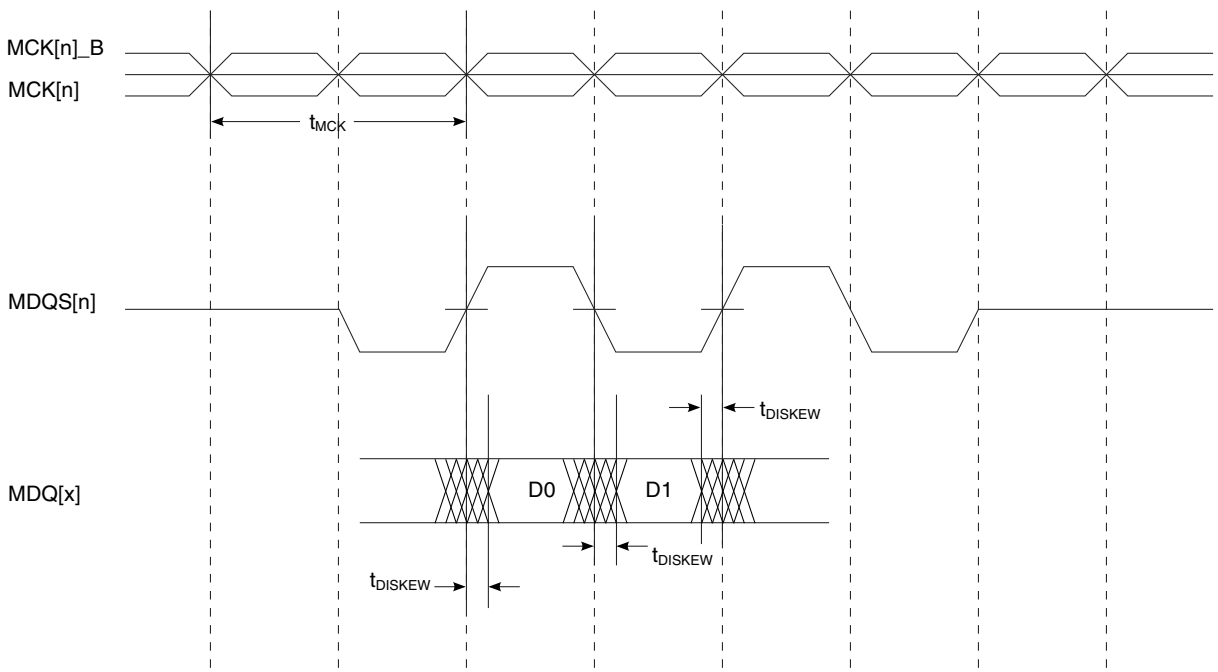

Figure 11. DDR4 SDRAM interface input timing diagram

3.10.2.2 DDR4 SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR4 SDRAM interface.

Table 29. DDR4 SDRAM interface output AC timing specifications (GV_{DD} = 1.2 V)[7]

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	938	1500	ps	2

Table continues on the next page...

Table 34. eSDHC interface DC electrical characteristics (E/D/OV_{DD}=1.8 V)[3] (continued)

Characteristic	Symbol	Min	Max	Unit	Notes
Input/output leakage current	(I_{IN}/I_{OZ})	-10	10	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max E/D/OV_{IN} values found in the Table 3.
2. Open-drain mode is for MMC cards only.
3. At recommended operating conditions with E/D/OV_{DD} = 1.8 V.

3.12.2 eSDHC AC timing specifications

This section provides the AC timing specifications.

This table provides the eSDHC AC timing specifications as defined in Figure 14, Figure 15, and Figure 16.

Table 35. eSDHC AC timing specifications (full-speed/high-speed mode)[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency: • SD/SDIO (full-speed/high-speed mode) • MMC (full-speed/high-speed mode)	f_{SHSCK}	0	25/50 20/52	MHz	2, 4
SDHC_CLK clock low time (full-speed/high-speed mode)	t_{SHSCKL}	10/7	-	ns	4
SDHC_CLK clock high time (full-speed/high-speed mode)	t_{SHSCKH}	10/7	-	ns	4
SDHC_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK	$t_{SHSIVKH}$	2.5	-	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK	$t_{SHSIXKH}$	2.5	-	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOX}$	-3	-	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOV}$	-	3	ns	4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC high-speed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0-25MHz for an SD/SDIO card and 0-20MHz for an MMC card. In high-speed mode, the clock frequency value can be 0-50MHz for an SD/SDIO card and 0-52MHz for an MMC card.

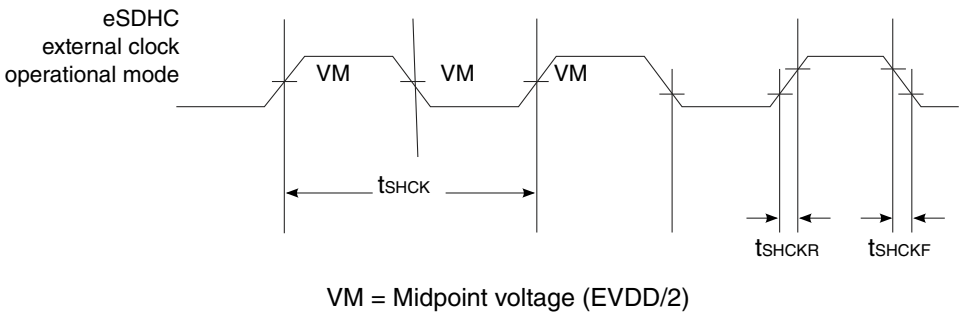

Figure 17. eSDHC SDR50 mode clock input timing diagram

This figure provides the eSDHC input AC timing diagram for SDR50 mode.

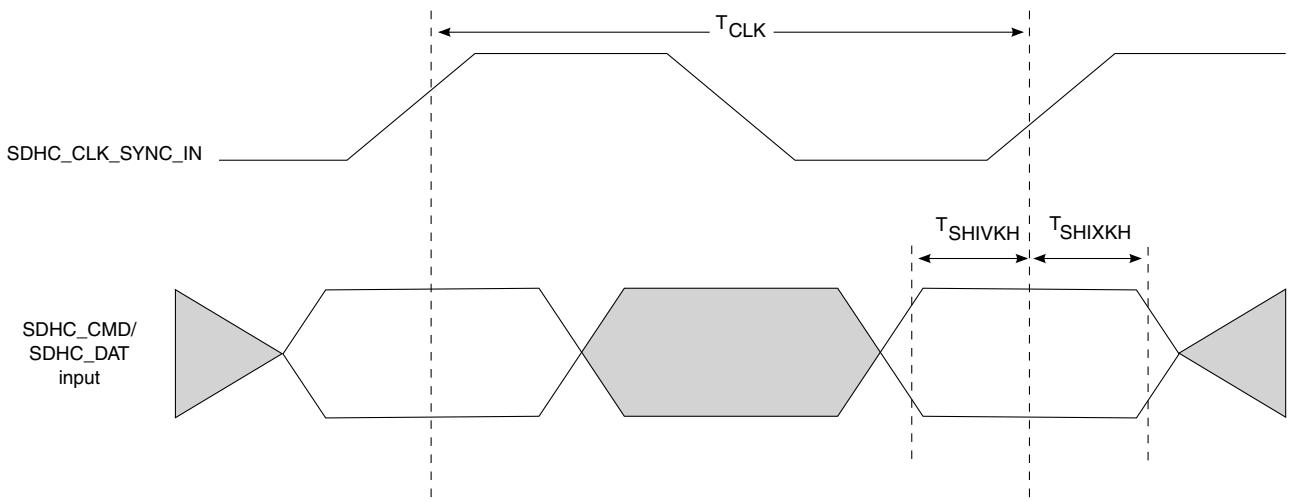

Figure 18. eSDHC SDR50 mode input AC timing diagram

This figure provides the eSDHC output timing diagram for SDR50 mode.

Table 37. eSDHC AC timing specifications (DDR50/DDR)[3] (continued)

Parameter	Symbol	Min	Max	Units	Notes
Notes:					
1. C_{CARD} ≤ 10 pF, (1 card).					
2. $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ ≤ 20 pF for MMC, ≤ 25pF for Input Data of DDR50, ≤ 30pF for Input CMD of DDR50.					
3. For recommended operating conditions, see Table 3.					
4. Total clock duty cycle and data and clock skew on the board should be limited to 0.2ns.					
5. Total clock duty cycle and command and clock skew on the board should be limited to 0.3ns.					

This figure provides the eSDHC DDR50/DDR mode input AC timing diagram.

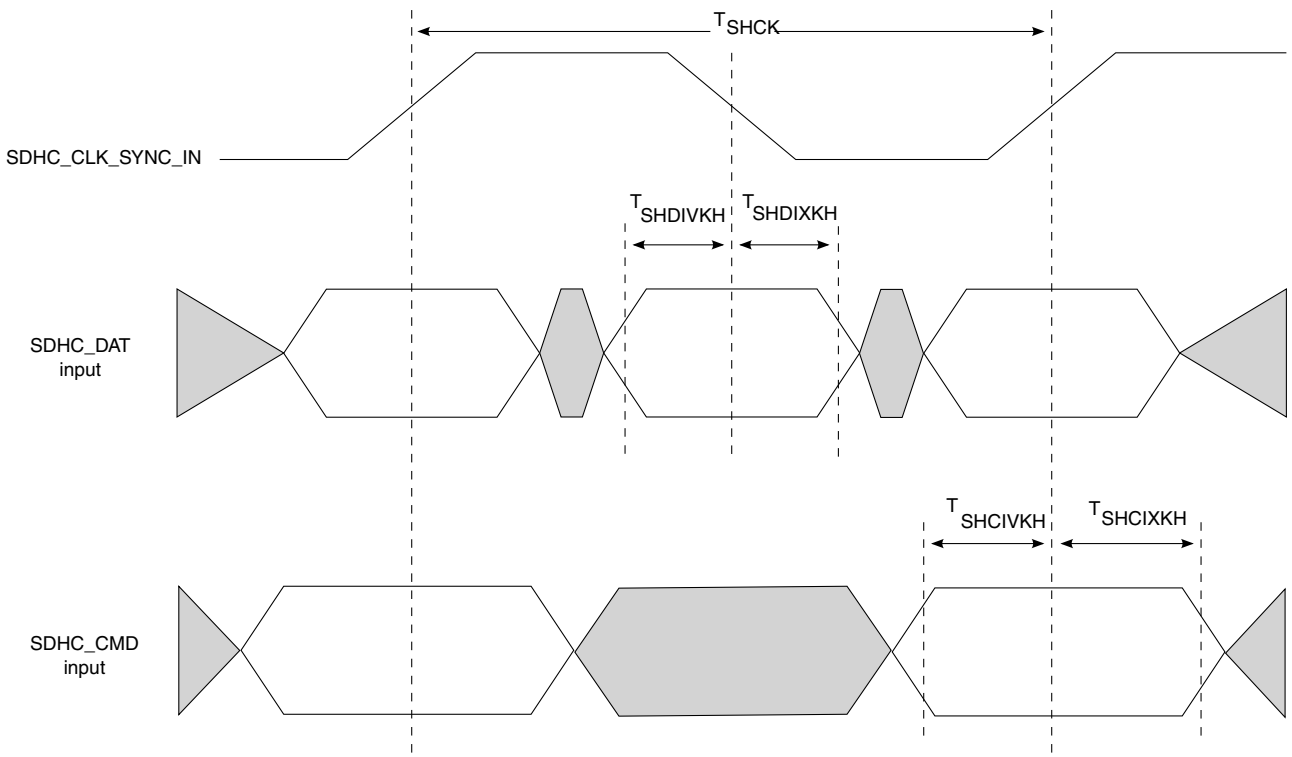

Figure 20. eSDHC DDR50/DDR mode input AC timing diagram

This figure provides the eSDHC DDR50/DDR mode output AC timing diagram.

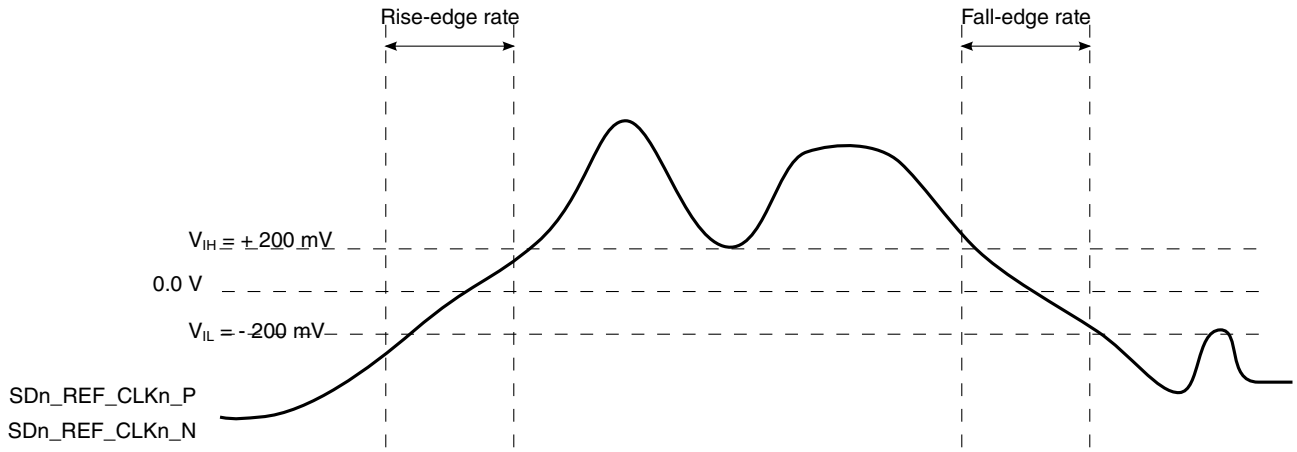

Figure 34. Differential measurement points for rise and fall time

This figure shows the single-ended measurement points for rise and fall time matching.

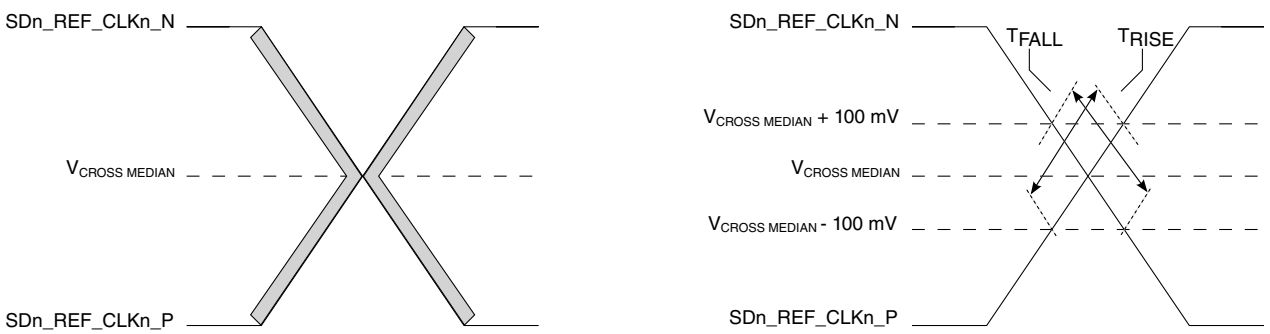

Figure 35. Single-ended measurement points for rise and fall time matching

3.16.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

Figure 36. SerDes transmitter and receiver reference circuits

The DC and AC specifications of the SerDes data lanes are defined in each interface protocol section below based on the application usage:

3.16.6 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 39, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100 Ω output impedance. Each input of the SerDes receiver differential pair features 50 Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 36.

3.16.6.1 SGMII clocking requirements for SDn_REF_CLK1_P and SDn_REF_CLK1_N

When operating in SGMII mode, the EC*n*_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N pins. SerDes lanes may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.16.6.2 SGMII DC electrical characteristics

This section describes the electrical characteristics for the SGMII interface.

3.16.6.2.1 SGMII and SGMII 2.5 G transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N)as shown in Figure 40.

Table 92. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD} \rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD} \rvert_{-min}/2$	-	-	mV	1
Output differential voltage[2, 3, 5] (XV_{DD-Typ} at 1.35 V)	$\lvert V_{OD} \rvert$	320	500.0	725.0	mV	TECR0[AMP_RED]=0b000000
		293.8	459.0	665.6		TECR0[AMP_RED]=0b000001
		266.9	417.0	604.7		TECR0[AMP_RED]=0b000011
		240.6	376.0	545.2		TECR0[AMP_RED]=0b000010

Table continues on the next page...

Table 96. SGMII transmit AC timing specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Notes:						
1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.						
2. See Figure 42 for single frequency sinusoidal jitter measurements.						
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.						
4. For recommended operating conditions, see Table 3.						

3.16.6.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) or at the receiver inputs (SD*n*_RX*n*_P and SD*n*_RX*n*_N) respectively, as shown in this figure.

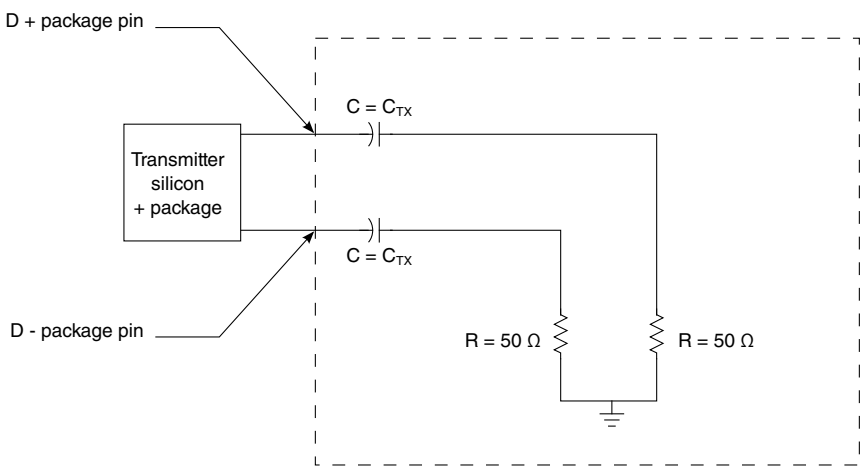

Figure 41. SGMII AC test/measurement load

3.16.6.3.3 SGMII and SGMII 2.5 G receiver AC timing specifications

This table provides the SGMII and SGMII 2.5 G receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 97. SGMII receiver AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2

Table continues on the next page...

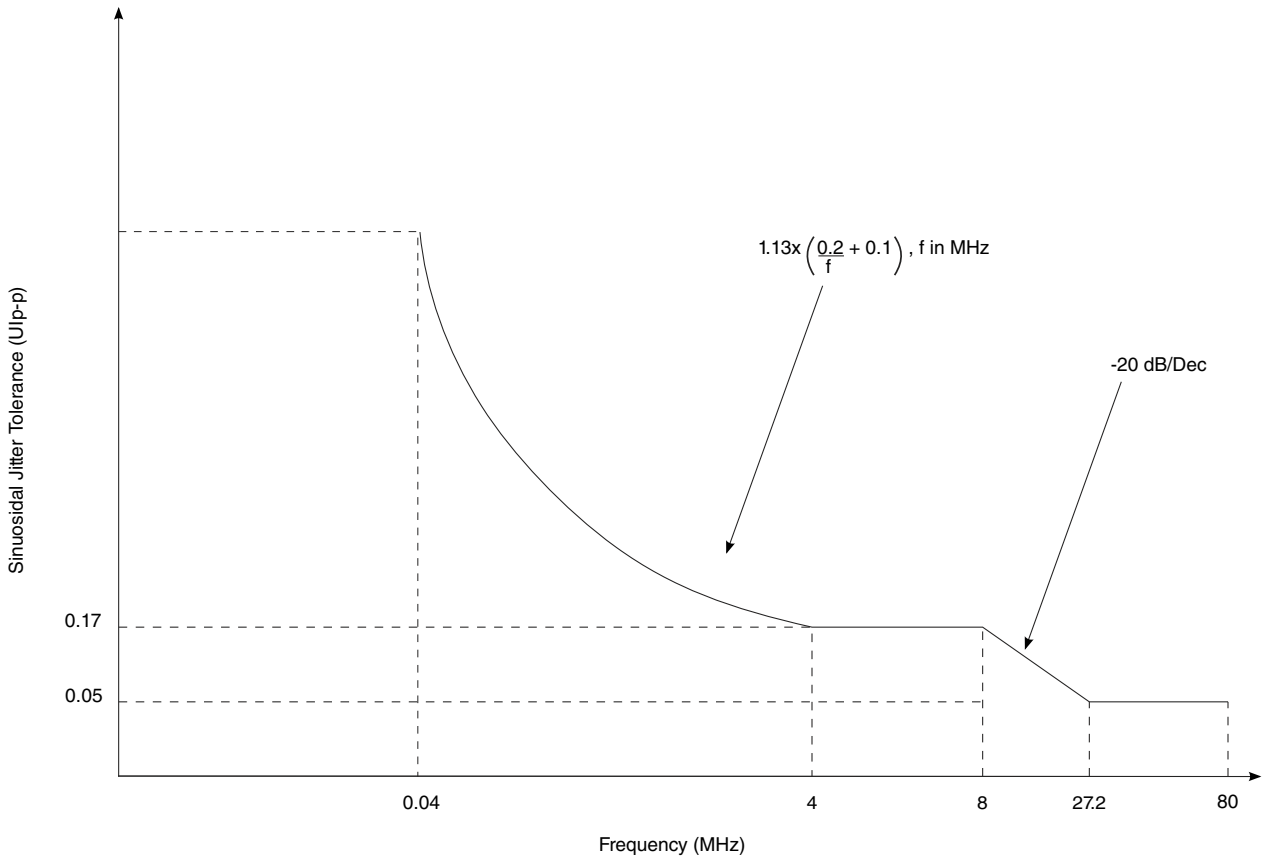

Figure 44. XFI host receiver input sinusoidal jitter tolerance

3.16.9 1000Base-KX interface

This section describes the electrical characteristics for the 1000Base-KX interface. Only AC-coupled operation is supported.

3.16.9.1 1000Base-KX DC electrical characteristics

This table describes the 1000Base-KX SerDes transmitter DC electrical characteristics at TP1 per IEEE Std 802.3ap-2007. Transmitter DC electrical characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N).

Table 106. 1000Base-KX transmitter DC electrical characteristics[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800.0	-	1600.0	mV	2

Table continues on the next page...

This table provides the DC electrical characteristics for the I^2C interface operating at DV_{DD} = 1.8 V.

Table 115. I^2C DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x DV_{DD}	V	2
Output low voltage (DV_{DD} = min, IOL = 3 mA, DV_{DD} ≤ 2V)	V_{OL}	0.0	0.36	V	3
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	4
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} (min) and 0.9 x DV_{DD} (max))	I_I	-50.0	50.0	µA	5
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
3. The output voltage (open drain or open collector) condition = 3 mA sink current.
4. See the chip reference manual for information about the digital filter used.
5. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.

3.17.2 I^2C AC timing specifications

This table provides the AC timing specifications for the I^2C interface.

Table 116. I^2C AC timing specifications[1]

Parameter	Symbol	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0.0	400.0	kHz	-
Low period of the SCL clock	t_{I2CL}	1.3	-	µs	-
High period of the SCL clock	t_{I2CH}	0.6	-	µs	-
Setup time for a repeated START condition	t_{I2SVKH}	0.6	-	µs	-
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	-	µs	-
Data setup time	t_{I2DVKH}	100.0	-	ns	-
Data input hold time (CBUS compatible masters, I^2C bus devices)	t_{I2DXKL}	0.0	-	µs	As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation

Table continues on the next page...

3.18.2 Integrated Flash Controller AC timing specifications

This section describes the AC timing specifications for the integrated flash controller.

3.18.2.1 Test condition

The figure below provides the AC test load for the integrated flash controller.

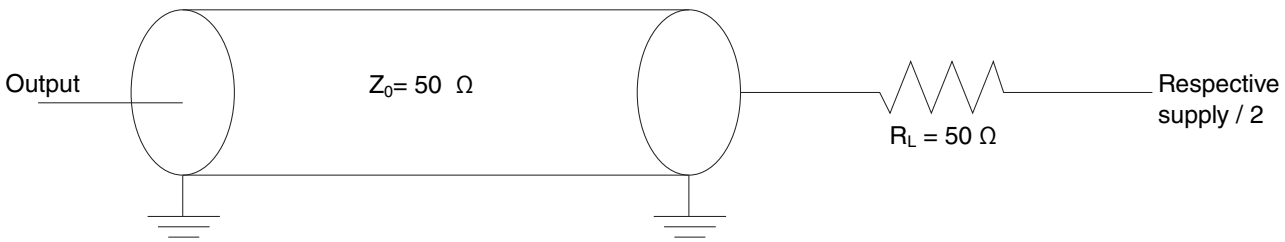

Figure 47. Integrated Flash Controller AC test load

3.18.2.2 IFC AC timing specifications (GPCM/GASIC)

The table below describes the input AC timing specifications for the IFC-GPCM and IFC-GASIC interface.

Table 118. Integrated flash controller input timing specifications for GPCM and GASIC mode (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH1}$	4	-	ns	-
Input hold	$t_{IBIXKH1}$	1	-	ns	-

NOTE:

1. For recommended operating conditions, see Table 3.

The figure below shows the input AC timing diagram for the IFC-GPCM, IFC-GASIC interface.

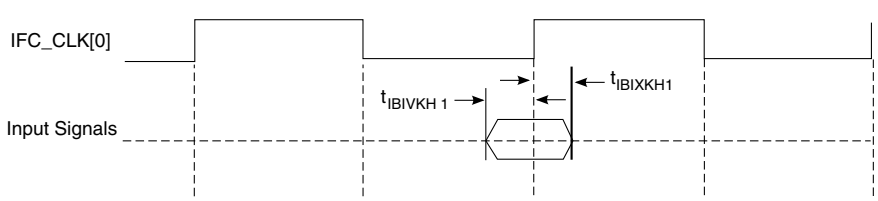

Figure 48. IFC-GPCM, IFC-GASIC input AC timing specifictions

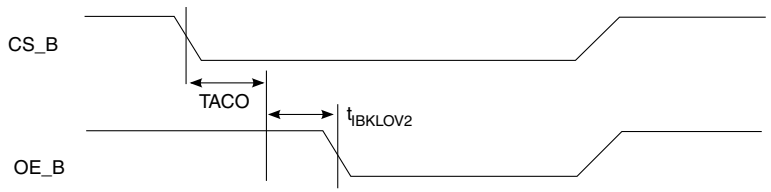

Figure 51. IFC-NOR interface output AC timings

3.18.2.4 IFC AC timing specifications (NAND)

The table below describes the input timing specifications of the IFC-NAND interface.

Table 122. Integrated flash controller input timing specifications for NAND mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH3}$	(2 x t_{IP_CLK}) + 2	-	ns	1
Input hold	$t_{IBIXKH3}$	1	-	ns	1
IFC_RB_B pulse width	t_{IBCH}	2	-	t_{IP_CLK}	1
NOTE: 1. t_{IP_CLK} is the period of ip clock on which IFC is running. 2. For recommended operating conditions, see Table 3.					

The figure below shows the AC input timing diagram for input signals of IFC-NAND interface. Here TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.

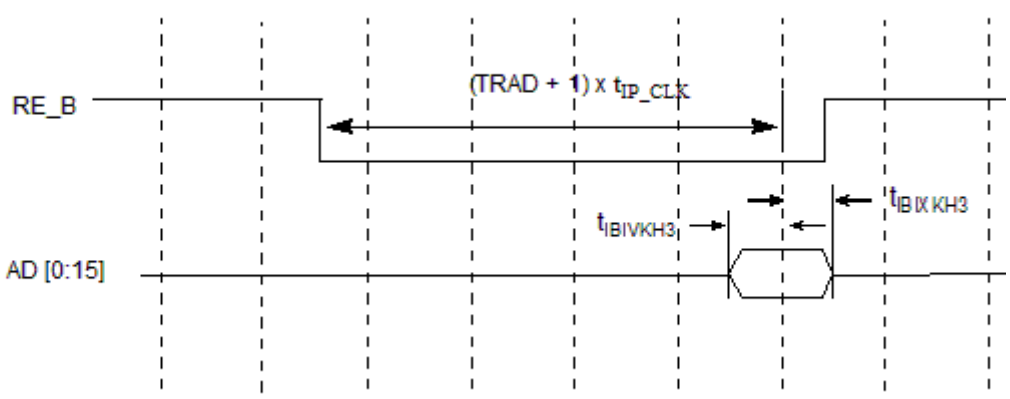

Figure 52. IFC-NAND interface input AC timings

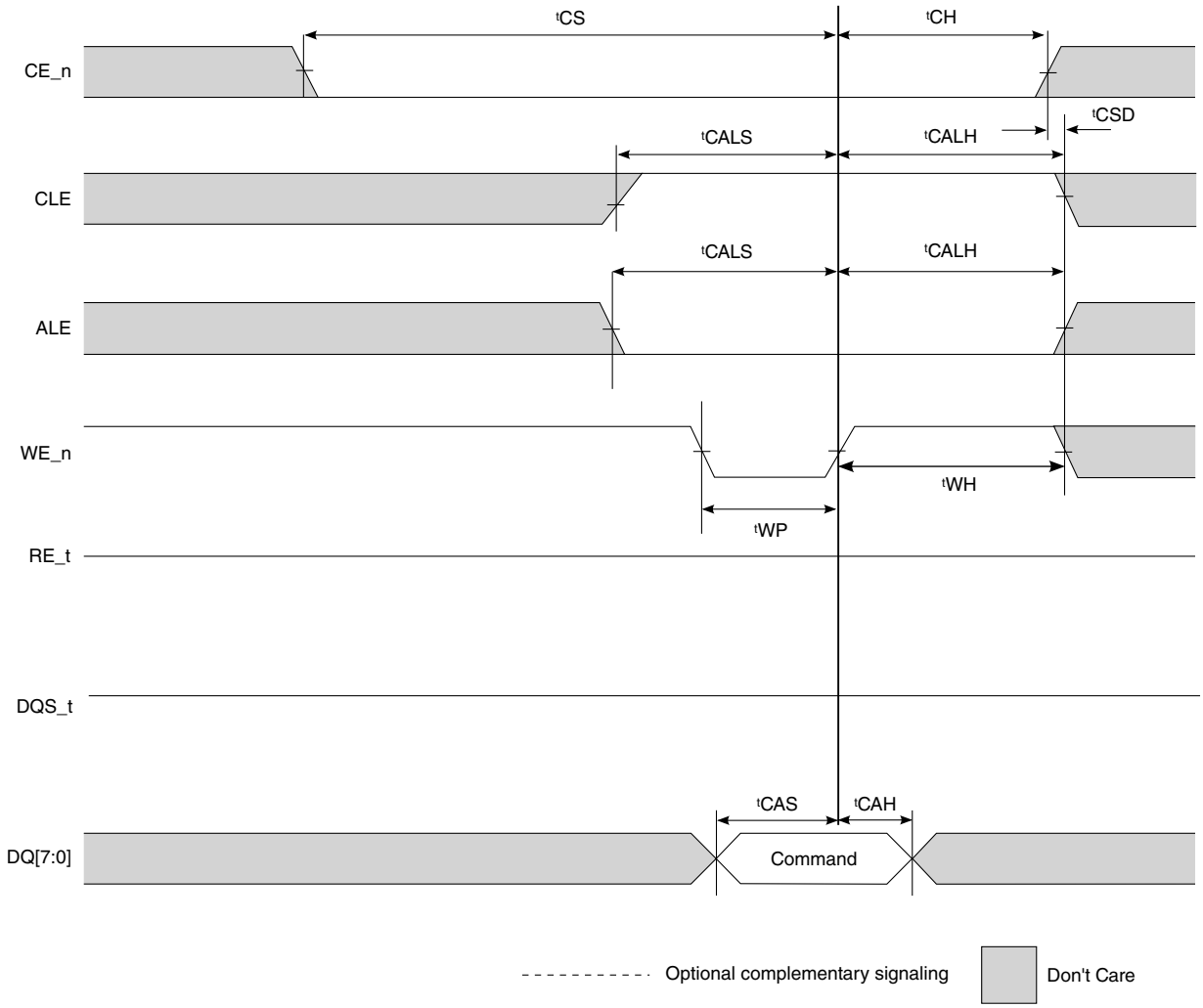

Figure 55. Command cycle

This figure shows the t_{AR} timings.

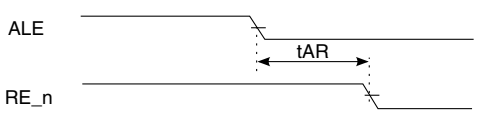

Figure 56. t_{AR} timings

This figure shows the data input cycle timings.

Table 127. JTAG AC timing specifications[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
					question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
Output hold times	t_{JTKLDX}	0.0	-	ns	All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the tJTG clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the tJTG clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the AC test load for TDO and the boundary-scan outputs of the device.

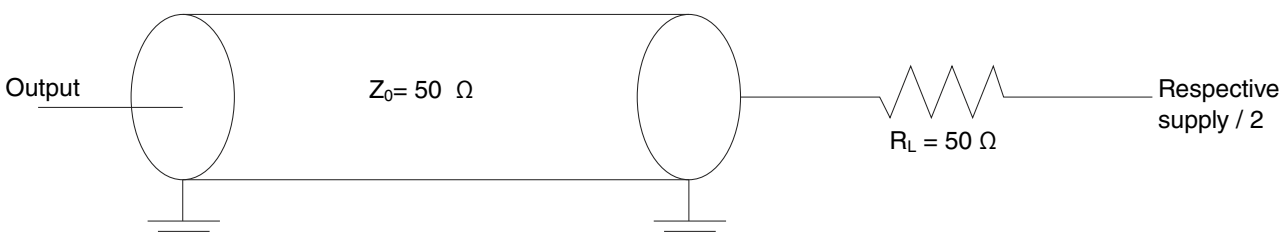

Figure 78. AC test load for the JTAG interface

This figure shows the JTAG clock input timing diagram.

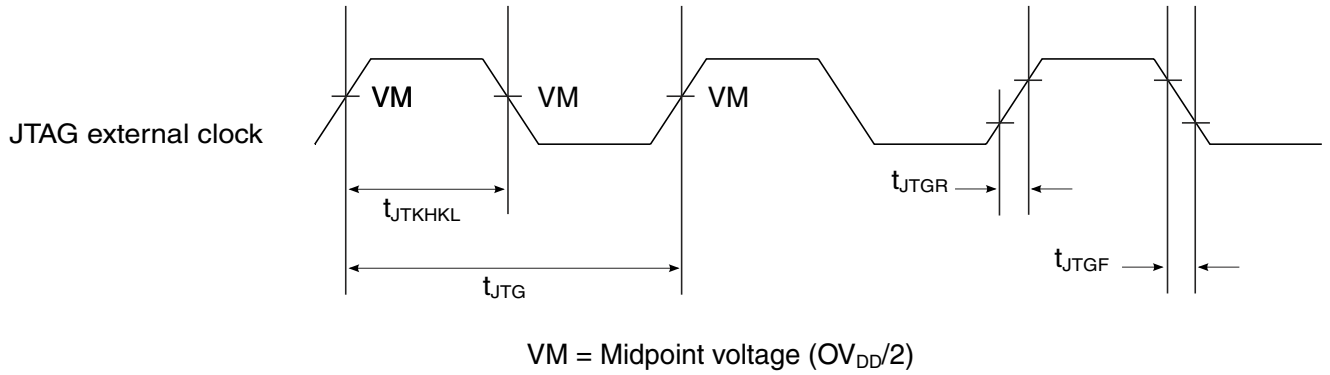

Figure 79. JTAG clock input timing diagram

This figure shows the TRST_B timing diagram.

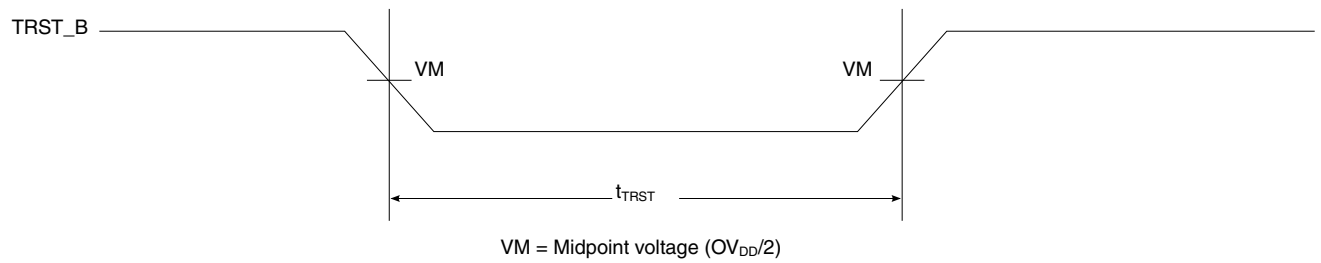

Figure 80. TRST_B timing diagram

This figure shows the boundary-scan timing diagram.

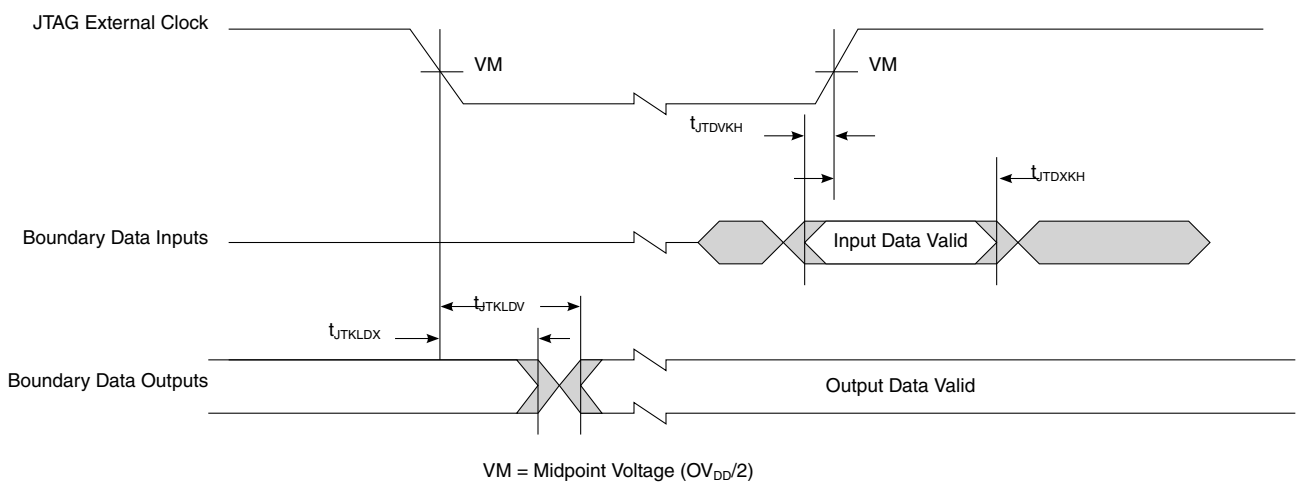

Figure 81. Boundary-scan timing diagram

Table 146. LFPS electrical specifications at the transmitter (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Peak-to-peak differential amplitude	$V_{tx\text{-}diff\text{-}pp\text{-}lfps}$	800.0	1200.0	mV	-
Low-power peak-to-peak differential amplitude	$V_{tx\text{-}diff\text{-}pp\text{-}lfps\text{-}lp}$	400.0	600.0	mV	-
Rise/fall time	$t_{rise/fall}$	-	4.0	ns	Measured at compliance TP1. See the Transmit normative setup figure below for details.
Duty cycle	DC_{LFPS}	40.0	60.0	%	Measured at compliance TP1. See the Transmit normative setup figure below for details.

This figure shows the Tx normative setup with reference channel per USB 3.0 specifications.

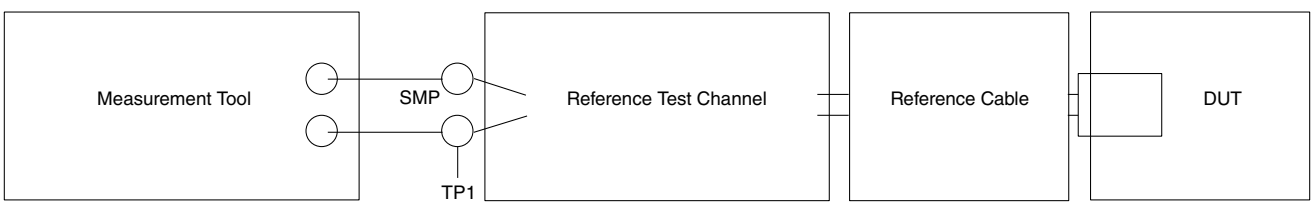

Figure 94. Transmit normative setup

4 Hardware design considerations

4.1 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.