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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	8 Core, 64-Bit
Speed	1.6GHz
Co-Processors/DSP	-
RAM Controllers	DDR4
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	10GbE (2), 1GbE (8)
SATA	SATA 6Gbps (1)
USB	USB 3.0 (2) + PHY
Voltage - I/O	-
Operating Temperature	-40°C ~ 105°C
Security Features	Secure Boot, TrustZone®
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ls1088axn7q1a

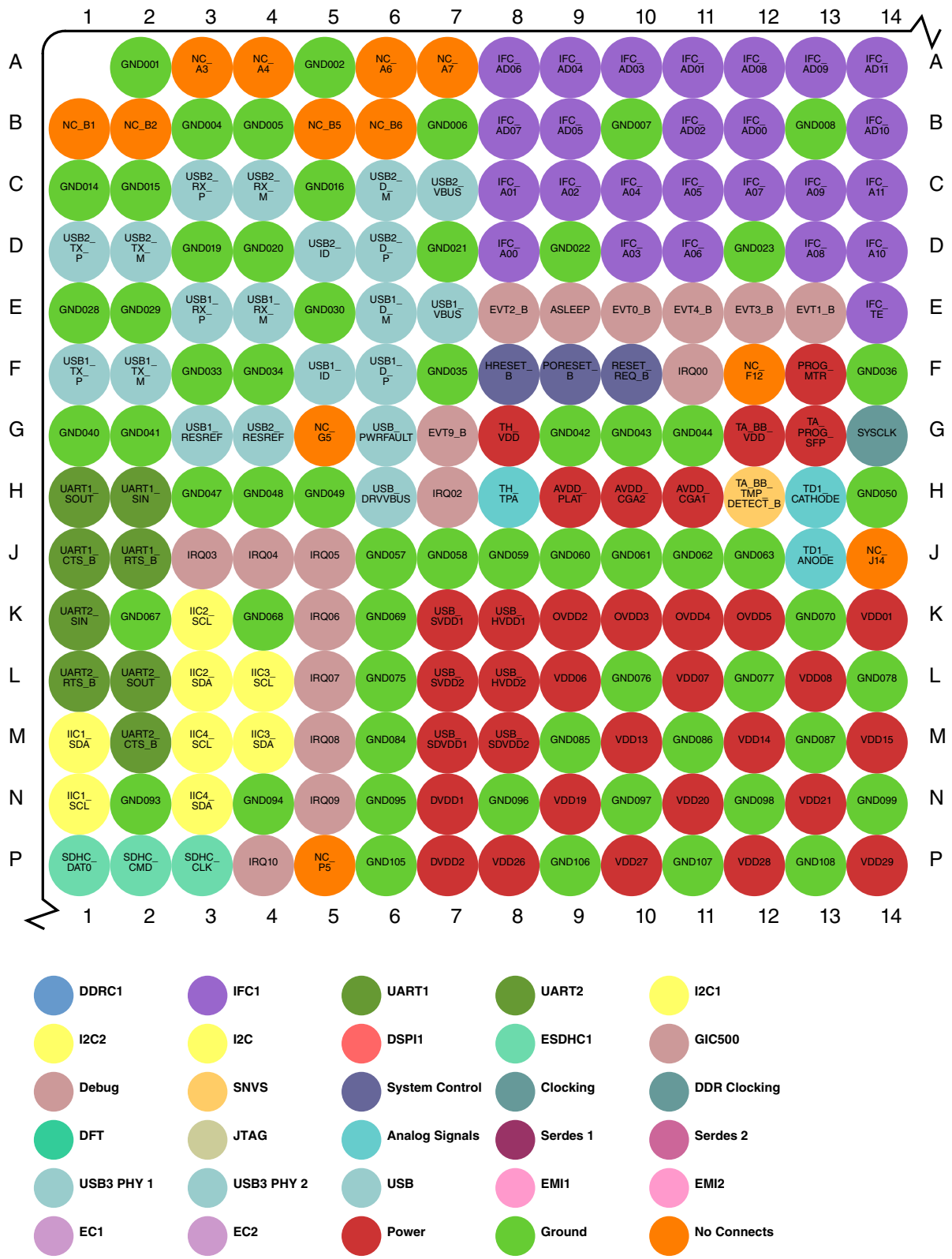


Figure 3. Detail A

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ26	Data	L24	IO	$G1V_{DD}$	---
D1_MDQ27	Data	M24	IO	$G1V_{DD}$	---
D1_MDQ28	Data	J22	IO	$G1V_{DD}$	---
D1_MDQ29	Data	H23	IO	$G1V_{DD}$	---
D1_MDQ30	Data	K24	IO	$G1V_{DD}$	---
D1_MDQ31	Data	L25	IO	$G1V_{DD}$	---
D1_MDQ32	Data	V24	IO	$G1V_{DD}$	---
D1_MDQ33	Data	U26	IO	$G1V_{DD}$	---
D1_MDQ34	Data	AA26	IO	$G1V_{DD}$	---
D1_MDQ35	Data	W23	IO	$G1V_{DD}$	---
D1_MDQ36	Data	U24	IO	$G1V_{DD}$	---
D1_MDQ37	Data	U25	IO	$G1V_{DD}$	---
D1_MDQ38	Data	W24	IO	$G1V_{DD}$	---
D1_MDQ39	Data	Y25	IO	$G1V_{DD}$	---
D1_MDQ40	Data	AB24	IO	$G1V_{DD}$	---
D1_MDQ41	Data	AB25	IO	$G1V_{DD}$	---
D1_MDQ42	Data	AE25	IO	$G1V_{DD}$	---
D1_MDQ43	Data	AF25	IO	$G1V_{DD}$	---
D1_MDQ44	Data	Y24	IO	$G1V_{DD}$	---
D1_MDQ45	Data	AA25	IO	$G1V_{DD}$	---
D1_MDQ46	Data	AD25	IO	$G1V_{DD}$	---
D1_MDQ47	Data	AE26	IO	$G1V_{DD}$	---
D1_MDQ48	Data	AA22	IO	$G1V_{DD}$	---
D1_MDQ49	Data	AB23	IO	$G1V_{DD}$	---
D1_MDQ50	Data	AC22	IO	$G1V_{DD}$	---
D1_MDQ51	Data	AB22	IO	$G1V_{DD}$	---
D1_MDQ52	Data	Y22	IO	$G1V_{DD}$	---
D1_MDQ53	Data	AA23	IO	$G1V_{DD}$	---
D1_MDQ54	Data	AD22	IO	$G1V_{DD}$	---
D1_MDQ55	Data	AE22	IO	$G1V_{DD}$	---
D1_MDQ56	Data	AH25	IO	$G1V_{DD}$	---
D1_MDQ57	Data	AF24	IO	$G1V_{DD}$	---
D1_MDQ58	Data	AG22	IO	$G1V_{DD}$	---
D1_MDQ59	Data	AF22	IO	$G1V_{DD}$	---
D1_MDQ60	Data	AH26	IO	$G1V_{DD}$	---
D1_MDQ61	Data	AG25	IO	$G1V_{DD}$	---
D1_MDQ62	Data	AF23	IO	$G1V_{DD}$	---
D1_MDQ63	Data	AH22	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_RB1_B/GPIO2_15	IFC Ready/Busy CS1	D16	I	OV_{DD}	1, 6
IFC_RB2_B/**IFC_A09**/ GPIO2_03/IFC_CS_B4/ QSPI_A_DATA3	IFC Ready/Busy CS 2	C13	I	OV_{DD}	1
IFC_RB3_B/**IFC_A10**/ GPIO2_04/IFC_CS_B5/ QSPI_A_DQS	IFC Ready/Busy CS 3	D14	I	OV_{DD}	1
IFC_TE/GPIO1_23/cfg_ifc_te	IFC External Transceiver Enable	E14	O	OV_{DD}	1, 4
IFC_WE0_B/GPIO1_22/ cfg_eng_use0	IFC Write Enable 0 / Start of Frame	C15	O	OV_{DD}	1, 4, 19
IFC_WP0_B/GPIO1_27/ cfg_eng_use2	IFC Write Protect	D19	O	OV_{DD}	1, 5
IFC_WP1_B/**IFC_A06**/ GPIO2_00/QSPI_A_DATA0	IFC Write Protect	D11	O	OV_{DD}	1
IFC_WP2_B/**IFC_A07**/ GPIO2_01/QSPI_A_DATA1	IFC Write Protect	C12	O	OV_{DD}	1
IFC_WP3_B/**IFC_A08**/ GPIO2_02/QSPI_A_DATA2	IFC Write Protect	D13	O	OV_{DD}	1
DUART1					
UART1_CTS_B/GPIO3_10/ UART3_SIN	Clear To Send	J1	I	DV_{DD}	1
UART1_RTS_B/GPIO3_08/ UART3_SOUT	Ready to Send	J2	O	DV_{DD}	1
UART1_SIN	Receive Data	H2	I	DV_{DD}	1
UART1_SOUT	Transmit Data	H1	O	DV_{DD}	1
DUART2					
UART2_CTS_B/GPIO3_11/ UART4_SIN	Clear To Send	M2	I	DV_{DD}	1
UART2_RTS_B/GPIO3_09/ UART4_SOUT	Ready to Send	L1	O	DV_{DD}	1
UART2_SIN/GPIO3_07	Receive Data	K1	I	DV_{DD}	1
UART2_SOUT/GPIO3_06	Transmit Data	L2	O	DV_{DD}	1
DUART3 and 4					
UART3_SIN/**UART1_CTS_B**/ GPIO3_10	Receive Data	J1	I	DV_{DD}	1
UART3_SOUT/ **UART1_RTS_B**/GPIO3_08	Transmit Data	J2	O	DV_{DD}	1
UART4_SIN/**UART2_CTS_B**/ GPIO3_11	Receive Data	M2	I	DV_{DD}	1
UART4_SOUT/ **UART2_RTS_B**/GPIO3_09	Transmit Data	L1	O	DV_{DD}	1
I2C1					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND119	Core, Platform and PLL Ground	R18	---	---	---
GND120	Core, Platform and PLL Ground	R20	---	---	---
GND121	Core, Platform and PLL Ground	R23	---	---	---
GND122	Core, Platform and PLL Ground	R26	---	---	---
GND123	Core, Platform and PLL Ground	T2	---	---	---
GND124	Core, Platform and PLL Ground	T4	---	---	---
GND125	Core, Platform and PLL Ground	T6	---	---	---
GND126	Core, Platform and PLL Ground	T9	---	---	---
GND127	Core, Platform and PLL Ground	T11	---	---	---
GND128	Core, Platform and PLL Ground	T13	---	---	---
GND129	Core, Platform and PLL Ground	T15	---	---	---
GND130	Core, Platform and PLL Ground	T17	---	---	---
GND131	Core, Platform and PLL Ground	T19	---	---	---
GND132	Core, Platform and PLL Ground	T21	---	---	---
GND133	Core, Platform and PLL Ground	T23	---	---	---
GND134	Core, Platform and PLL Ground	T26	---	---	---
GND135	Core, Platform and PLL Ground	U6	---	---	---
GND136	Core, Platform and PLL Ground	U8	---	---	---
GND137	Core, Platform and PLL Ground	U10	---	---	---
GND138	Core, Platform and PLL Ground	U12	---	---	---
GND139	Core, Platform and PLL Ground	U14	---	---	---
GND140	Core, Platform and PLL Ground	U16	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND02	SerDes core logic, transceiver, and PLL ground	Y7	---	---	18
SD_GND03	SerDes core logic, transceiver, and PLL ground	Y8	---	---	18
SD_GND04	SerDes core logic, transceiver, and PLL ground	Y9	---	---	18
SD_GND05	SerDes core logic, transceiver, and PLL ground	Y10	---	---	18
SD_GND06	SerDes core logic, transceiver, and PLL ground	Y13	---	---	18
SD_GND07	SerDes core logic, transceiver, and PLL ground	Y14	---	---	18
SD_GND08	SerDes core logic, transceiver, and PLL ground	Y15	---	---	18
SD_GND09	SerDes core logic, transceiver, and PLL ground	Y16	---	---	18
SD_GND10	SerDes core logic, transceiver, and PLL ground	AA5	---	---	18
SD_GND11	SerDes core logic, transceiver, and PLL ground	AA7	---	---	18
SD_GND12	SerDes core logic, transceiver, and PLL ground	AA9	---	---	18
SD_GND13	SerDes core logic, transceiver, and PLL ground	AA12	---	---	18
SD_GND14	SerDes core logic, transceiver, and PLL ground	AA14	---	---	18
SD_GND15	SerDes core logic, transceiver, and PLL ground	AA17	---	---	18
SD_GND16	SerDes core logic, transceiver, and PLL ground	AA18	---	---	18
SD_GND17	SerDes core logic, transceiver, and PLL ground	AA19	---	---	18
SD_GND18	SerDes core logic, transceiver, and PLL ground	AB7	---	---	18
SD_GND19	SerDes core logic, transceiver, and PLL ground	AB9	---	---	18
SD_GND20	SerDes core logic, transceiver, and PLL ground	AB12	---	---	18
SD_GND21	SerDes core logic, transceiver, and PLL ground	AB14	---	---	18
SD_GND22	SerDes core logic, transceiver, and PLL ground	AB17	---	---	18
SD_GND23	SerDes core logic, transceiver, and PLL ground	AB20	---	---	18

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD18	DDR supply	AA27	---	$G1V_{DD}$	---
G1VDD19	DDR supply	AC27	---	$G1V_{DD}$	---
G1VDD20	DDR supply	AE27	---	$G1V_{DD}$	---
G1VDD21	DDR supply	AG27	---	$G1V_{DD}$	---
G1VDD22	DDR supply	AH27	---	$G1V_{DD}$	---
SVDD1	SerDes transceiver supply	W7	---	SV_{DD}	---
SVDD2	SerDes transceiver supply	W8	---	SV_{DD}	---
SVDD3	SerDes transceiver supply	W9	---	SV_{DD}	---
SVDD4	SerDes transceiver supply	W10	---	SV_{DD}	---
SVDD5	SerDes transceiver supply	W13	---	SV_{DD}	---
SVDD6	SerDes transceiver supply	W14	---	SV_{DD}	---
SVDD7	SerDes transceiver supply	W15	---	SV_{DD}	---
SVDD8	SerDes transceiver supply	W16	---	SV_{DD}	---
XVDD1	SerDes transceiver supply	AC7	---	XV_{DD}	---
XVDD2	SerDes transceiver supply	AC9	---	XV_{DD}	---
XVDD3	SerDes transceiver supply	AC12	---	XV_{DD}	---
XVDD4	SerDes transceiver supply	AC14	---	XV_{DD}	---
XVDD5	SerDes transceiver supply	AC17	---	XV_{DD}	---
XVDD6	SerDes transceiver supply	AC20	---	XV_{DD}	---
FA_VL	Reserved	AB21	---	FA_VL	---
PROG_MTR	Reserved	F13	---	PROG_MTR	---
TA_PROG_SFP	SFP Fuse Programming Override supply	G13	---	TA_PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	G8	---	TH_V_{DD}	---
VDD01	Supply for cores and platform	K14	---	V_{DD}	---
VDD02	Supply for cores and platform	K16	---	V_{DD}	---
VDD03	Supply for cores and platform	K18	---	V_{DD}	---
VDD04	Supply for cores and platform	K20	---	V_{DD}	---
VDD05	Supply for cores and platform	K22	---	V_{DD}	---
VDD06	Supply for cores and platform	L9	---	V_{DD}	---
VDD07	Supply for cores and platform	L11	---	V_{DD}	---
VDD08	Supply for cores and platform	L13	---	V_{DD}	---
VDD09	Supply for cores and platform	L15	---	V_{DD}	---
VDD10	Supply for cores and platform	L17	---	V_{DD}	---
VDD11	Supply for cores and platform	L19	---	V_{DD}	---
VDD12	Supply for cores and platform	L21	---	V_{DD}	---
VDD13	Supply for cores and platform	M10	---	V_{DD}	---
VDD14	Supply for cores and platform	M12	---	V_{DD}	---

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Characteristic		Symbol	Min	Max	Unit	Notes
	3/4/5/6/7/8/9/10), USB control (DRVVBUS, PWRFAULT)					
	Ethernet management interface 2 (EMI2), GPIO2	TV_{IN}	-0.3	TV_{DD} + 0.3	V	13
USB PHY transceiver supply voltage	Transceiver supply for USB PHY	USB_HV_{IN}	-0.3	USB_HV_{DD} + 0.3	V	10
	Analog and Digital HS supply for USB PHY	USB_SDV_{DD}	-0.3	USB_SDV_{DD} + 0.3	V	11
	Analog and Digital SS supply for USB PHY	USB_SV_{DD}	-0.3	USB_SV_{DD} + 0.3	V	12
Storage temperature range		T_{STG}	-55	150	°C	--

Notes:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

5. (D, G1, L, O, X, S, T, E)V_{IN} and $USBn\_HV_{IN}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

6. **Caution:** DV_{IN} must not exceed DV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

7. **Caution:** EV_{IN} must not exceed EV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

8. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

9. See the power supply column to determine which power supply rail is used for each interface.

10. Transceiver supply for USB PHY.

11. Analog and Digital SS supply for USB PHY.

12. Analog and Digital HS supply for USB PHY.

13. **Caution:** TV_{IN} must not exceed TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3.1.2 Recommended operating conditions

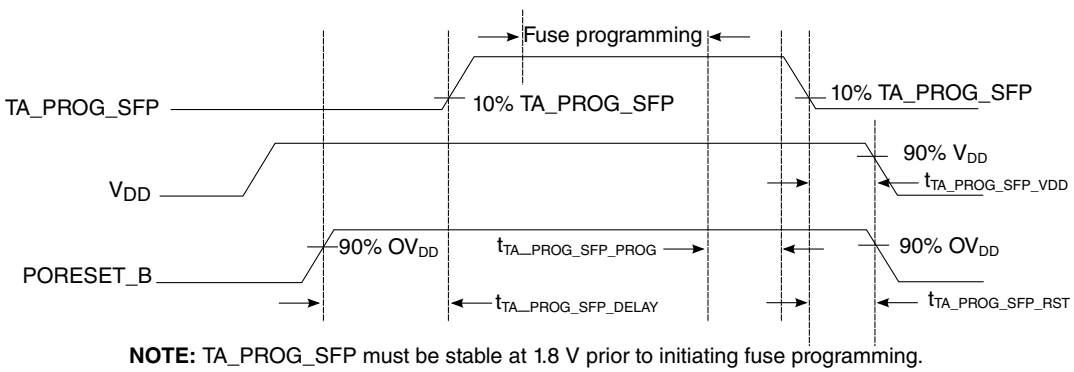
This table provides the recommended operating conditions for this chip.

2. After fuse programming is completed, it is required to return TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 6. See Security fuse processor for additional details.

Warning

No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND.

This figure shows the TA_PROG_SFP timing diagram.



NOTE: TA_PROG_SFP must be stable at 1.8 V prior to initiating fuse programming.

Figure 9. TA_PROG_SFP timing diagram

This table provides information on the power-down and power-up sequence parameters for TA_PROG_SFP.

Table 6. TA_PROG_SFP timing [5]

Driver type	Min	Max	Unit	Notes
$t_{TA\_PROG\_SFP\_DELAY}$	100	—	SYSCLKs	1
$t_{TA\_PROG\_SFP\_PROG}$	0	—	us	2
$t_{TA\_PROG\_SFP\_VDD}$	0	—	us	3
$t_{TA\_PROG\_SFP\_RST}$	0	—	us	4

Notes:

1. Delay required from the deassertion of PORESET_B to driving TA_PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% TA_PROG_SFP ramp up.

2. Delay required from fuse programming completion to TA_PROG_SFP ramp down start. Fuse programming must complete while TA_PROG_SFP is stable at 1.8 V. No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND. After fuse programming is complete, it is required to return TA_PROG_SFP = GND.

3.7.1.1 SYSCLK DC electrical characteristics

This table provides the SYSCLK DC characteristics.

Table 12. SYSCLK DC electrical characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 X OV_{DD}	—	—	V	1
Input low voltage	V_{IL}	—	—	0.3 X OV_{DD}	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (V_{IN}= 0 V or V_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. At recommended operating conditions with OV_{DD}= 1.8 V. See Table 3.

3.7.1.2 SYSCLK AC timing specifications

This table provides the SYSCLK AC timing specifications.

Table 13. SYSCLK AC timing specifications[1, 5]

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	100.0	—	125/133.3	MHz	2, 6
SYSCLK cycle time	t_{SYSCLK}	7.5	—	10.0	ns	1, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at -56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	1.08	—	1.8	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequencies do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8 V. See Table 3.
6. The 125 MHz max frequency is limited to parts with 1200 MHz CPU frequency. The 133 MHz max frequency can be used for parts with 1600 MHz and 1400 MHz CPU frequency.

Table 34. eSDHC interface DC electrical characteristics (E/D/OV_{DD}=1.8 V)[3] (continued)

Characteristic	Symbol	Min	Max	Unit	Notes
Input/output leakage current	(I_{IN}/I_{OZ})	-10	10	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max E/D/OV_{IN} values found in the Table 3.
2. Open-drain mode is for MMC cards only.
3. At recommended operating conditions with E/D/OV_{DD} = 1.8 V.

3.12.2 eSDHC AC timing specifications

This section provides the AC timing specifications.

This table provides the eSDHC AC timing specifications as defined in Figure 14, Figure 15, and Figure 16.

Table 35. eSDHC AC timing specifications (full-speed/high-speed mode)[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency: • SD/SDIO (full-speed/high-speed mode) • MMC (full-speed/high-speed mode)	f_{SHSCK}	0	25/50 20/52	MHz	2, 4
SDHC_CLK clock low time (full-speed/high-speed mode)	t_{SHSCKL}	10/7	-	ns	4
SDHC_CLK clock high time (full-speed/high-speed mode)	t_{SHSCKH}	10/7	-	ns	4
SDHC_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK	$t_{SHSIVKH}$	2.5	-	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK	$t_{SHSIXKH}$	2.5	-	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOX}$	-3	-	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOV}$	-	3	ns	4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC high-speed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0-25MHz for an SD/SDIO card and 0-20MHz for an MMC card. In high-speed mode, the clock frequency value can be 0-50MHz for an SD/SDIO card and 0-52MHz for an MMC card.

Table 37. eSDHC AC timing specifications (DDR50/DDR)[3] (continued)

Parameter	Symbol	Min	Max	Units	Notes
Notes:					
1. C_{CARD} ≤ 10 pF, (1 card).					
2. $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ ≤ 20 pF for MMC, ≤ 25pF for Input Data of DDR50, ≤ 30pF for Input CMD of DDR50.					
3. For recommended operating conditions, see Table 3.					
4. Total clock duty cycle and data and clock skew on the board should be limited to 0.2ns.					
5. Total clock duty cycle and command and clock skew on the board should be limited to 0.3ns.					

This figure provides the eSDHC DDR50/DDR mode input AC timing diagram.

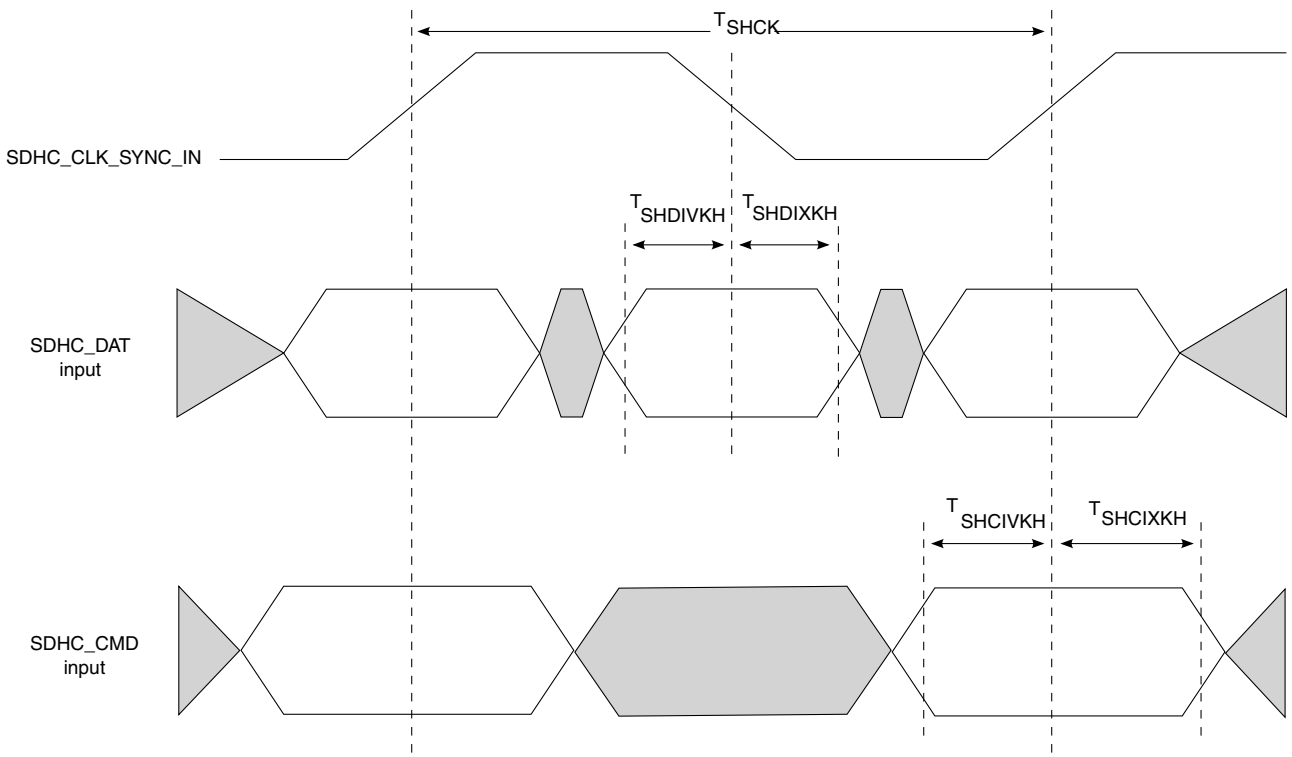


Figure 20. eSDHC DDR50/DDR mode input AC timing diagram

This figure provides the eSDHC DDR50/DDR mode output AC timing diagram.

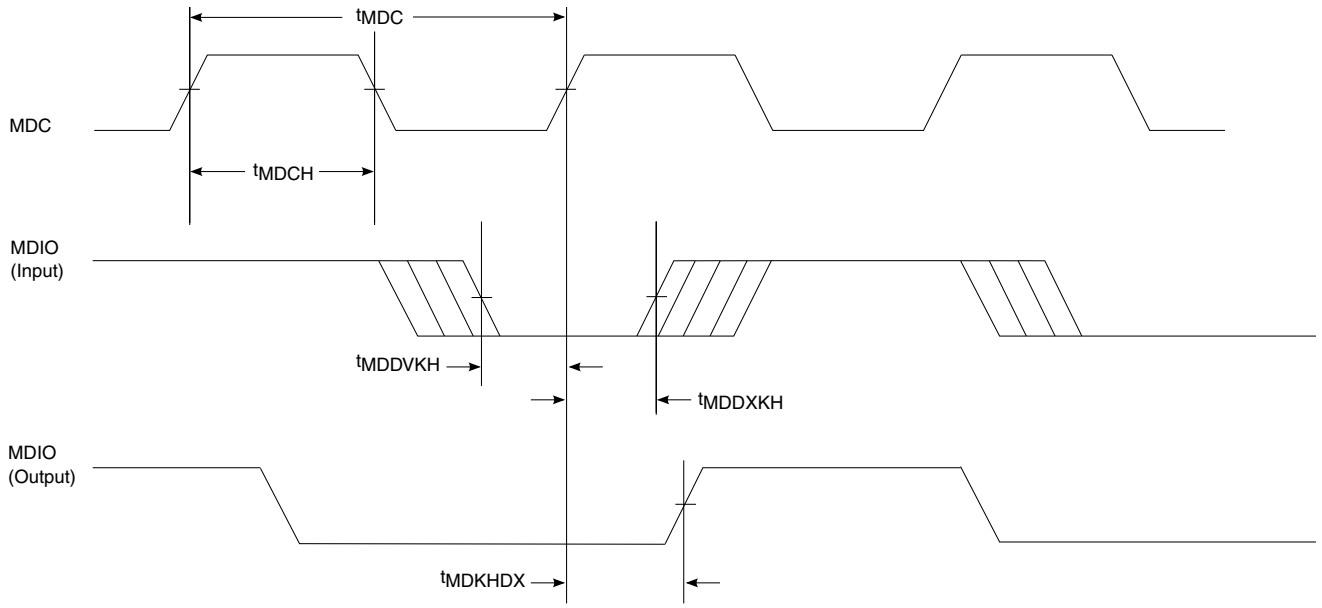


Figure 23. Ethernet management interface 1 timing diagram

3.13.1.2 Ethernet management interface 2 (EMI2)

This section describes the electrical characteristics for the EMI2 interface.

The EMI2 interface timing is compatible with IEEE Std 802.3™ clause 45.

3.13.1.2.1 EMI2 DC electrical characteristics

This section describes the DC electrical characteristics for EMI2_MDIO and EMI2_MDC. The pins are available on TV_{DD}. For operating voltages, see Table 3.

This table provides the EMI2 DC electrical characteristics when operating at TV_{DD} = 2.5 V.

Table 42. EMI2 DC electrical characteristics (TV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TVDD	-	-	2
Input low voltage	V_{IL}	-	0.2 x TVDD	-	2
Input current (V_{IN} = 0 or V_{IN} = TV_{DD})	I_{IN}	-50.0	50.0	-	3, 4
Output high voltage (TV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.0	-	-	4
Output low voltage (TV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	-	0.4	-	4

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3.

3.14.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for the GPIO interface operating at D/EV_{DD} = 3.3 V.

Table 52. GPIO DC electrical characteristics (D/EV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/EV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x D/EV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (D/EV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (D/EV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN}/EV_{IN} values found in Table 3. 3. The symbol DV_{IN}/EV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at TV_{DD} = 2.5 V.

Table 53. GPIO DC electrical characteristics (TV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x TV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (TV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (TV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3. 3. The symbol TV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at $D/E/TV_{DD}$ = 1.8 V.

Table 54. GPIO DC electrical characteristics ($D/E/TV_{DD}$ = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $D/E/TV_{DD}$	-	V	2

Table continues on the next page...

Table 79. Gen1i/1m 1.5 G transmitter DC specifications (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Tx differential output voltage	V_{SATA_TXDIFF}	400	500	600	mV p-p	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	2

Notes:

1. Terminated by 50 Ω load.
2. DC impedance.
3. For recommended operating conditions, see Table 3.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission.

Table 80. Gen 2i/2m 3 G transmitter DC specifications (XV_{DD} = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	400	—	700	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Notes:

1. Terminated by 50 Ω load.
2. For recommended operating conditions, see Table 3.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen 3i transmission.

Table 81. Gen 3i transmitter DC specifications (XV_{DD} = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	240	—	900	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Notes:

1. Terminated by 50 Ω load.
2. For recommended operating conditions, see Table 3.

3.16.5.1.2 SATA DC receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

3.16.6 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 39, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100 Ω output impedance. Each input of the SerDes receiver differential pair features 50 Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 36.

3.16.6.1 SGMII clocking requirements for SDn_REF_CLK1_P and SDn_REF_CLK1_N

When operating in SGMII mode, the EC*n*_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N pins. SerDes lanes may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.16.6.2 SGMII DC electrical characteristics

This section describes the electrical characteristics for the SGMII interface.

3.16.6.2.1 SGMII and SGMII 2.5 G transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N)as shown in Figure 40.

Table 92. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD} \rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD} \rvert_{-min}/2$	-	-	mV	1
Output differential voltage[2, 3, 5] (XV_{DD-Typ} at 1.35 V)	$\lvert V_{OD} \rvert$	320	500.0	725.0	mV	TECR0[AMP_RED]=0b000000
		293.8	459.0	665.6		TECR0[AMP_RED]=0b000001
		266.9	417.0	604.7		TECR0[AMP_RED]=0b000011
		240.6	376.0	545.2		TECR0[AMP_RED]=0b000010

Table continues on the next page...

Table 96. SGMII transmit AC timing specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Notes:						
1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.						
2. See Figure 42 for single frequency sinusoidal jitter measurements.						
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.						
4. For recommended operating conditions, see Table 3.						

3.16.6.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) or at the receiver inputs (SD*n*_RX*n*_P and SD*n*_RX*n*_N) respectively, as shown in this figure.

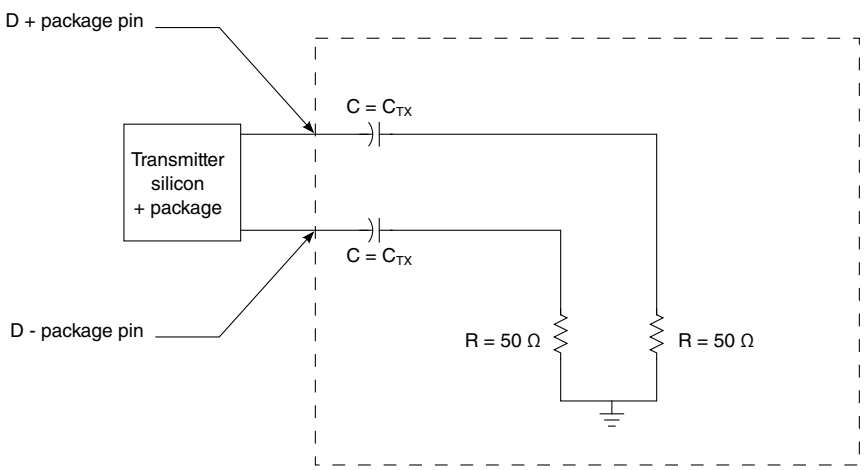


Figure 41. SGMII AC test/measurement load

3.16.6.3.3 SGMII and SGMII 2.5 G receiver AC timing specifications

This table provides the SGMII and SGMII 2.5 G receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 97. SGMII receiver AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2

Table continues on the next page...

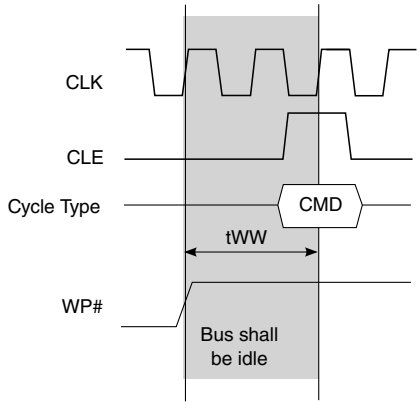


Figure 66. t_{WW} timings

This figure shows the $t_{IBIXKH4}$ timings.

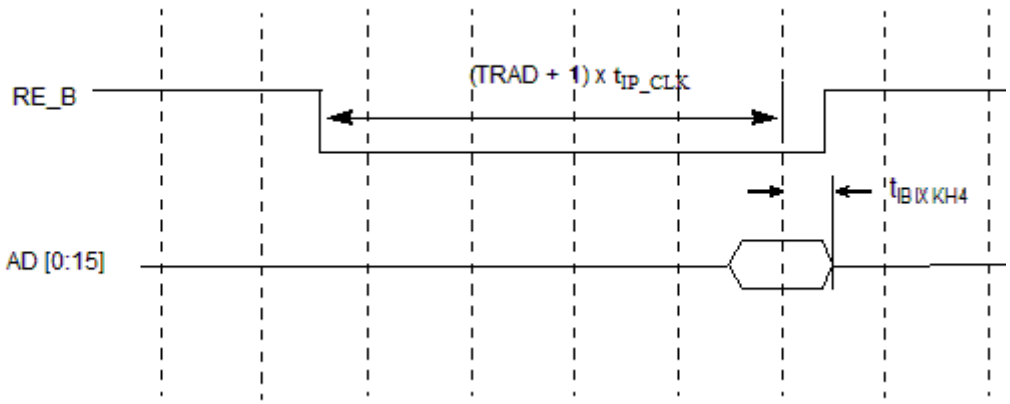


Figure 67. $t_{IBIXKH4}$ timings

3.18.2.6 IFC-NAND NVDDR AC timing specification

The table below describes the AC timing specifications for the IFC-NAND NVDDR interface. These specifications are compliant to NVDDR mode of ONFI specification revision 3.0.

Table 125. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Access window of DQ[7:0] from CLK	t_{AC}	I	3 - 150 (ps)	20 + 150 (ps)	ns	Figure 71
Address cycle to data loading time	t_{ADL}	I	TADL	-	t_{IP_CLK}	Figure 72

Table continues on the next page...

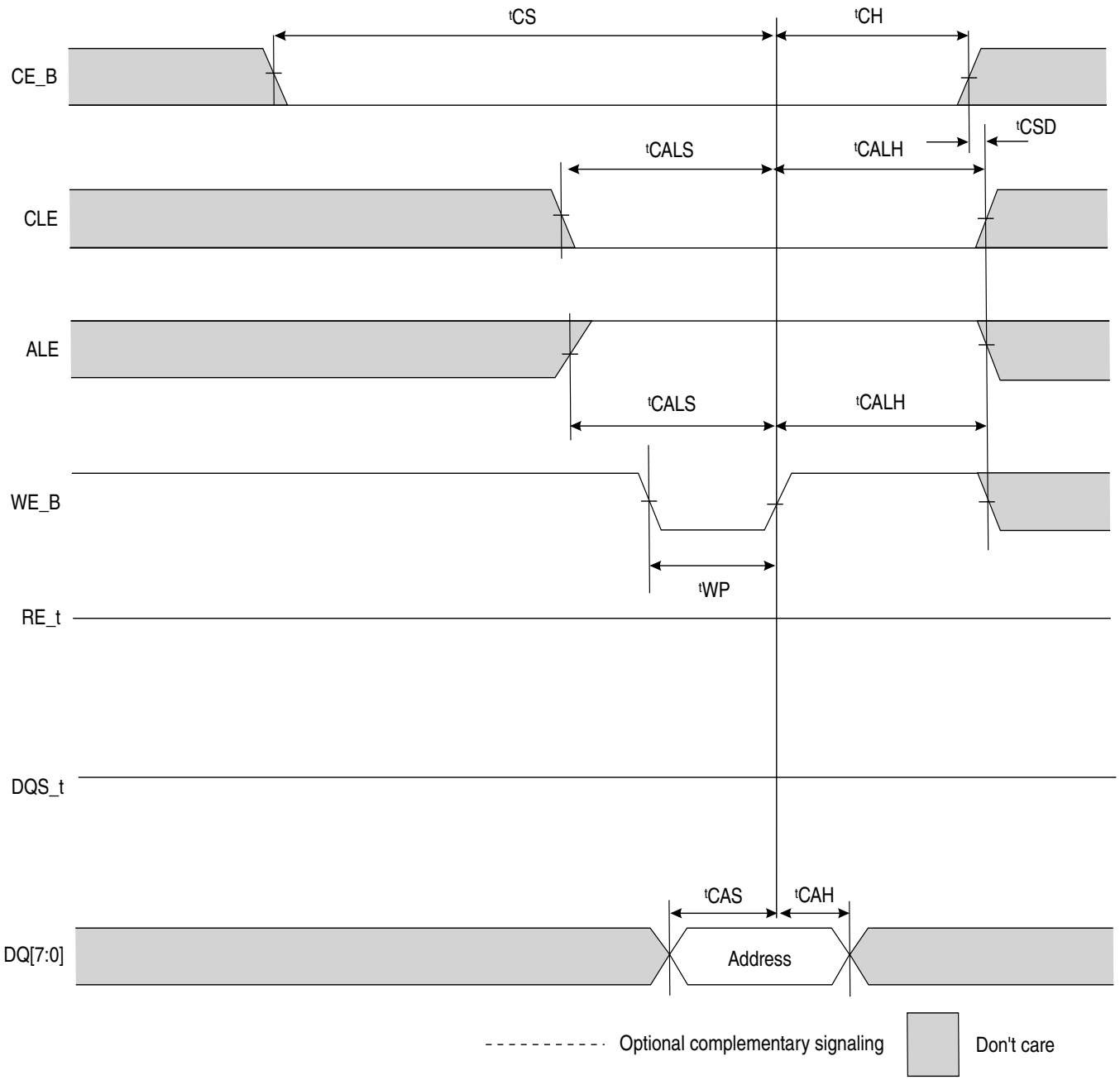


Figure 69. Address cycle

Table 141. USB 3.0 PHY transceiver supply DC voltage (USB_HV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	-	V	2
Input low voltage	V_{IL}	-	0.8	V	2
Input current (USB_HVIN = 0V or USB_HV_{IN} = USB_HV_{DD})	I_{IN}	-50.0	50.0	µA	3
Output high voltage (USB_HV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.8	-	V	-
Output low voltage (USB_HV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.3	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max USB_HV_{IN} values found in Table 3. 3. The symbol USB_HV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the USB 3.0 transmitter DC electrical characteristics at package pins.

Table 142. USB 3.0 transmitter DC electrical characteristics[1]

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage	$V_{tx\text{-}diff\text{-}pp}$	800.0	1000.0	1200.0	mVp-p
Low power differential output voltage	$V_{tx\text{-}diff\text{-}pp\text{-}low}$	400.0	-	1200.0	mVp-p
Transmit de-emphasis	$V_{tx\text{-}de\text{-}ratio}$	3.0	-	4.0	dB
Differential impedance	Z_{diffTX}	72.0	100.0	120.0	Ω
Transmit common mode impedance	$R_{TX\text{-}DC}$	18.0	-	30.0	Ω
Absolute DC common mode voltage between U1 and U0	$T_{TX\text{-}CM\text{-}DC\text{-}ACTIVEIDLE\text{-}DELTA}$	-	-	200.0	mV
DC electrical idle differential output voltage	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	0.0	-	10.0	mV
1. For recommended operating conditions, see Table 3.					

This table provides the USB 3.0 transmitter DC electrical characteristics at receiver package pins.

Table 143. USB 3.0 receiver DC electrical characteristics[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential receiver input impedance	$R_{RX\text{-}DIFF\text{-}DC}$	72.0	100.0	120.0	Ω	-
Receiver DC common mode impedance	$R_{RX\text{-}DC}$	18.0	-	30.0	Ω	-
DC input CM input impedance for V > 0 during reset or power down	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	25000.0	-	-	Ω	-

Table continues on the next page...

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