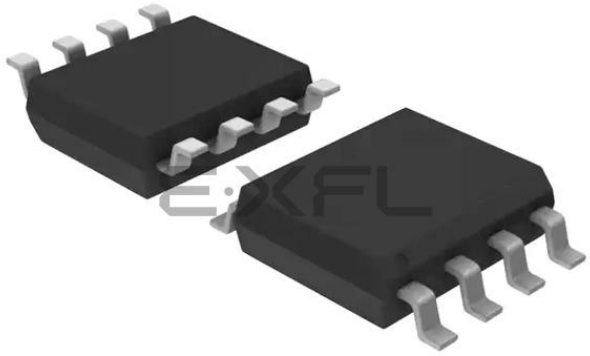

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	240 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 2x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f572kpf-g-sne2

3. Differences Among Products And Notes On Product Selection

- Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.
  For details of current consumption, see “Electrical Characteristics”.

- Package
  For details of information on each package, see “Packages And Corresponding Products” and “Package Dimension”.

- Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of the operating voltage, see “Electrical Characteristics”.

- On-chip debug function
  The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 21 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in “New 8FX MB95560H/570H/580H Series Hardware Manual”.

5. Pin Functions (MB95560H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	C	—	Decoupling capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F562H/F563H/F564H
9	P63	E	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
10	P62	E	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12			
13			
14			
15	P00	D	General-purpose I/O port High-current pin
	AN00		A/D converter analog input pin
16	P64	E	General-purpose I/O port High-current pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
17	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
18	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin

Pin no.	Pin name	I/O circuit type*	Function
19	P03	D	General-purpose I/O port High-current pin
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
20	P04	D	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
21	P05	D	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
22	P06	E	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
23	P12	F	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin
24	P07	E	General-purpose I/O port High-current pin
	INT07		External interrupt input pin
25	NC	—	It is an internally connected pin. Always leave it unconnected.
26			
27			
28			
29			
30			
31			
32			

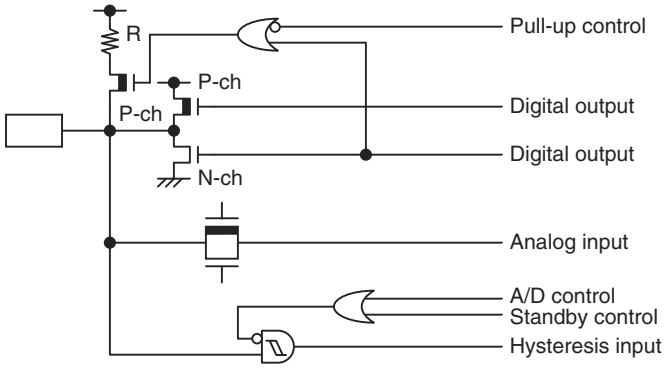
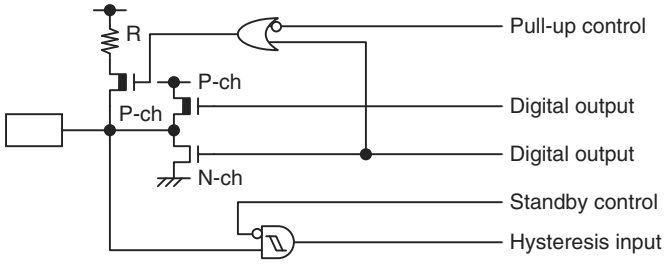
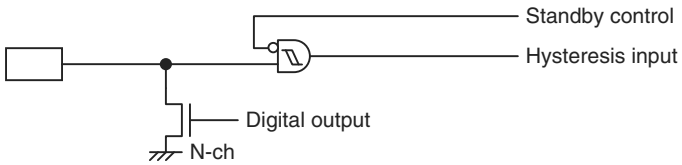
*: For the I/O circuit types, see “I/O Circuit Type”.

6. Pin Functions (MB95560H Series, 20 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	C	—	Decoupling capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F562H/F563H/F564H
9	P62	E	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
10	P63	E	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
11	P64	E	General-purpose I/O port High-current pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
12	P00	D	General-purpose I/O port High-current pin
	AN00		A/D converter analog input pin
13	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
14	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
15	P03	D	General-purpose I/O port High-current pin
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

Pin no.	Pin name	I/O circuit type*	Function
16	P04	D	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
17	P05	D	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
18	P06	E	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
19	P07	E	General-purpose I/O port High-current pin
	INT07		External interrupt input pin
20	P12	F	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see “I/O Circuit Type”.

Type	Circuit	Remarks
D		• CMOS output • Hysteresis input • Pull-up control available • Analog input
E		• CMOS output • Hysteresis input • Pull-up control available
F		• N-ch open drain output • Hysteresis input

11. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

11.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

• Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

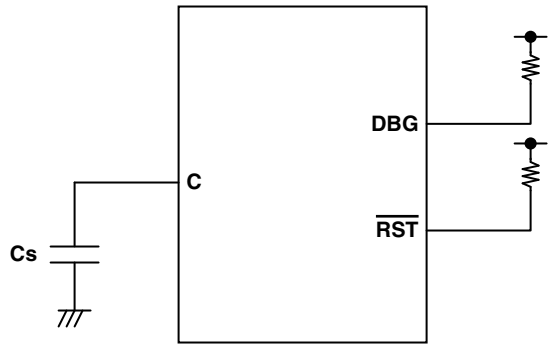
• Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

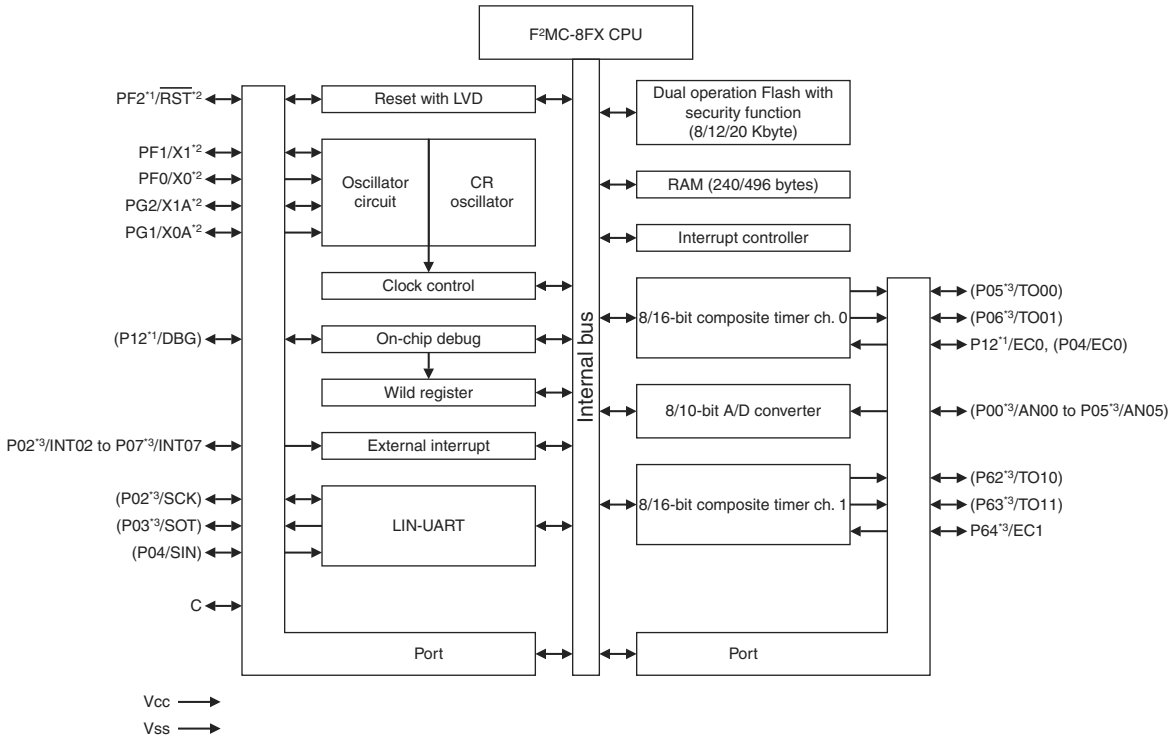
Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- DBG/$\overline{\text{RST}}$/C pins connection diagram



14. Block Diagram (MB95560H Series)



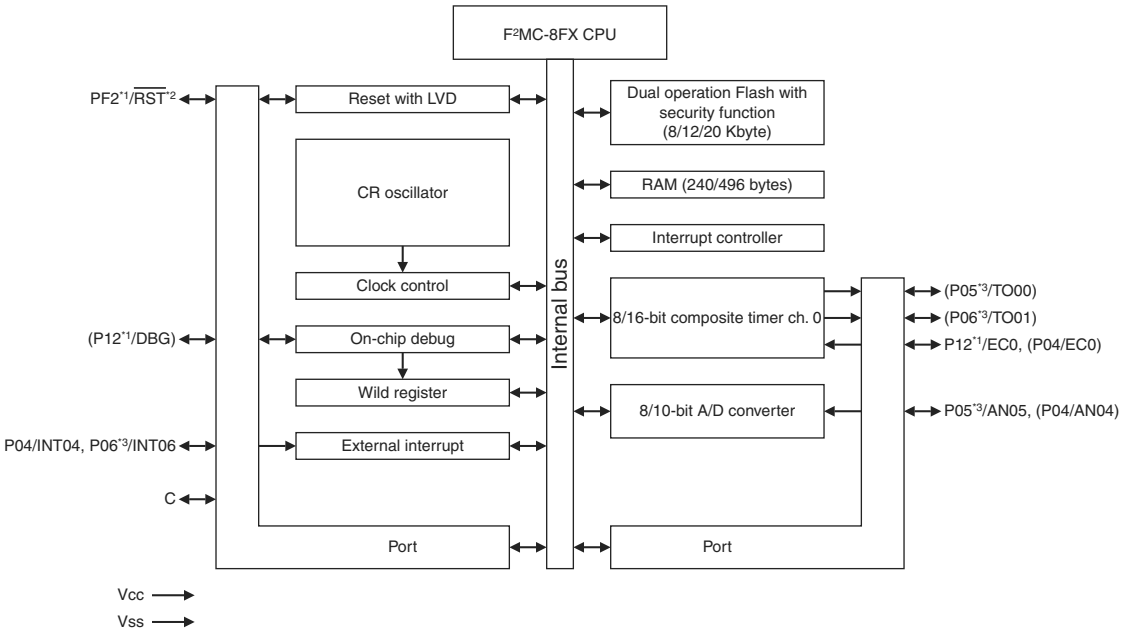
*1: PF2 and P12 are N-ch open drain pins.

*2: Software option

*3: P00 to P03, P05 to P07 and P62 to P64 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

15. Block Diagram (MB95570H Series)



*1: PF2 and P12 are N-ch open drain pins.

*2: Software option

*3: P05 and P06 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

18. I/O Map (MB95560H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000H	PDR0	Port 0 data register	R/W	00000000B
0001H	DDR0	Port 0 direction register	R/W	00000000B
0002H	PDR1	Port 1 data register	R/W	00000000B
0003H	DDR1	Port 1 direction register	R/W	00000000B
0004H	—	(Disabled)	—	—
0005H	WATR	Oscillation stabilization wait time setting register	R/W	11111111B
0006H	PLLC	PLL control register	R/W	000X0000B
0007H	SYCC	System clock control register	R/W	XXX11011B
0008H	STBC	Standby control register	R/W	00000000B
0009H	RSRR	Reset source register	R/W	000XXXXXB
000AH	TBTC	Time-base timer control register	R/W	00000000B
000BH	WPCR	Watch prescaler control register	R/W	00000000B
000CH	WDTC	Watchdog timer control register	R/W	00XX0000B
000DH	SYCC2	System clock control register 2	R/W	XXXX0011B
000EH	STBC2	Standby control register 2	R/W	00000000B
000FH to 0015H	—	(Disabled)	—	—
0016H	PDR6	Port 6 data register	R/W	00000000B
0017H	DDR6	Port 6 direction register	R/W	00000000B
0018H to 0027H	—	(Disabled)	—	—
0028H	PDRF	Port F data register	R/W	00000000B
0029H	DDRF	Port F direction register	R/W	00000000B
002AH	PDRG	Port G data register	R/W	00000000B
002BH	DDRG	Port G direction register	R/W	00000000B
002CH	PUL0	Port 0 pull-up register	R/W	00000000B
002DH to 0032H	—	(Disabled)	—	—
0033H	PUL6	Port 6 pull-up register	R/W	00000000B
0034H	—	(Disabled)	—	—
0035H	PULG	Port G pull-up register	R/W	00000000B
0036H	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000B
0037H	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000B
0038H	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	00000000B
0039H	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	00000000B
003AH to 0048H	—	(Disabled)	—	—

Address	Register abbreviation	Register name	R/W	Initial value
006C$_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000$_B$
006D$_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000$_B$
006E$_H$	ADDH	8/10-bit A/D converter data register (upper)	R/W	00000000$_B$
006F$_H$	ADDL	8/10-bit A/D converter data register (lower)	R/W	00000000$_B$
0070$_H$	—	(Disabled)	—	—
0071$_H$	FSR2	Flash memory status register 2	R/W	00000000$_B$
0072$_H$	FSR	Flash memory status register	R/W	000X0000$_B$
0073$_H$	SWRE0	Flash memory sector write control register 0	R/W	00000000$_B$
0074$_H$	FSR3	Flash memory status register 3	R	000XXXXX$_B$
0075$_H$	FSR4	Flash memory status register 4	R/W	00000000$_B$
0076$_H$	WREN	Wild register address compare enable register	R/W	00000000$_B$
0077$_H$	WROR	Wild register data test setting register	R/W	00000000$_B$
0078$_H$	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079$_H$	ILR0	Interrupt level setting register 0	R/W	11111111$_B$
007A$_H$	ILR1	Interrupt level setting register 1	R/W	11111111$_B$
007B$_H$, 007C$_H$	—	(Disabled)	—	—
007D$_H$	ILR4	Interrupt level setting register 4	R/W	11111111$_B$
007E$_H$	ILR5	Interrupt level setting register 5	R/W	11111111$_B$
007F$_H$	—	(Disabled)	—	—
0F80$_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000$_B$
0F81$_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000$_B$
0F82$_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000$_B$
0F83$_H$	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000$_B$
0F84$_H$	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000$_B$
0F85$_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000$_B$
0F86$_H$	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000$_B$
0F87$_H$	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000$_B$
0F88$_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000$_B$
0F89$_H$ to 0F91$_H$	—	(Disabled)	—	—
0F92$_H$	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	00000000$_B$
0F93$_H$	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	00000000$_B$
0F94$_H$	T01DR	8/16-bit composite timer 01 data register	R/W	00000000$_B$
0F95$_H$	T00DR	8/16-bit composite timer 00 data register	R/W	00000000$_B$
0F96$_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	00000000$_B$
0F97$_H$ to 0FC2$_H$	—	(Disabled)	—	—

24.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

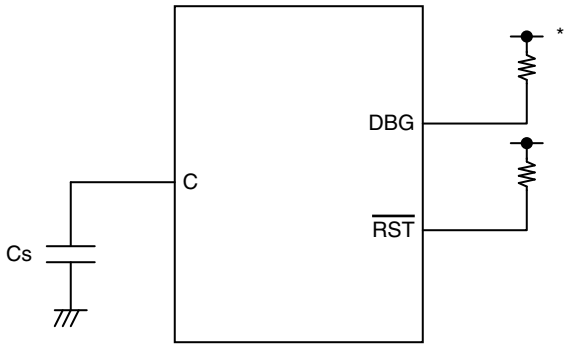
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1, *2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Decoupling capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	−40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The minimum power supply voltage becomes 2.88 V when a product with the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

• DBG / $\overline{\text{RST}}$ / C pins connection diagram



*: Connect the DBG pin to an external pull-up resistor of 2 kΩ or above. After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*2		
Power supply current*5	I_{LVD}	V_{CC}	Current consumption for the low-voltage detection circuit	—	3.6	6.6	µA	
	I_{CRH}		Current consumption for the main CR oscillator	—	220	280	µA	
	I_{CRL}		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	5.1	9.3	µA	
	I_{NSTBY}		Current consumption difference between normal standby mode and deep standby mode T_A = +25 °C	—	20	30	µA	

*1: V_{CC} = 5.0 V, T_A = + 25 °C

*2: V_{CC} = 5.5 V, T_A = + 85 °C (unless otherwise specified)

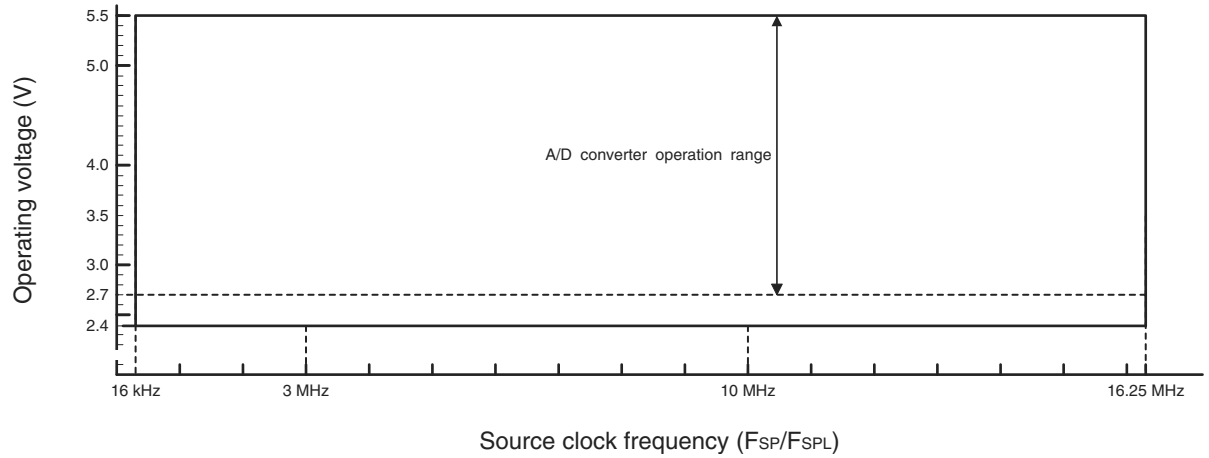
*3: P00, P62, P63 and P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

*4: P01, P02, P03, P07, PF0, PF1, PG1 and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.

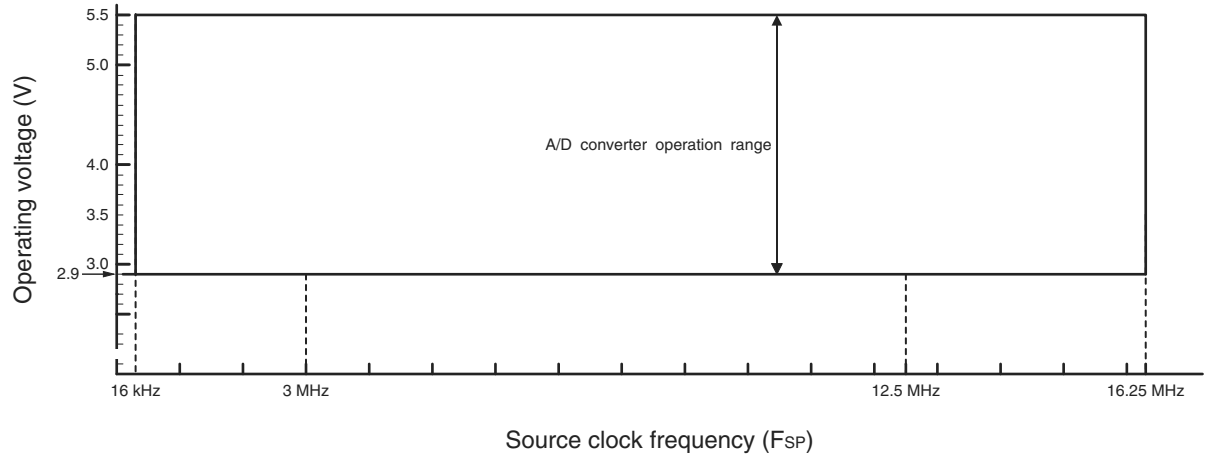
*5:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See “24.4 AC Characteristics: Clock Timing” for F_{CH} and F_{CL}.
- See “24.4 AC Characteristics: Source Clock / Machine Clock” for F_{MP} and F_{MPL}.

*6: In sub-CR clock mode, the power supply current value is the sum of adding I_{CRL} to I_{CCLS} or I_{CCT}. In addition, when the sub-CR clock mode is selected with F_{MPL} being 50 kHz, the current consumption increases accordingly.

- Operating voltage - Operating frequency (T_A = −40°C to +85°C)
  Without the on-chip debug function



- Operating voltage - Operating frequency (T_A = −40 °C to +85 °C)
  With the on-chip debug function

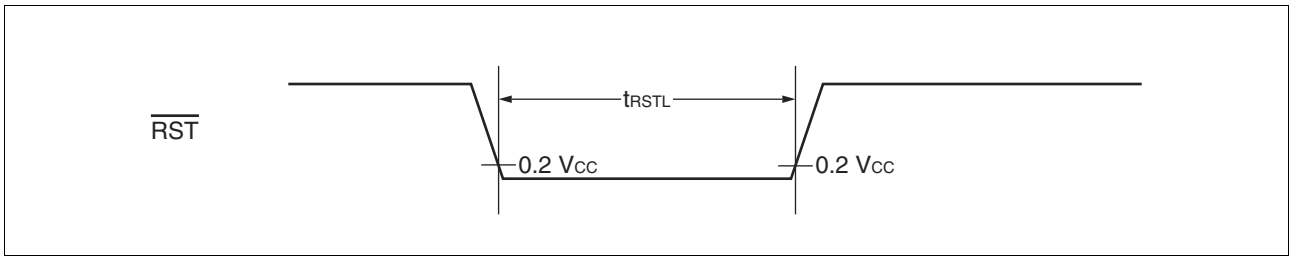


24.4.3 External Reset

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation

*1: See "Source Clock / Machine Clock" for t_{MCLK}.



24.5 A/D Converter

24.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

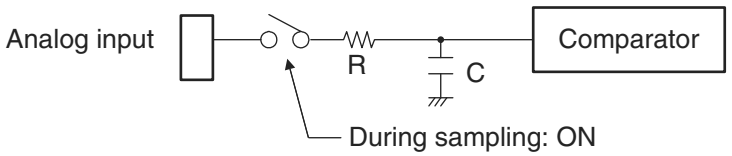
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		−3	—	+3	LSB	
Linearity error		−2.5	—	+2.5	LSB	
Differential linearity error		−1.9	—	+1.9	LSB	
Zero transition voltage	V_{0T}	V_{SS} − 1.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} − 4.5 LSB	V_{CC} − 2 LSB	V_{CC} + 0.5 LSB	V	
Compare time	—	1	—	10	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		3	—	10	µs	2.7 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	2.7 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 3.3 kΩ
Analog input current	I_{AIN}	−0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

24.5.2 Notes on Using A/D Converter

- External impedance of analog input and its sampling time

  The A/D converter of the MB95560H/570H/580H Series has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

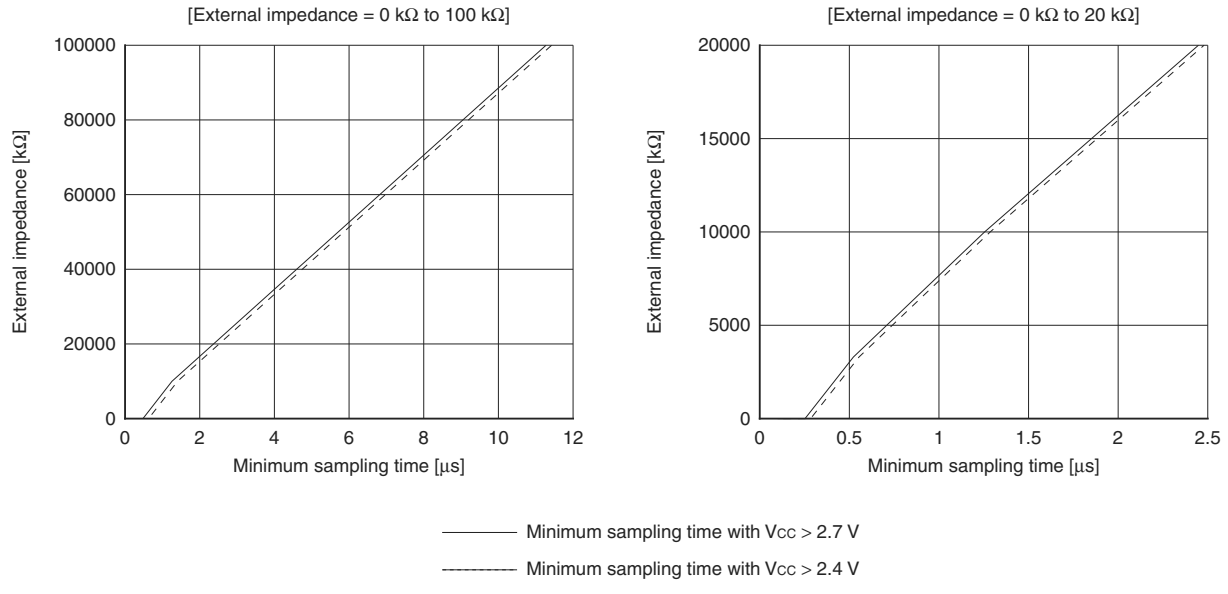
- Analog input equivalent circuit



V_{CC}	R	C
4.5 V ≤ V_{CC} ≤ 5.5 V	1.45 kΩ (Max)	14.89 pF (Max)
2.7 V ≤ V_{CC} < 4.5 V	2.7 kΩ (Max)	14.89 pF (Max)

Note: The values are reference values.

- Relationship between external impedance and minimum sampling time

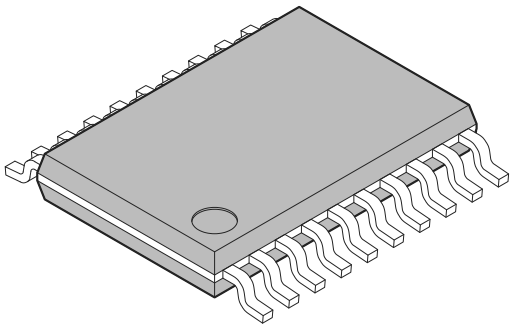


- A/D conversion error

  As |V_{CC} – V_{SS}| decreases, the A/D conversion error increases proportionately.

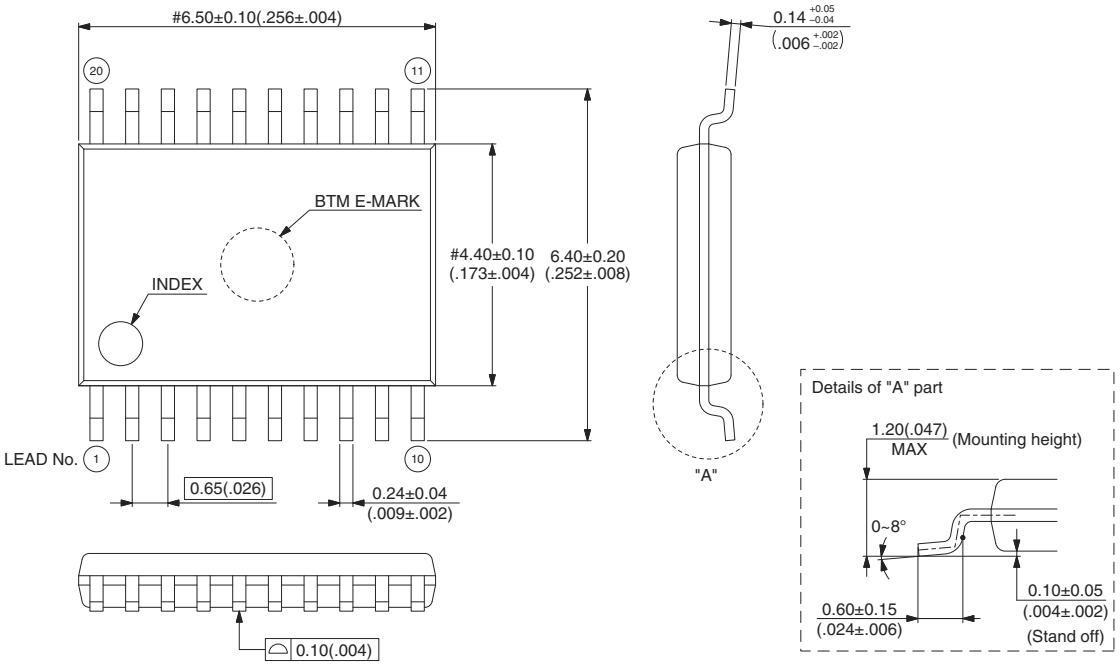
26. Mask Options

No.	Part Number	MB95F562H MB95F563H MB95F564H MB95F572H MB95F573H MB95F574H MB95F582H MB95F583H MB95F584H	MB95F562K MB95F563K MB95F564K MB95F572K MB95F573K MB95F574K MB95F582K MB95F583K MB95F584K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

20-pin plastic TSSOP		
	Lead pitch	0.65 mm
	Package width × package length	4.40 mm × 6.50 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.08 g
(FPT-20P-M10)		

20-pin plastic TSSOP
(FPT-20P-M10)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

29. Major Changes In This Edition

Spansion Publication Number: DS702-00010-5v0-E

Page	Section	Details
—	—	Changed the series name. MB95560H Series → MB95560H/570H/580H Series
		Added information on the MB95570H Series.
		Added information on the MB95580H Series.
27	■ PIN CONNECTION • DBG pin	Revised details of "• DBG pin".
	• $\overline{\text{RST}}$ pin	Revised details of "• $\overline{\text{RST}}$ pin".
28	• C pin	Corrected the following statement. The decoupling capacitor for the V_{CC} pin must have a capacitance larger than C_S. → The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S.
39	■ I/O MAP (MB95570H Series)	Corrected the R/W attribute of the CMDR register. R/W → R
		Corrected the R/W attribute of the WDTH register. R/W → R
		Corrected the R/W attribute of the WDTL register. R/W → R
42	■ I/O MAP (MB95580H Series)	Corrected the R/W attribute of the CMDR register. R/W → R
		Corrected the R/W attribute of the WDTH register. R/W → R
		Corrected the R/W attribute of the WDTL register. R/W → R
46	■ ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Corrected the rating of the parameter ""L" level total maximum output current". 48 → 100
		Corrected the rating of the parameter ""H" level total maximum output current". 48 → −100

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