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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	240 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 5x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f582kpf-g-sne2

Parameter \ Part number	MB95F562H	MB95F563H	MB95F564H	MB95F562K	MB95F563K	MB95F564K
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Flash security feature for protecting the content of the Flash memory Number of program/erase cycles: 1000 / 10000 / 100000 Data retention time: 20 years / 10 years / 5 years					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	LCC-32P-M19 FPT-20P-M09 FPT-20P-M10					

• MB95570H Series

Parameter \ Part number	MB95F572H	MB95F573H	MB95F574H	MB95F572K	MB95F573K	MB95F574K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 4 • CMOS I/O : 3 • N-ch open drain: 1			• I/O ports (Max) : 5 • CMOS I/O : 3 • N-ch open drain: 2		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace 3 bytes of data.					
LIN-UART	No LIN-UART					
8/10-bit A/D converter	2 channels					
	8-bit or 10-bit resolution can be selected.					

Part number / Parameter	MB95F572H	MB95F573H	MB95F574H	MB95F572K	MB95F573K	MB95F574K
8/16-bit composite timer	1 channel • The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (7 types) and external clocks. • It can output square wave.					
External interrupt	2 channels • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Flash security feature for protecting the content of the Flash memory Number of program/erase cycles: 1000 / 10000 / 100000 Data retention time: 20 years / 10 years / 5 years					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	DIP-8P-M03 FPT-8P-M08					

• MB95580H Series

Part number / Parameter	MB95F582H	MB95F583H	MB95F584H	MB95F582K	MB95F583K	MB95F584K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 12 • CMOS I/O : 11 • N-ch open drain: 1			• I/O ports (Max) : 13 • CMOS I/O : 11 • N-ch open drain: 2		

<table>
<tr><th>Part number
Parameter</th><th>MB95F582H</th><th>MB95F583H</th><th>MB95F584H</th><th>MB95F582K</th><th>MB95F583K</th><th>MB95F584K</th></tr>
<tr><td>Time-base timer</td><td colspan="6">Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)</td></tr>
<tr><td>Hardware/ software watchdog timer</td><td colspan="6">• Reset generation cycle
Main oscillation clock at 10 MHz: 105 ms (Min)
• The sub-CR clock can be used as the source clock of the hardware watchdog timer.</td></tr>
<tr><td>Wild register</td><td colspan="6">It can be used to replace 3 bytes of data.</td></tr>
<tr><td>LIN-UART</td><td colspan="6">• A wide range of communication speed can be selected by a dedicated reload timer.
• It has a full duplex double buffer.
• Both clock synchronous serial data transfer and clock asynchronous serial data transfer are enabled.
• The LIN function can be used as a LIN master or a LIN slave.</td></tr>
<tr><td rowspan="2">8/10-bit A/D converter</td><td colspan="6">5 channels</td></tr>
<tr><td colspan="6">8-bit or 10-bit resolution can be selected.</td></tr>
<tr><td rowspan="2">8/16-bit composite timer</td><td colspan="6">1 channel</td></tr>
<tr><td colspan="6">• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel".
• It has the following functions: interval timer function, PWC function, PWM function and input capture function.
• Count clock: it can be selected from internal clocks (7 types) and external clocks.
• It can output square wave.</td></tr>
<tr><td rowspan="2">External interrupt</td><td colspan="6">6 channels</td></tr>
<tr><td colspan="6">• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.)
• It can be used to wake up the device from the standby mode.</td></tr>
<tr><td>On-chip debug</td><td colspan="6">• 1-wire serial control
• It supports serial writing (asynchronous mode).</td></tr>
<tr><td>Watch prescaler</td><td colspan="6">Eight different time intervals can be selected.</td></tr>
<tr><td>Flash memory</td><td colspan="6">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table>
<tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr>
<tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr>
</table></td></tr>
<tr><td>Standby mode</td><td colspan="6">Sleep mode, stop mode, watch mode, time-base timer mode</td></tr>
<tr><td>Package</td><td colspan="6">LCC-32P-M19
FPT-16P-M08
FPT-16P-M23</td></tr>
</table>

2. Packages And Corresponding Products

- MB95560H Series

Part number / Package	MB95F562H	MB95F562K	MB95F563H	MB95F563K	MB95F564H	MB95F564K
LCC-32P-M19	O	O	O	O	O	O
FPT-20P-M09	O	O	O	O	O	O
FPT-20P-M10	O	O	O	O	O	O
FPT-16P-M08	X	X	X	X	X	X
FPT-16P-M23	X	X	X	X	X	X
DIP-8P-M03	X	X	X	X	X	X
FPT-8P-M08	X	X	X	X	X	X

- MB95570H Series

Part number / Package	MB95F572H	MB95F572K	MB95F573H	MB95F573K	MB95F574H	MB95F574K
LCC-32P-M19	X	X	X	X	X	X
FPT-20P-M09	X	X	X	X	X	X
FPT-20P-M10	X	X	X	X	X	X
FPT-16P-M08	X	X	X	X	X	X
FPT-16P-M23	X	X	X	X	X	X
DIP-8P-M03	O	O	O	O	O	O
FPT-8P-M08	O	O	O	O	O	O

- MB95580H Series

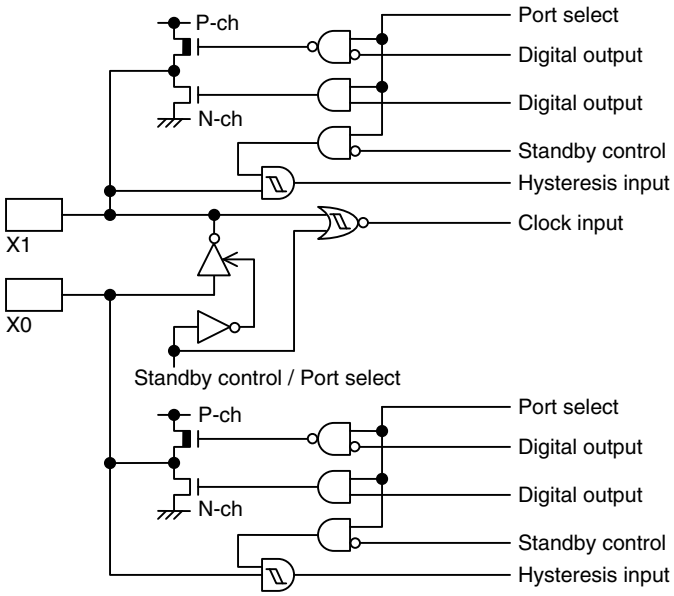
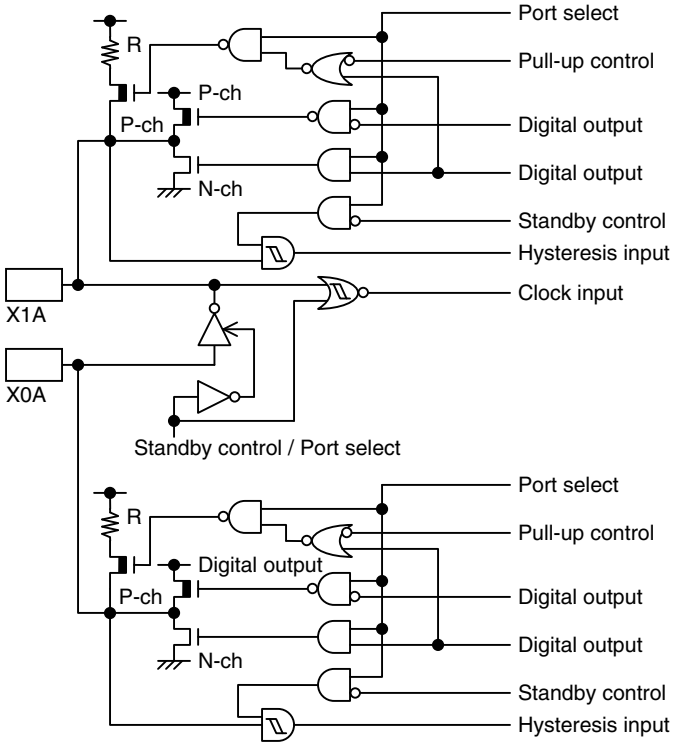
Part number / Package	MB95F582H	MB95F582K	MB95F583H	MB95F583K	MB95F584H	MB95F584K
LCC-32P-M19	O	O	O	O	O	O
FPT-20P-M09	X	X	X	X	X	X
FPT-20P-M10	X	X	X	X	X	X
FPT-16P-M08	O	O	O	O	O	O
FPT-16P-M23	O	O	O	O	O	O
DIP-8P-M03	X	X	X	X	X	X
FPT-8P-M08	X	X	X	X	X	X

O: Available
X: Unavailable

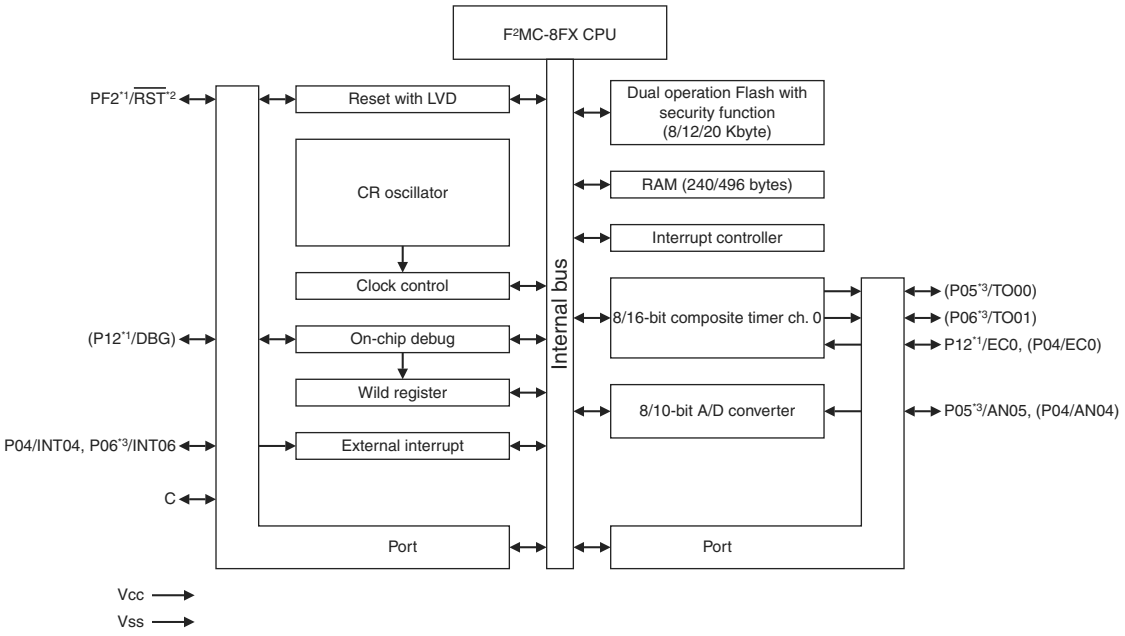
8. Pin Functions (MB95580H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	C	—	Decoupling capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F582H/F583H/F584H
9	NC	—	It is an internally connected pin. Always leave it unconnected.
10			
11			
12			
13			
14			
15			
16			
17	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
18	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	D	General-purpose I/O port High-current pin
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

10. I/O Circuit Type

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx.10 MΩ • CMOS output • Hysteresis input • Pull-up control available

15. Block Diagram (MB95570H Series)



*1: PF2 and P12 are N-ch open drain pins.

*2: Software option

*3: P05 and P06 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

23. Interrupt Source Table (MB95580H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	FFFA$_H$	FFFB$_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ01	FFF8$_H$	FFF9$_H$	L01 [1:0]	
External interrupt ch. 2	IRQ02	FFF6$_H$	FFF7$_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4$_H$	FFF5$_H$	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	FFF2$_H$	FFF3$_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0$_H$	FFF1$_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE$_H$	FFEF$_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFEC$_H$	FFED$_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEA$_H$	FFEB$_H$	L08 [1:0]	
—	IRQ09	FFE8$_H$	FFE9$_H$	L09 [1:0]	
—	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1:0]	
—	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1:0]	
—	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1:0]	
—	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1:0]	
—	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1:0]	
—	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1:0]	
—	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1:0]	
—	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1:0]	
Time-base timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1:0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1:0]	
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1:0]	
—	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1:0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1:0]	Low

24.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

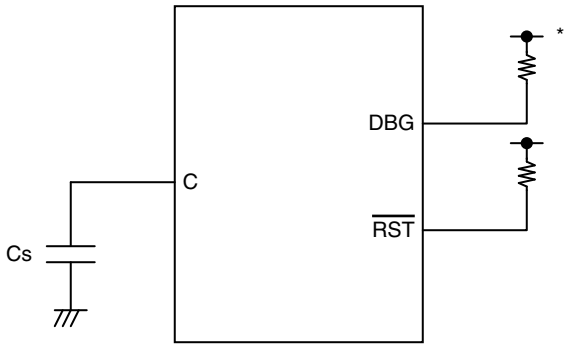
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1, *2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Decoupling capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	−40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The minimum power supply voltage becomes 2.88 V when a product with the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

• DBG / $\overline{\text{RST}}$ / C pins connection diagram



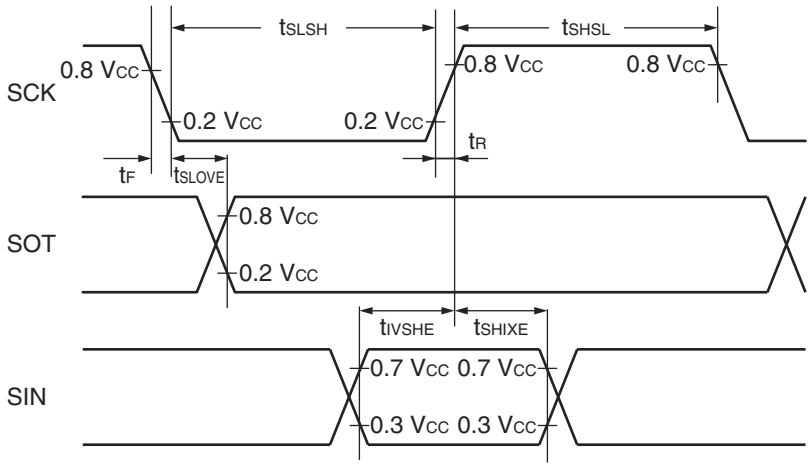
*: Connect the DBG pin to an external pull-up resistor of 2 kΩ or above. After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

• External shift clock mode



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2. (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

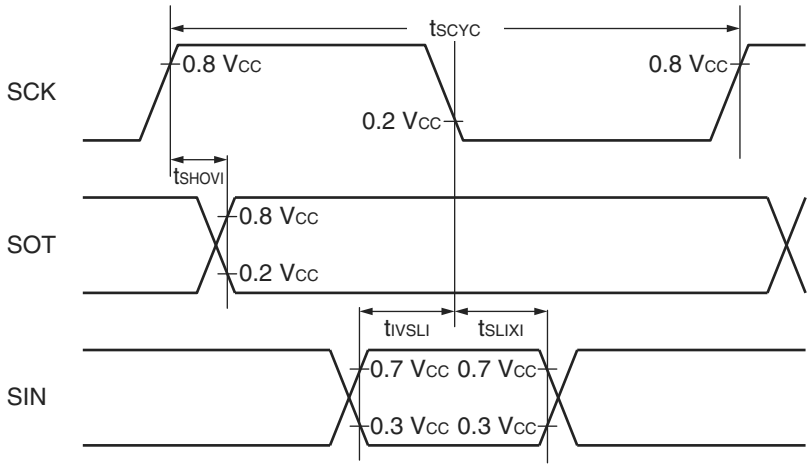
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 – t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 10	—	ns
SCK ↑→ SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		30	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

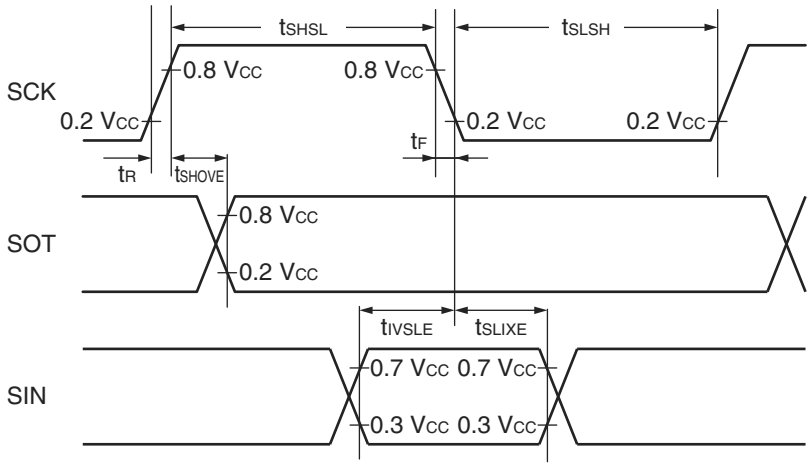
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “Source Clock / Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2. (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

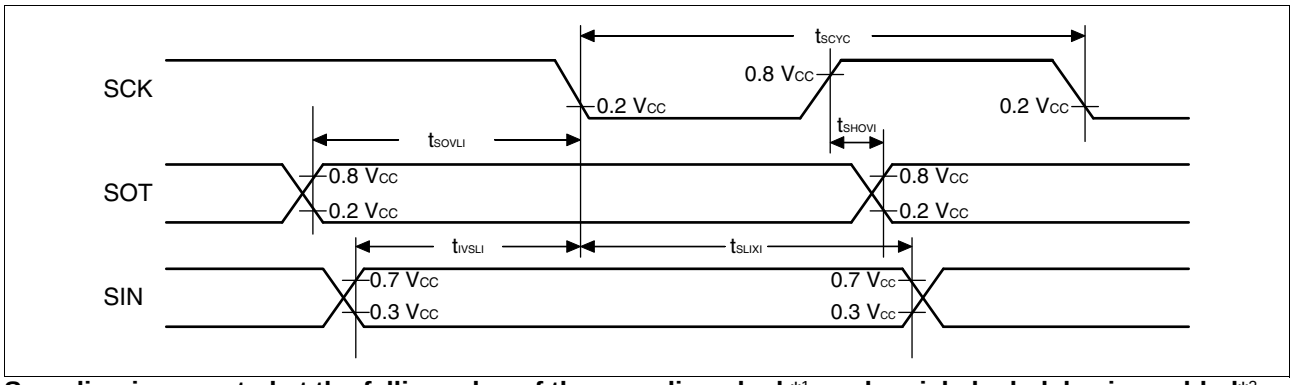
(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		3 t_{MCLK}*3 – 70	—	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “Source Clock / Machine Clock” for t_{MCLK}.



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2. (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operating output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		3 t_{MCLK}*3 – 70	—	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “Source Clock / Machine Clock” for t_{MCLK}.

24.5 A/D Converter

24.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		−3	—	+3	LSB	
Linearity error		−2.5	—	+2.5	LSB	
Differential linearity error		−1.9	—	+1.9	LSB	
Zero transition voltage	V_{0T}	V_{SS} − 1.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} − 4.5 LSB	V_{CC} − 2 LSB	V_{CC} + 0.5 LSB	V	
Compare time	—	1	—	10	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		3	—	10	µs	2.7 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	2.7 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 3.3 kΩ
Analog input current	I_{AIN}	−0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

24.6 Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.3*1	1.6*2	s	The time of writing 00_H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.6*1	3.1*2	s	The time of writing 00_H prior to erasure is excluded.
Byte writing time	—	17	272	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	2.4	—	5.5	V	
Flash memory data retention time	5*3	—	—	year	Average T_A = +85 °C

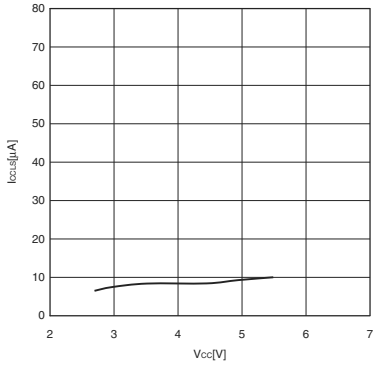
*1: V_{CC} = 5.5 V, T_A = +25 °C, 0 cycle

*2: V_{CC} = 2.4 V, T_A = +85 °C, 100000 cycles

*3: This value was converted from the result of a technology reliability assessment. (The value was converted from the result of a high temperature accelerated test using the Arrhenius equation with an average temperature of +85 °C).

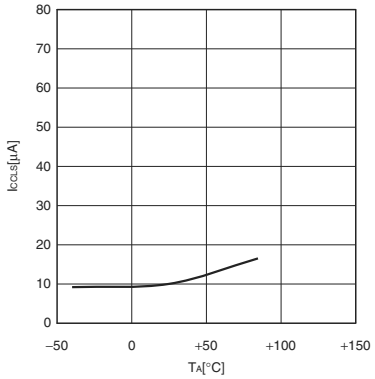
I_{CCLS} – V_{CC}

T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



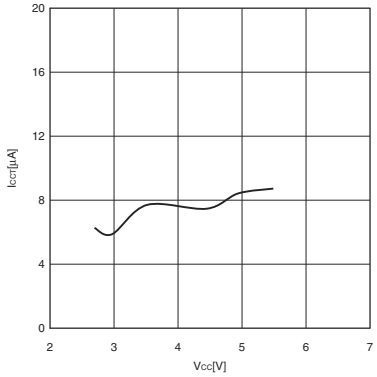
I_{CCLS} – T_A

V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



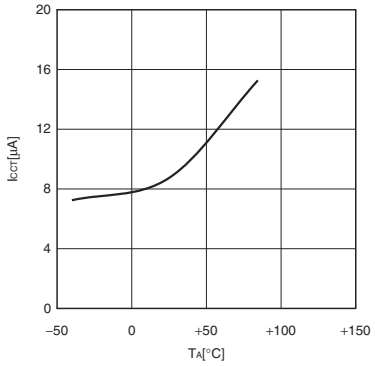
I_{CCT} – V_{CC}

T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



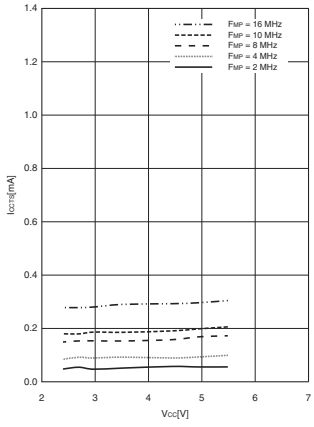
I_{CCT} – T_A

V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



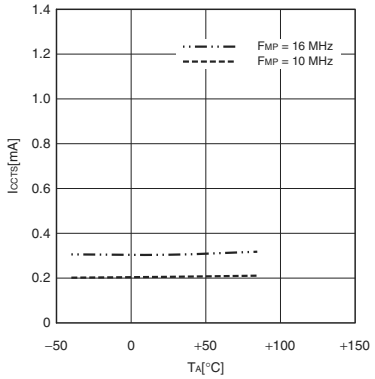
I_{CCTS} – V_{CC}

T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



I_{CCTS} – T_A

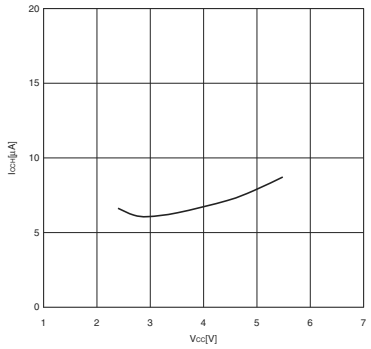
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



I_{CCH} – V_{CC}

T_A = +25 °C, F_{MPL} = (stop)

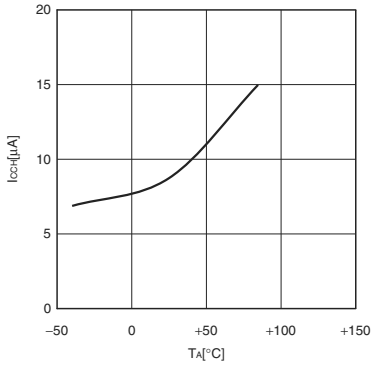
Substop mode with the external clock stopping



I_{CCH} – T_A

V_{CC} = 5.5 V, F_{MPL} = (stop)

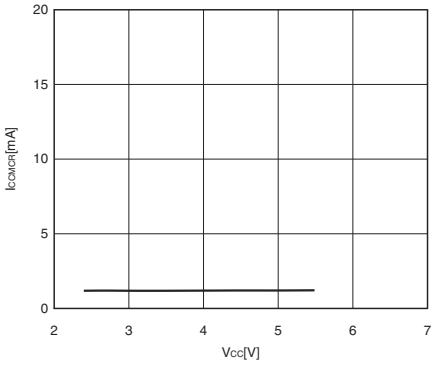
Substop mode with the external clock stopping



I_{CCMCR} – V_{CC}

T_A = +25 °C, F_{MP} = 4 MHz (no division)

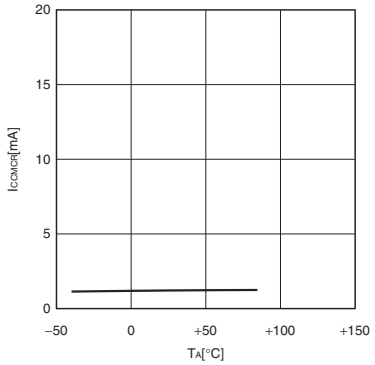
Main clock mode with the main CR clock operating



I_{CCMCR} – T_A

V_{CC} = 5.5 V, F_{MP} = 4 MHz (no division)

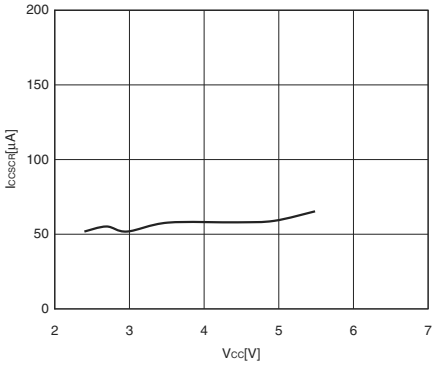
Main clock mode with the main CR clock operating



I_{CCSCR} – V_{CC}

T_A = +25 °C, F_{MPL} = 50 kHz (divided by 2)

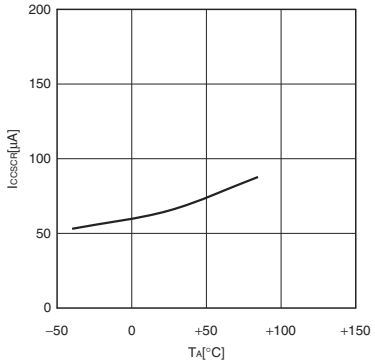
Subclock mode with the sub-CR clock operating



I_{CCSCR} – T_A

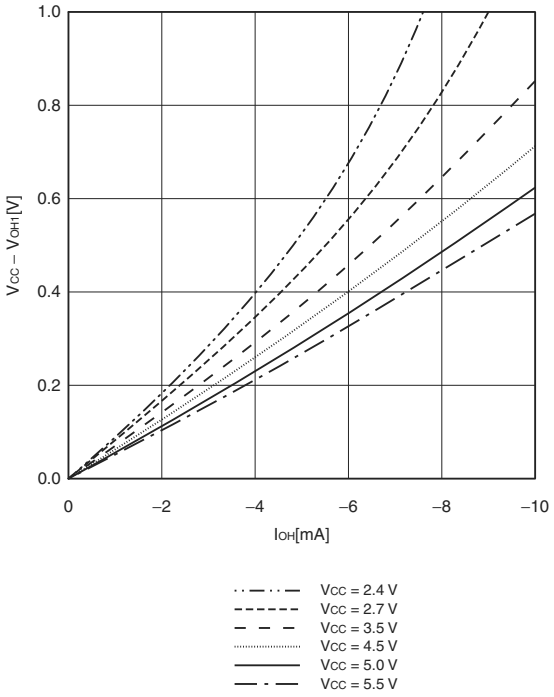
V_{CC} = 5.5 V, F_{MPL} = 50 kHz (divided by 2)

Subclock mode with the sub-CR clock operating

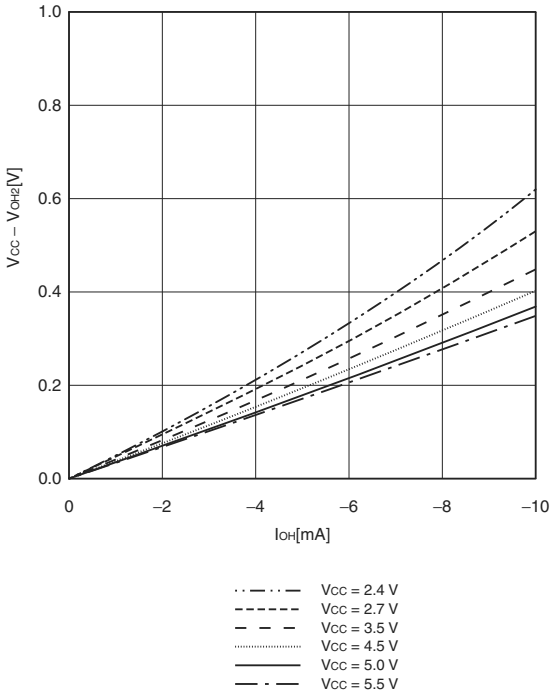


- Output voltage characteristics

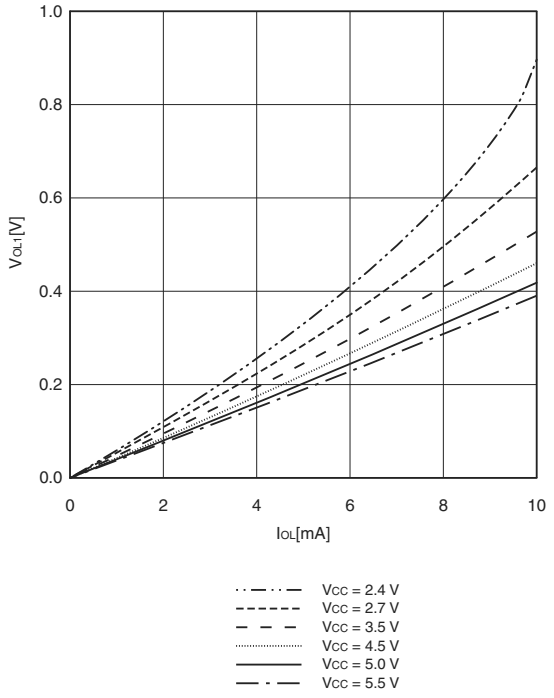
$(V_{CC} - V_{OH1}) - I_{OH}$
$T_A = +25\ °C$



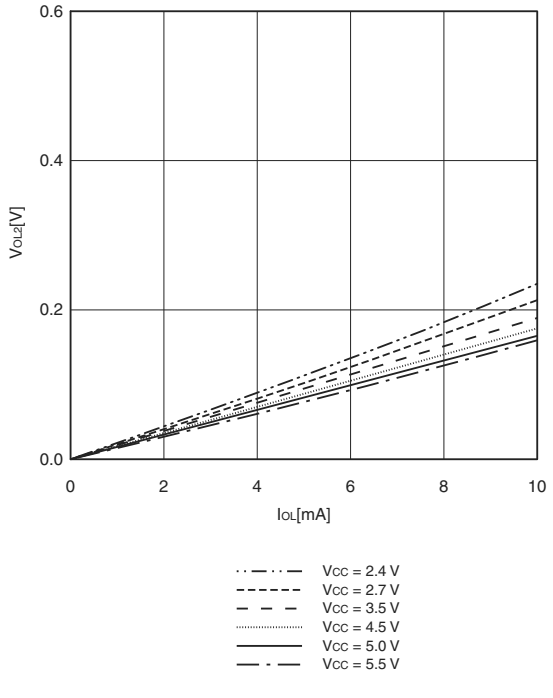
$(V_{CC} - V_{OH2}) - I_{OH}$
$T_A = +25\ °C$



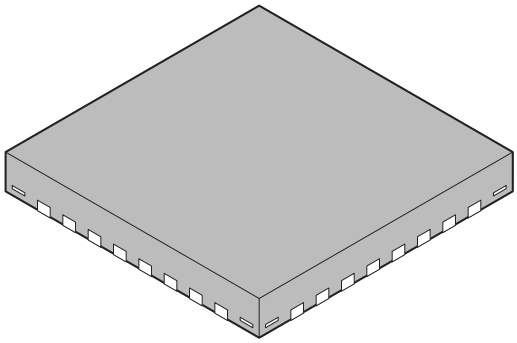
$V_{OL1} - I_{OL}$
$T_A = +25\ °C$



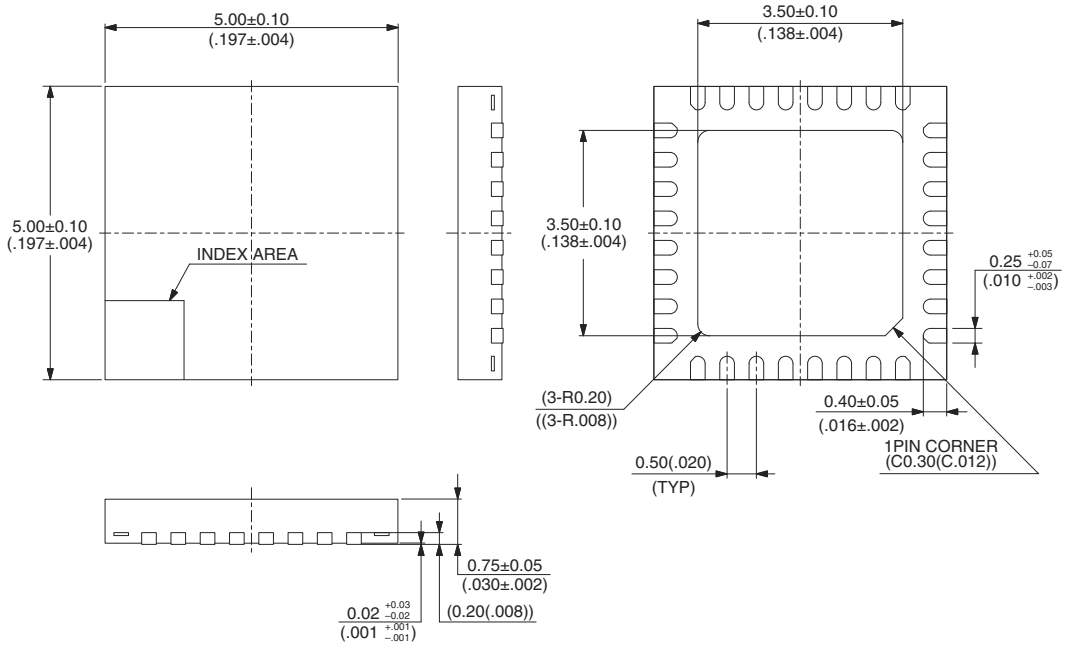
$V_{OL2} - I_{OL}$
$T_A = +25\ °C$



28. Package Dimension

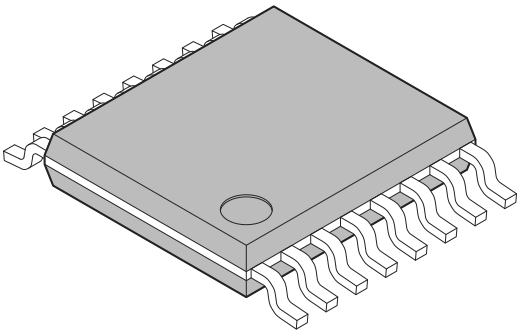
32-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	5.00 mm × 5.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.06 g
(LCC-32P-M19)		

32-pin plastic QFN
(LCC-32P-M19)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

16-pin plastic TSSOP

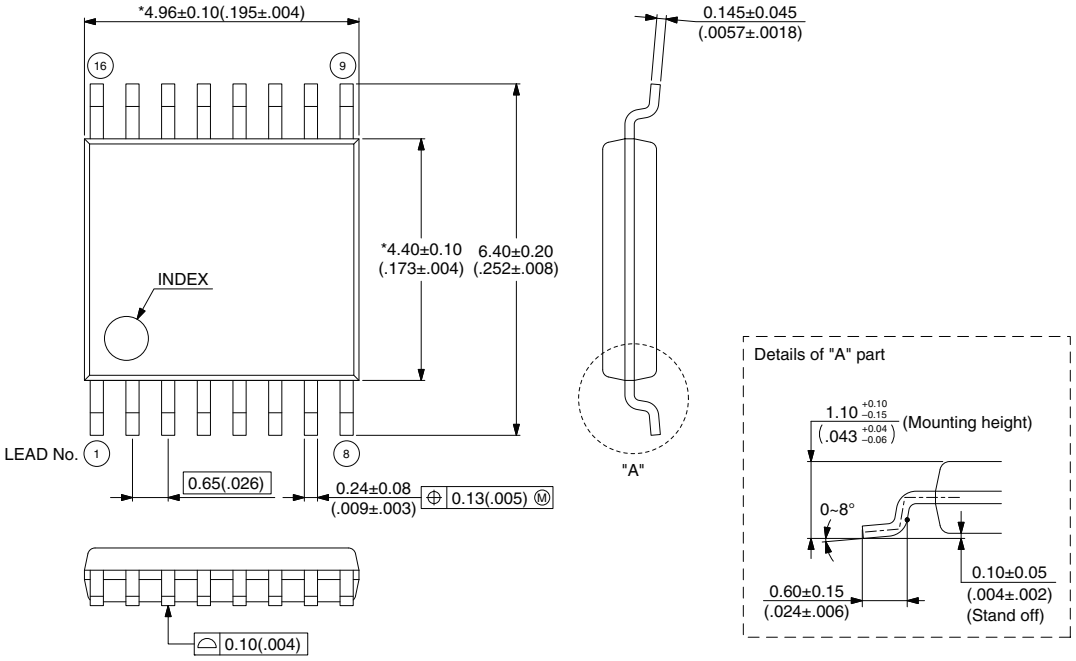


(FPT-16P-M08)

Lead pitch	0.65 mm
Package width × package length	4.40 mm × 4.96 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.20 mm Max
Weight	0.06 g

16-pin plastic TSSOP
(FPT-16P-M08)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) * : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

29. Major Changes In This Edition

Spansion Publication Number: DS702-00010-5v0-E

Page	Section	Details
—	—	Changed the series name. MB95560H Series → MB95560H/570H/580H Series
		Added information on the MB95570H Series.
		Added information on the MB95580H Series.
27	■ PIN CONNECTION • DBG pin	Revised details of "• DBG pin".
	• $\overline{\text{RST}}$ pin	Revised details of "• $\overline{\text{RST}}$ pin".
28	• C pin	Corrected the following statement. The decoupling capacitor for the V_{CC} pin must have a capacitance larger than C_S. → The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S.
39	■ I/O MAP (MB95570H Series)	Corrected the R/W attribute of the CMDR register. R/W → R
		Corrected the R/W attribute of the WDTH register. R/W → R
		Corrected the R/W attribute of the WDTL register. R/W → R
42	■ I/O MAP (MB95580H Series)	Corrected the R/W attribute of the CMDR register. R/W → R
		Corrected the R/W attribute of the WDTH register. R/W → R
		Corrected the R/W attribute of the WDTL register. R/W → R
46	■ ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Corrected the rating of the parameter ""L" level total maximum output current". 48 → 100
		Corrected the rating of the parameter ""H" level total maximum output current". 48 → −100