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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	240 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 5x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f582kpft-g-sne2

Part number / Parameter	MB95F572H	MB95F573H	MB95F574H	MB95F572K	MB95F573K	MB95F574K
8/16-bit composite timer	1 channel • The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (7 types) and external clocks. • It can output square wave.					
External interrupt	2 channels • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Flash security feature for protecting the content of the Flash memory Number of program/erase cycles: 1000 / 10000 / 100000 Data retention time: 20 years / 10 years / 5 years					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	DIP-8P-M03 FPT-8P-M08					

• MB95580H Series

Part number / Parameter	MB95F582H	MB95F583H	MB95F584H	MB95F582K	MB95F583K	MB95F584K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 12 • CMOS I/O : 11 • N-ch open drain: 1			• I/O ports (Max) : 13 • CMOS I/O : 11 • N-ch open drain: 2		

5. Pin Functions (MB95560H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	C	—	Decoupling capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F562H/F563H/F564H
9	P63	E	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
10	P62	E	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12			
13			
14			
15	P00	D	General-purpose I/O port High-current pin
	AN00		A/D converter analog input pin
16	P64	E	General-purpose I/O port High-current pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
17	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
18	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin

9. Pin Functions (MB95580H Series, 16 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F582H/F583H/F584H
8	C	—	Decoupling capacitor connection pin
9	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
10	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
11	P03	D	General-purpose I/O port High-current pin
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
12	P04	D	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin

Supply voltage must be stabilized.
A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.
As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

- Notes on using the external clock
  When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

13. Pin Connection

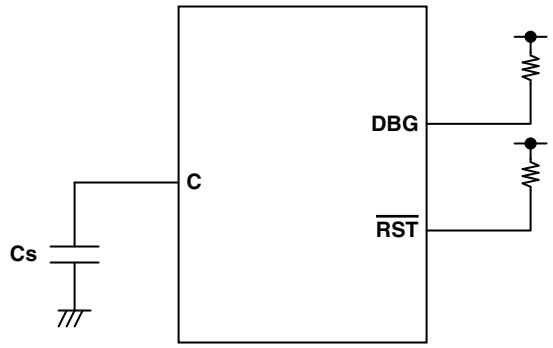
- Treatment of unused pins
  If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

- Power supply pins
  To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.
  It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a decoupling capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

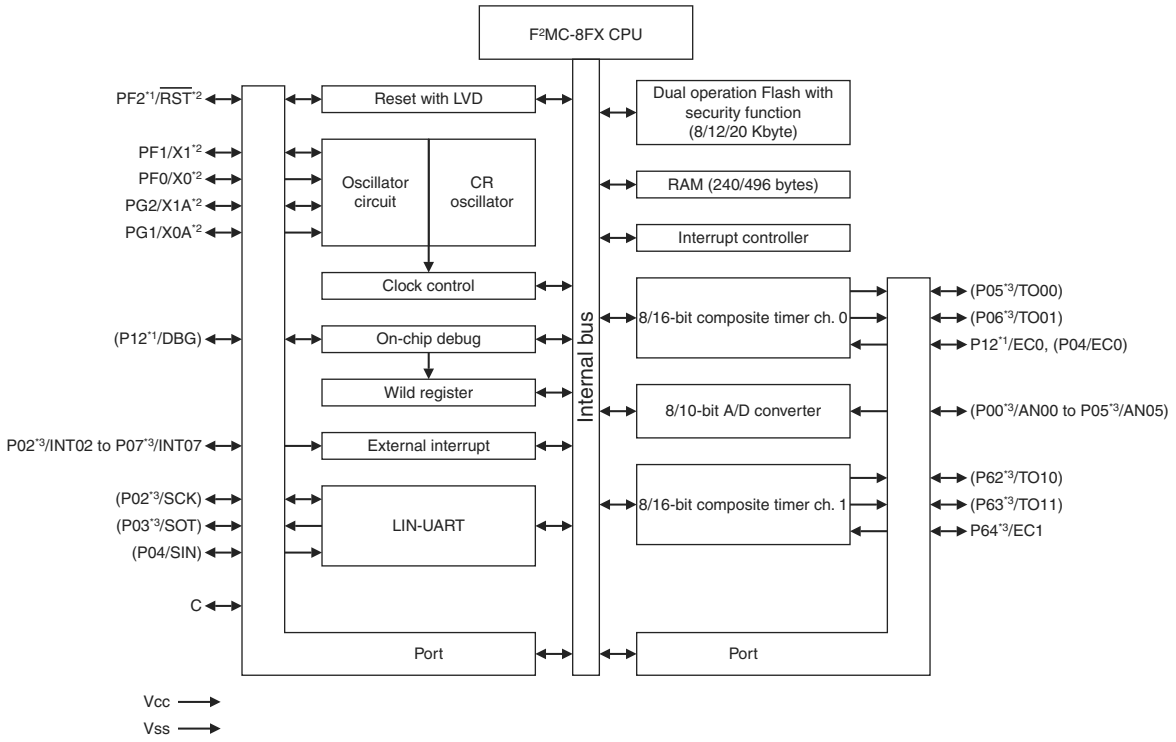
- DBG pin
  Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.
  After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released.
  The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

- $\overline{\text{RST}}$ pin
  Connect the $\overline{\text{RST}}$ pin to an external pull-up resistor of 2 kΩ or above.
  To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{\text{RST}}$ pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.
  The PF2/$\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{\text{RST}}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.
- C pin
  Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG/$\overline{\text{RST}}$/C pins connection diagram



14. Block Diagram (MB95560H Series)



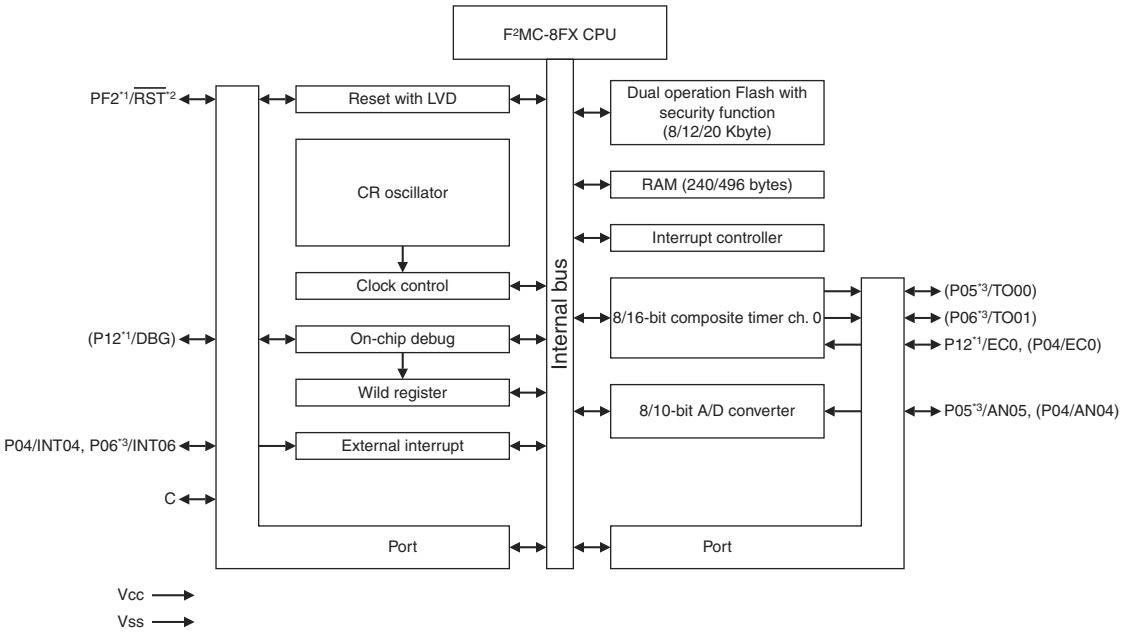
*1: PF2 and P12 are N-ch open drain pins.

*2: Software option

*3: P00 to P03, P05 to P07 and P62 to P64 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

15. Block Diagram (MB95570H Series)



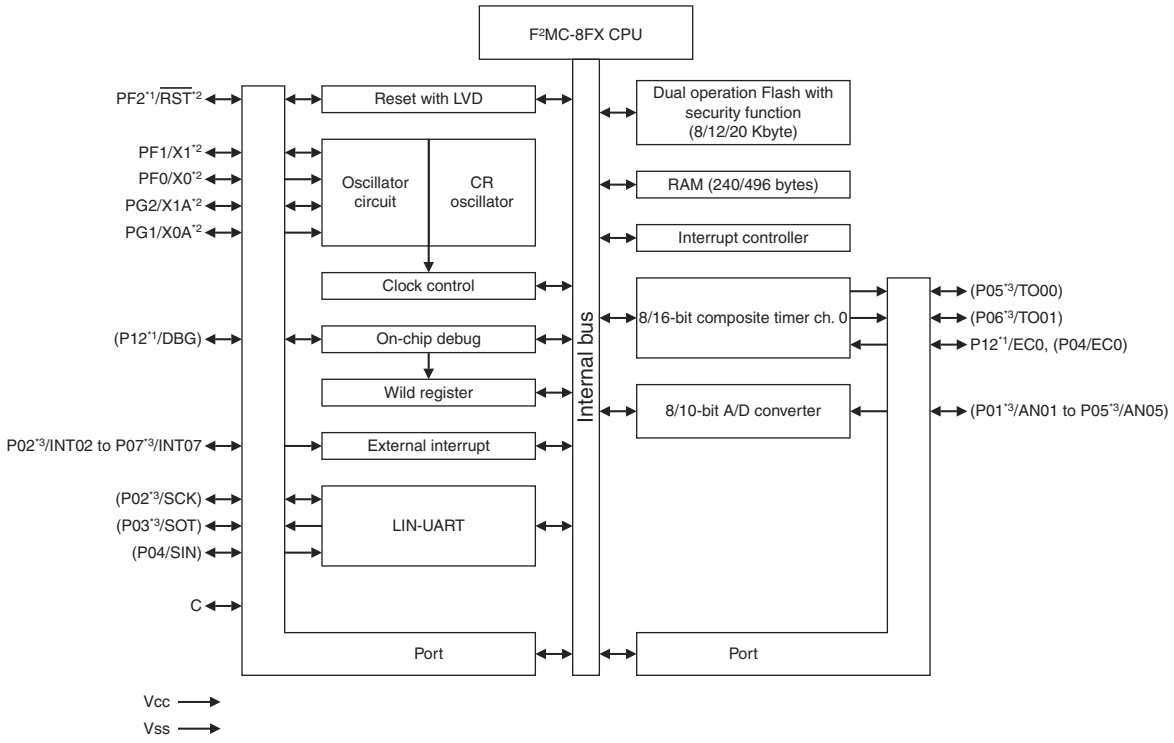
*1: PF2 and P12 are N-ch open drain pins.

*2: Software option

*3: P05 and P06 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

16. Block Diagram (MB95580H Series)



*1: PF2 and P12 are N-ch open drain pins.

*2: Software option

*3: P01 to P03 and P05 to P07 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

Address	Register abbreviation	Register name	R/W	Initial value
006C$_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000$_B$
006D$_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000$_B$
006E$_H$	ADDH	8/10-bit A/D converter data register (upper)	R/W	00000000$_B$
006F$_H$	ADDL	8/10-bit A/D converter data register (lower)	R/W	00000000$_B$
0070$_H$	—	(Disabled)	—	—
0071$_H$	FSR2	Flash memory status register 2	R/W	00000000$_B$
0072$_H$	FSR	Flash memory status register	R/W	000X0000$_B$
0073$_H$	SWRE0	Flash memory sector write control register 0	R/W	00000000$_B$
0074$_H$	FSR3	Flash memory status register 3	R	000XXXXX$_B$
0075$_H$	FSR4	Flash memory status register 4	R/W	00000000$_B$
0076$_H$	WREN	Wild register address compare enable register	R/W	00000000$_B$
0077$_H$	WROR	Wild register data test setting register	R/W	00000000$_B$
0078$_H$	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079$_H$	ILR0	Interrupt level setting register 0	R/W	11111111$_B$
007A$_H$	ILR1	Interrupt level setting register 1	R/W	11111111$_B$
007B$_H$, 007C$_H$	—	(Disabled)	—	—
007D$_H$	ILR4	Interrupt level setting register 4	R/W	11111111$_B$
007E$_H$	ILR5	Interrupt level setting register 5	R/W	11111111$_B$
007F$_H$	—	(Disabled)	—	—
0F80$_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000$_B$
0F81$_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000$_B$
0F82$_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000$_B$
0F83$_H$	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000$_B$
0F84$_H$	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000$_B$
0F85$_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000$_B$
0F86$_H$	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000$_B$
0F87$_H$	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000$_B$
0F88$_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000$_B$
0F89$_H$ to 0F91$_H$	—	(Disabled)	—	—
0F92$_H$	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	00000000$_B$
0F93$_H$	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	00000000$_B$
0F94$_H$	T01DR	8/16-bit composite timer 01 data register	R/W	00000000$_B$
0F95$_H$	T00DR	8/16-bit composite timer 00 data register	R/W	00000000$_B$
0F96$_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	00000000$_B$
0F97$_H$ to 0FC2$_H$	—	(Disabled)	—	—

23. Interrupt Source Table (MB95580H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	FFFA$_H$	FFFB$_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ01	FFF8$_H$	FFF9$_H$	L01 [1:0]	
External interrupt ch. 2	IRQ02	FFF6$_H$	FFF7$_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4$_H$	FFF5$_H$	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	FFF2$_H$	FFF3$_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0$_H$	FFF1$_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE$_H$	FFEF$_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFEC$_H$	FFED$_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEA$_H$	FFEB$_H$	L08 [1:0]	
—	IRQ09	FFE8$_H$	FFE9$_H$	L09 [1:0]	
—	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1:0]	
—	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1:0]	
—	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1:0]	
—	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1:0]	
—	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1:0]	
—	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1:0]	
—	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1:0]	
—	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1:0]	
Time-base timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1:0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1:0]	
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1:0]	
—	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1:0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1:0]	Low

24. Electrical Characteristics

24.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	−2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL}	—	15	mA	
"L" level average current	I_{OLAV1}	—	4	mA	Other than P00 to P03, P05 to P07, P62 to P64*4 Average output current= operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P00 to P03, P05 to P07, P62 to P64*4 Average output current= operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current= operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH}	—	−15	mA	
"H" level average current	I_{OHAV1}	—	−4	mA	Other than P00 to P03, P05 to P07, P62 to P64*4 Average output current= operating current × operating ratio (1 pin)
	I_{OHAV2}		−8		P00 to P03, P05 to P07, P62 to P64*4 Average output current= operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	−100	mA	
"H" level total average output current	ΣI_{OHAV}	—	−50	mA	Total average output current= operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	T_{stg}	−55	+150	°C	

*1: These parameters are based on the condition that V_{SS} is 0.0 V.

24.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

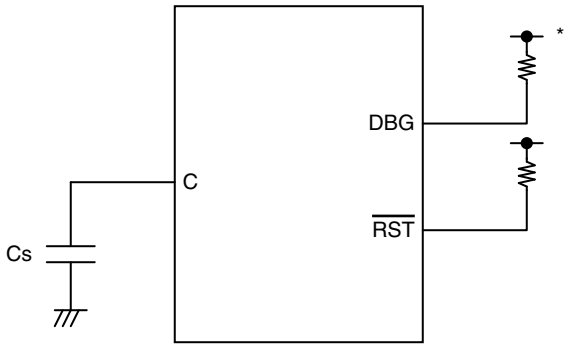
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1, *2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Decoupling capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	−40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The minimum power supply voltage becomes 2.88 V when a product with the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

• DBG / $\overline{\text{RST}}$ / C pins connection diagram



*: Connect the DBG pin to an external pull-up resistor of 2 kΩ or above. After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*2		
Power supply current*5	I_{LVD}	V_{CC}	Current consumption for the low-voltage detection circuit	—	3.6	6.6	µA	
	I_{CRH}		Current consumption for the main CR oscillator	—	220	280	µA	
	I_{CRL}		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	5.1	9.3	µA	
	I_{NSTBY}		Current consumption difference between normal standby mode and deep standby mode T_A = +25 °C	—	20	30	µA	

*1: V_{CC} = 5.0 V, T_A = + 25 °C

*2: V_{CC} = 5.5 V, T_A = + 85 °C (unless otherwise specified)

*3: P00, P62, P63 and P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

*4: P01, P02, P03, P07, PF0, PF1, PG1 and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.

*5:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See “24.4 AC Characteristics: Clock Timing” for F_{CH} and F_{CL}.
- See “24.4 AC Characteristics: Source Clock / Machine Clock” for F_{MP} and F_{MPL}.

*6: In sub-CR clock mode, the power supply current value is the sum of adding I_{CRL} to I_{CCLS} or I_{CCT}. In addition, when the sub-CR clock mode is selected with F_{MPL} being 50 kHz, the current consumption increases accordingly.

24.4.2 Source Clock / Machine Clock

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

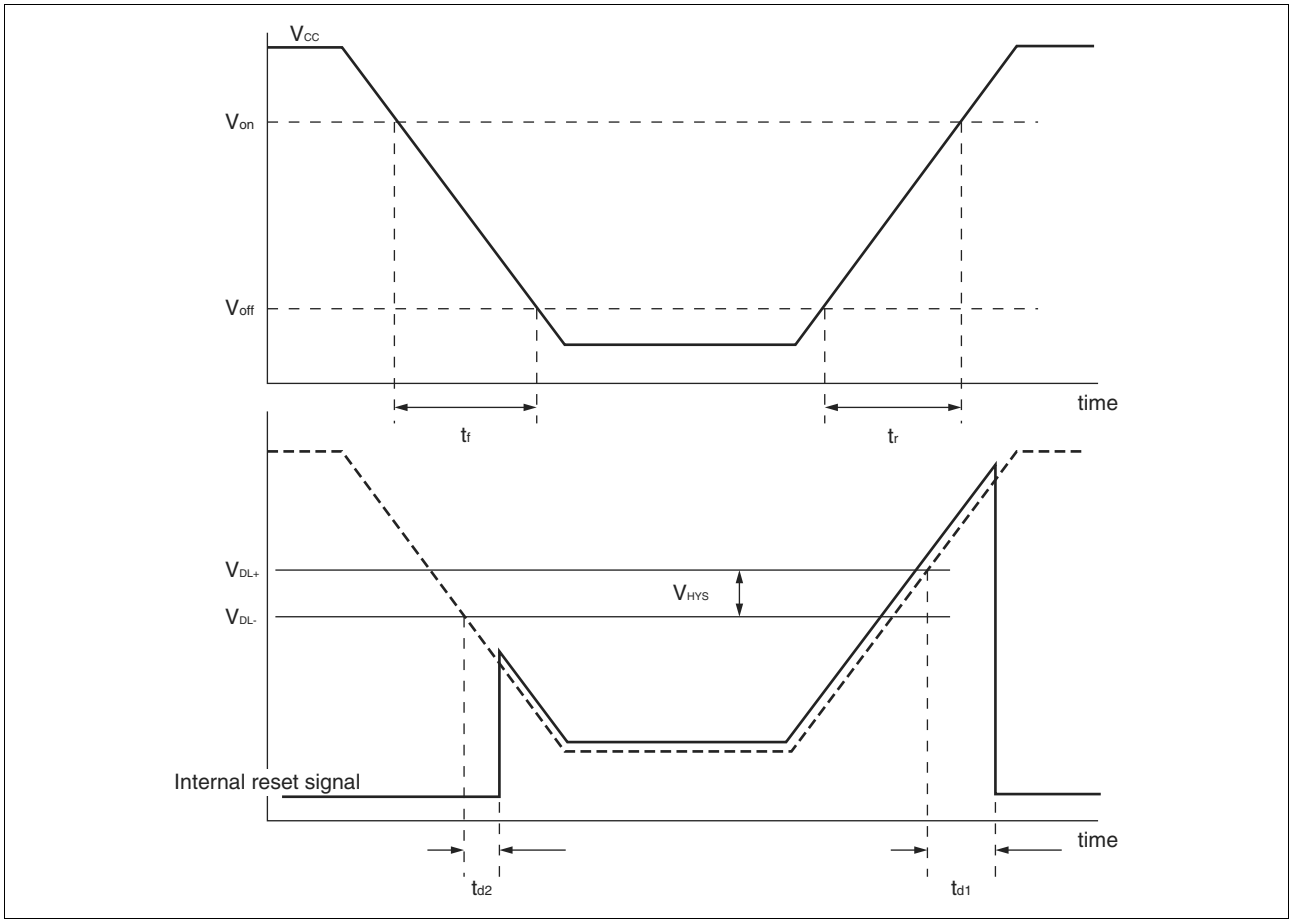
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			62.5	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 4 MHz, multiplied by 4 Max: F_{CRH} = 4 MHz, divided by 4
			—	61	—	µs	When the suboscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			—	4	—	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the suboscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			250	—	1000	ns	When the main CR clock is used Min: F_{SP} = 4 MHz, no division Max: F_{SP} = 4 MHz, divided by 4
			61	—	976.5	µs	When the suboscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.25	—	16	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the suboscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Subclock divided by 2
- Sub-CR clock divided by 2

*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

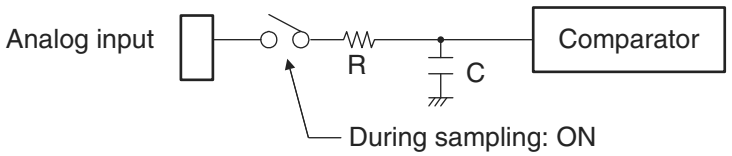

V_{CC}
V_{on}
V_{off}
time
t_f
t_r
V_{DL+}
V_{DL-}
V_{HYS}
Internal reset signal
time
t_{d2}
t_{d1}

24.5.2 Notes on Using A/D Converter

- External impedance of analog input and its sampling time

  The A/D converter of the MB95560H/570H/580H Series has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

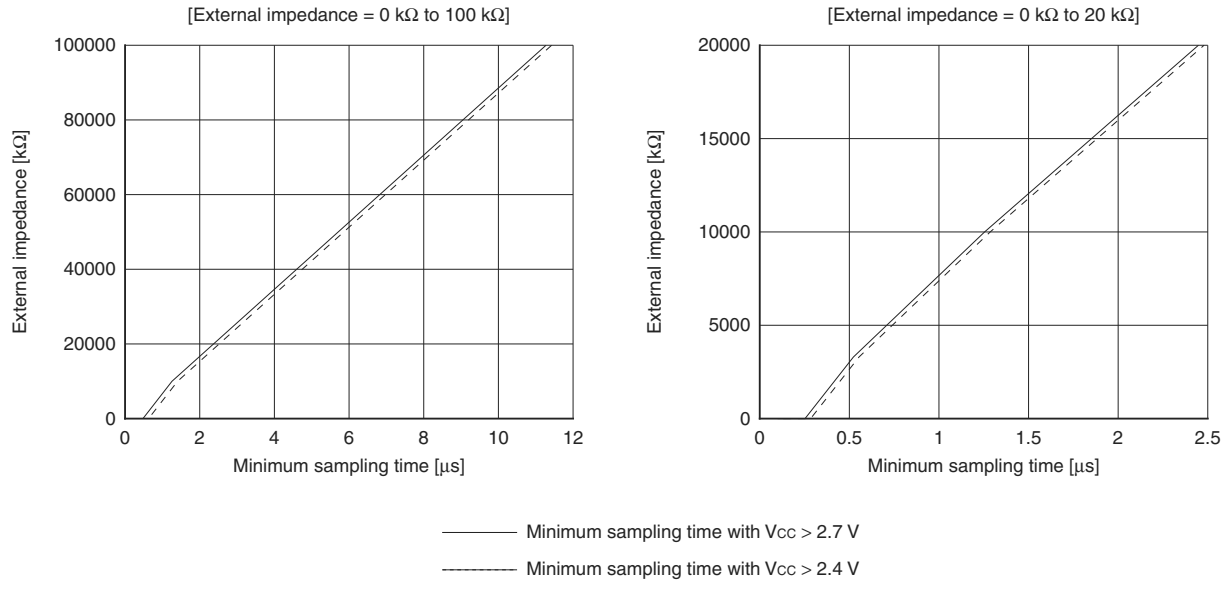
- Analog input equivalent circuit



V_{CC}	R	C
4.5 V ≤ V_{CC} ≤ 5.5 V	1.45 kΩ (Max)	14.89 pF (Max)
2.7 V ≤ V_{CC} < 4.5 V	2.7 kΩ (Max)	14.89 pF (Max)

Note: The values are reference values.

- Relationship between external impedance and minimum sampling time

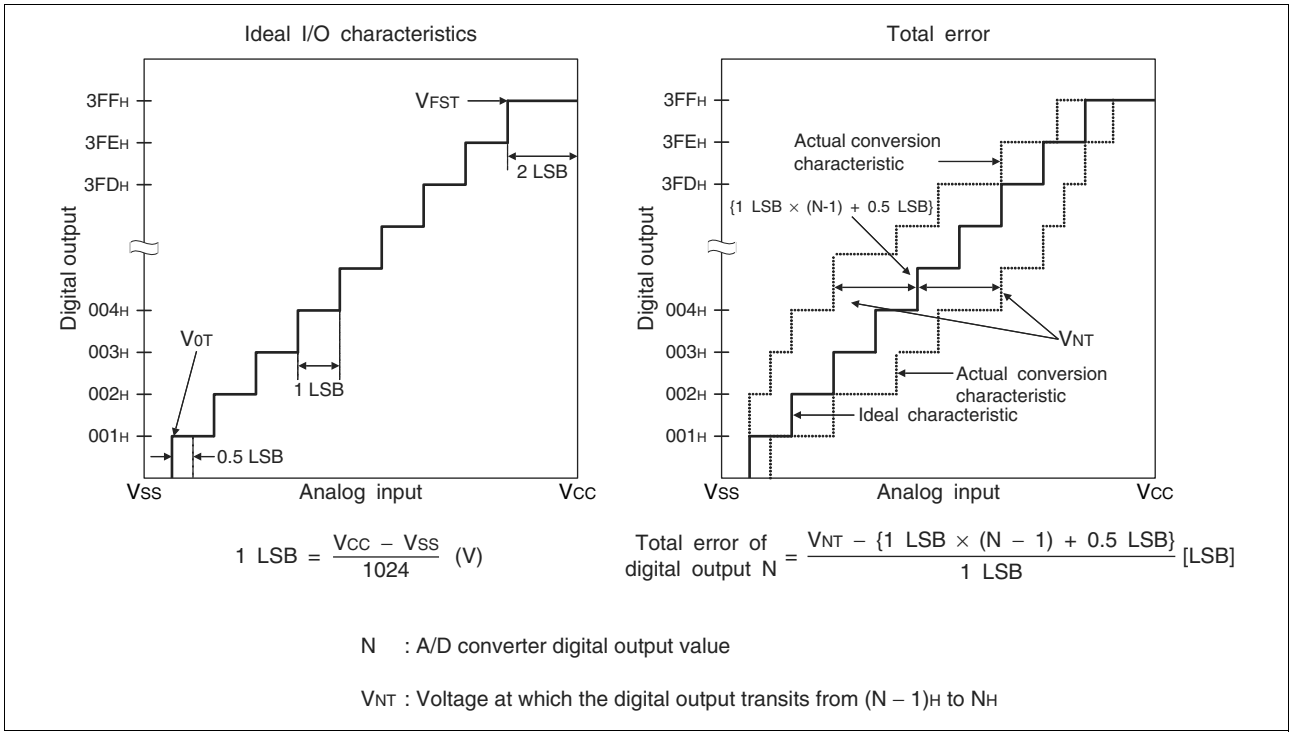


- A/D conversion error

  As |V_{CC} – V_{SS}| decreases, the A/D conversion error increases proportionately.

24.5.3 Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("0000000000" ← → "0000000001") of a device to the full-scale transition point ("1111111111" ← → "1111111110") of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (\text{V})$$

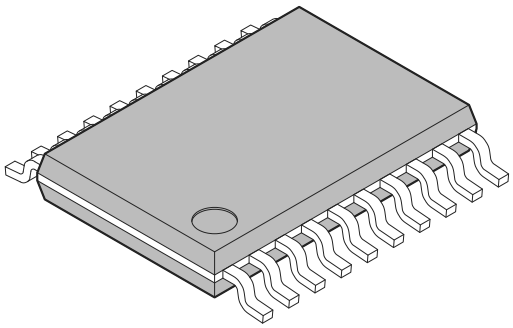
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

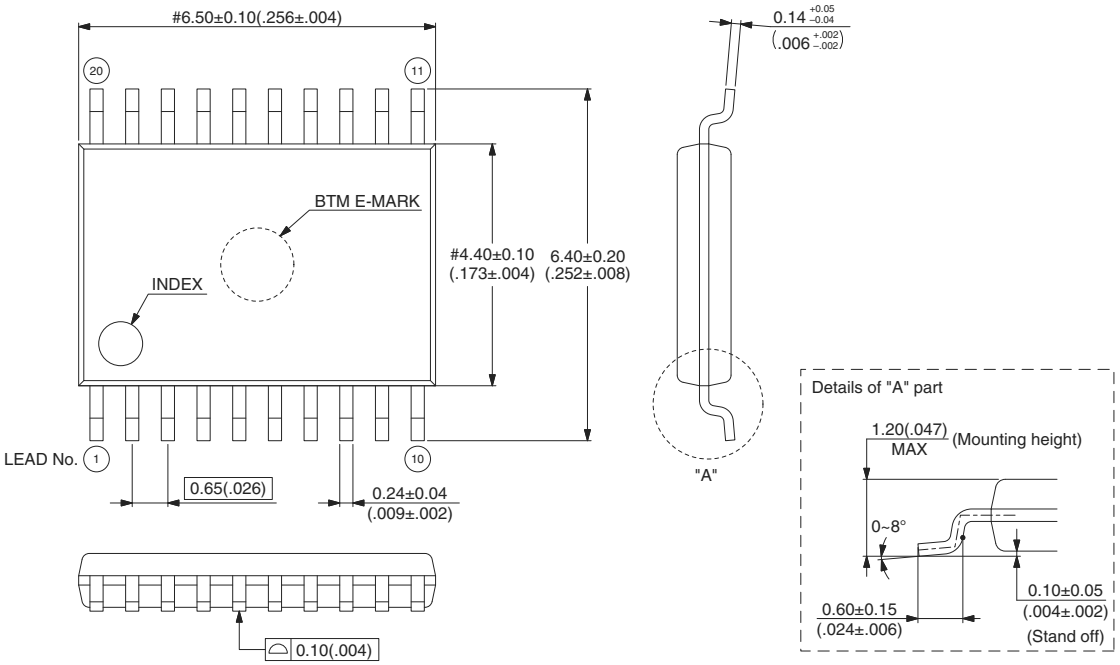
27. Ordering Information

Part number	Package
MB95F562HWQN-G-SNE1 MB95F562HWQN-G-SNERE1 MB95F562KWQN-G-SNE1 MB95F562KWQN-G-SNERE1 MB95F563HWQN-G-SNE1 MB95F563HWQN-G-SNERE1 MB95F563KWQN-G-SNE1 MB95F563KWQN-G-SNERE1 MB95F564HWQN-G-SNE1 MB95F564HWQN-G-SNERE1 MB95F564KWQN-G-SNE1 MB95F564KWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)
MB95F562HPF-G-SNE2 MB95F562KPF-G-SNE2 MB95F563HPF-G-SNE2 MB95F563KPF-G-SNE2 MB95F564HPF-G-SNE2 MB95F564KPF-G-SNE2 MB95F564KPF-G-UNE2	20-pin plastic SOP (FPT-20P-M09)
MB95F562HPFT-G-SNE2 MB95F562KPFT-G-SNE2 MB95F563HPFT-G-SNE2 MB95F563KPFT-G-SNE2 MB95F564HPFT-G-SNE2 MB95F564KPFT-G-SNE2 MB95F564KPFT-G-UNE2	20-pin plastic TSSOP (FPT-20P-M10)
MB95F582HWQN-G-SNE1 MB95F582HWQN-G-SNERE1 MB95F582KWQN-G-SNE1 MB95F582KWQN-G-SNERE1 MB95F583HWQN-G-SNE1 MB95F583HWQN-G-SNERE1 MB95F583KWQN-G-SNE1 MB95F583KWQN-G-SNERE1 MB95F584HWQN-G-SNE1 MB95F584HWQN-G-SNERE1 MB95F584KWQN-G-SNE1 MB95F584KWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)
MB95F582HPFT-G-SNE2 MB95F582KPFT-G-SNE2 MB95F583HPFT-G-SNE2 MB95F583KPFT-G-SNE2 MB95F584HPFT-G-SNE2 MB95F584KPFT-G-SNE2	16-pin plastic TSSOP (FPT-16P-M08)

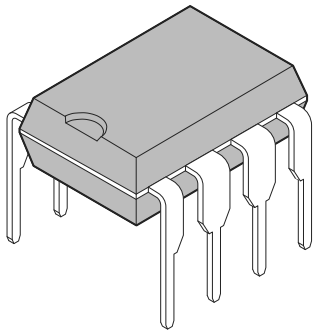
20-pin plastic TSSOP		
	Lead pitch	0.65 mm
	Package width × package length	4.40 mm × 6.50 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.08 g
(FPT-20P-M10)		

20-pin plastic TSSOP
(FPT-20P-M10)

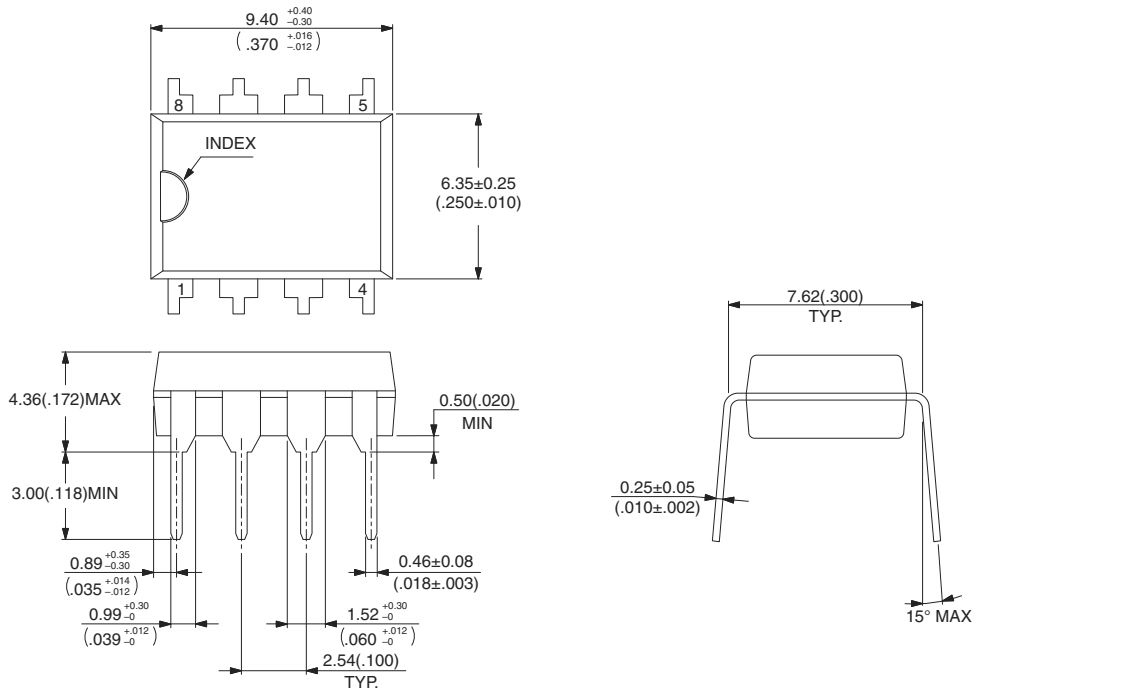
Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

8-pin plastic DIP	Lead pitch	2.54 mm
	Sealing method	Plastic mold
(DIP-8P-M03)		

8-pin plastic DIP
(DIP-8P-M03)



Dimensions in mm (inches).
Note: The values in parentheses are reference values

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