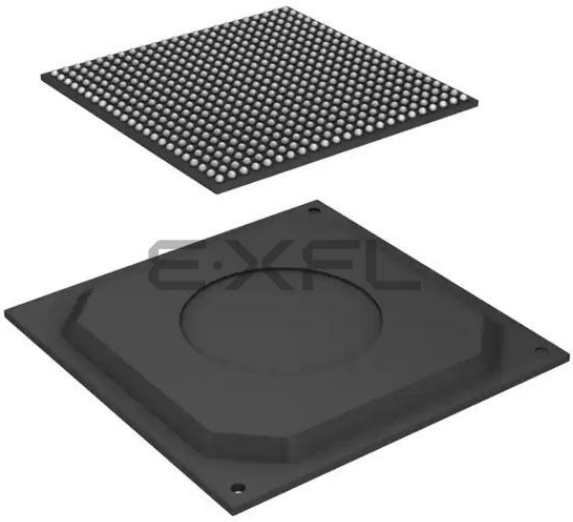

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx535dvv1b

Table 8. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_JTAG		Use maximal IO Eq[1], N=6	
NVCC_KPAD		Use maximal IO Eq[1], N=11	
NVCC_LCD		Use maximal IO Eq[1], N=29	
NVCC_LVDS		Use maximal IO Eq[1], N=20	
NVCC_LVDS_BG		Use maximal IO Eq[1], N=1	
NVCC_NANDF		Use maximal IO Eq[1], N=8	
NVCC_PATA		Use maximal IO Eq[1], N=29	
NVCC_REST		Use maximal IO Eq[1], N=5	
NVCC_SD1		Use maximal IO Eq[1], N=6	
NVCC_SD2		Use maximal IO Eq[1], N=6	
NVCC_XTAL		Use maximal IO Eq[1], N=2	

[1] General Equation for estimated, maximal power consumption of an IO power supply:

Imax = N * C * V * (0.5 * F)

Where:

N - Number of IO pins supplies by the power line

C - Equivalent external capacitive load

V - IO voltage

(0.5 * F) - Data change rate. Up to 0.5 of the clock rate (F).

4.1.6 USB-OH-3 (OTG + 3 Host ports) Module and the Two USB PHY (OTG and H1) Current Consumption

Table 9 shows the USB interface current consumption.

Table 9. USB Interface Current Consumption

Parameter	Conditions		Typical @ 25 °C	Max	Unit
Analog Supply 3.3 V USB_H1_VDDA33 USB_OTG_VDDA33	Full Speed	RX	5.5	6	mA
		TX	7	8	
	High Speed	RX	5	6	
		TX	5	6	

Table 37. Revision 2.0 EIM Internal Module Multiplexing

Setup	Non Multiplexed Address/Data Mode						Multiplexed Address/Data mode	
	8 Bit			16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 111	MUM = 0, DSZ = 111	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
A[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]	EIM_DA[15:0]
A[25:16]	EIM_A[25:16]	EIM_A[25:16]	EIM_A[25:16]	EIM_A[25:16]	EIM_A[25:16]	EIM_A[24:16][1]	EIM_A[25:16]	NANDF_D[8:0][1]
D[7:0], EIM_EB0	NANDF_D[7:0][2]			NANDF_D[7:0][2]		NANDF_D[7:0]	EIM_DA[7:0]	EIM_DA[7:0]
D[15:8], EIM_EB1		NANDF_D[15:8][3]		NANDF_D[15:8][3]		NANDF_D[15:8]	EIM_DA[15:8]	EIM_DA[15:8]
D[23:16], EIM_EB2					EIM_D[23:16]	EIM_D[23:16]		NANDF_D[7:0]
D[31:24], EIM_EB3			EIM_D[31:24]		EIM_D[31:24]	EIM_D[31:24]		NANDF_D[15:8]

1 For 32-bit mode, the address range is A[24:0], due to address space allocation in memory map.

2 NANDF_D[7:0] multiplexed on ALT3 mode of PATA_DATA[7:0]

3 NANDF_D[15:8] multiplexed on ALT3 mode of PATA_DATA[15:8]

NOTE

To receive the reported setup/hold values, write calibration should be perform to locate the DQS in the middle of DQ window.

Figure 29 shows the read timing parameters.

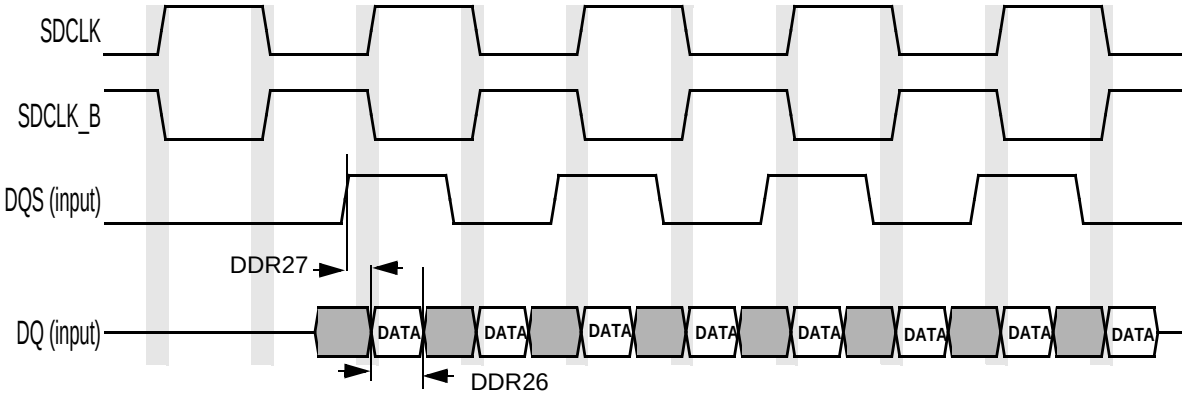

Figure 29. DDR SDRAM DQ vs. DQS and SDCLK Read Cycle

4.7 External Peripheral Interfaces Parameters

The following subsections provide information on external peripheral interfaces.

4.7.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.7.2 CSPI and ECSPI Timing Parameters

This section describes the timing parameters of the CSPI and ECSPI blocks. The CSPI and ECSPI have separate timing parameters for master and slave modes. The nomenclature used with the CSPI / ECSPI modules and the respective routing of these signals is shown in Table 40.

Table 40. CSPI Nomenclature and Routing

Block Instance	I/O Access
ECSPI-1	GPIO, KPP, DISP0_DAT, CSI0_DAT and EIM_D through IOMUXC
ECSPI-2	DISP0_DAT, CSI0_DAT and EIM through IOMUXC
CSPI	DISP0_DAT, EIM_A/D, SD1 and SD2 through IOMUXC

4.7.2.1 CSPI Master Mode Timing

Figure 30 depicts the timing of CSPI in master mode. Table 41 lists the CSPI master mode timing characteristics.

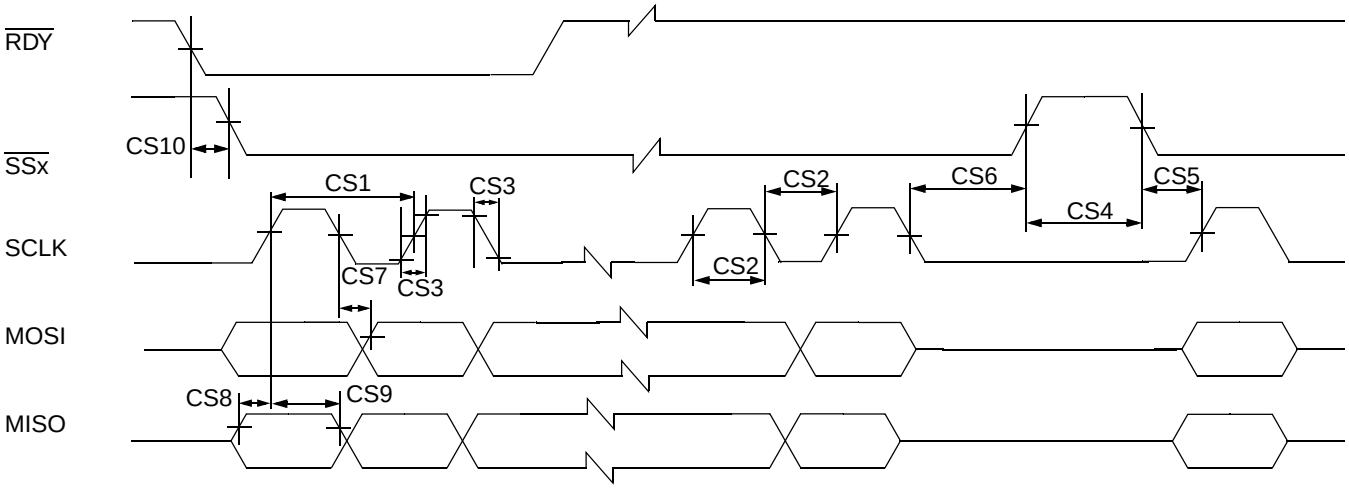

Figure 30. CSPI/ECSPI Master Mode Timing Diagram

Table 41. CSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	60		ns
CS2	SCLK High or Low Time	t_{SW}	26		ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$			ns
CS4	SSx pulse width	t_{CSLH}	26		ns
CS5	SSx Lead Time (Slave Select setup time)	t_{SCS}	26		ns
CS6	SSx Lag Time (SS hold time)	t_{HCS}	26		ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	1	21	ns
CS8	MISO Setup Time	t_{Smiso}	5		ns
CS9	MISO Hold Time	t_{Hmiso}	5		ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5		ns

1 See specific I/O AC parameters Section 4.5, I/O AC Parameters

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

Table 57. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET * Tdiclk	DISP_CLK_OFFSET offset of IPP_DISP_CLK edges from local start point, in DI_CLK [2] (0.5 DI_CLK Resolution) Defined by DISP_CLK counter	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET * Tdiclk	VSYNC_OFFSET offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK [2] (0.5 DI_CLK Resolution).The VSYNC_OFFSET should be built by suitable DI s counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET * Tdiclk	HSYNC_OFFSET offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK [2] (0.5 DI_CLK Resolution).The HSYNC_OFFSET should be built by suitable DI s counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET * Tdiclk	DRDY_OFFSET offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK [2] (0.5 DI_CLK Resolution) The DRDY_OFFSET should be built by suitable DI s counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} * \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}, & \text{for integer } \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \\ T_{diclk} * floor\left[\frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}\right] + 0.5 \text{ or } 0.5, & \text{for fractional } \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \end{cases}$$

DISP_CLK_PERIOD number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.

DI_CLK_PERIOD relation of between programing clock frequency and current system clock frequency

Display interface clock period average value.

$$\overline{Tdicp} = T_{diclk} * \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}$$

[2] DI s counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI s registers directly (by name), but can be generated by corresponding DI s counter. The SCREEN_WIDTH is an input value for DI s HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$Accuracy = \pm 0.5 * T_{diclk} \pm 0.62ns$$

Table 72. UDMA in Burst Timing Parameters (continued)

ATA Parameter	Parameter from Figure 70 , Figure 71 , Figure 72	Description	Controlling Variable
tcyc	tc1	(tcyc tskew) > T	T big enough
trp	trp	trp (min) = time_rp UT (tskew1 + tskew2 + tskew6)	time_rp
	tx1 [1]	(time_rp UT) (tco + tsu + 3T + 2 Utbuf + 2 Utcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) UT	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) UT	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs UT) (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh UT) (tskew1 + tskew2)	time_cvh
	ton toff[2]	ton = time_on UT tskew1 toff = time_off UT tskew1	

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2 Make ton and toff big enough to avoid bus contention.

4.7.12.3 UDMA Output Timing

Figure 73 shows timing when the UDMA out transfer starts, Figure 74 shows timing when the UDMA out host terminates transfer, Figure 75 shows timing when the UDMA out device terminates transfer, and Table 73 lists the timing parameters for UDMA out burst.

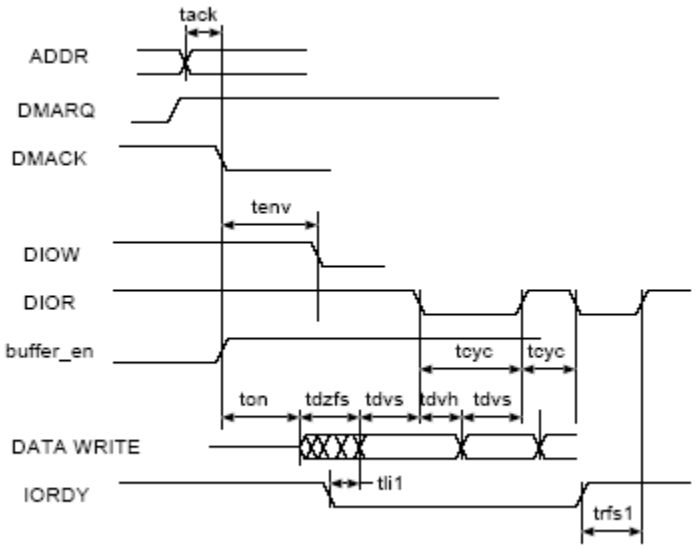

Figure 73. UDMA Out Transfer Starts Timing Diagram

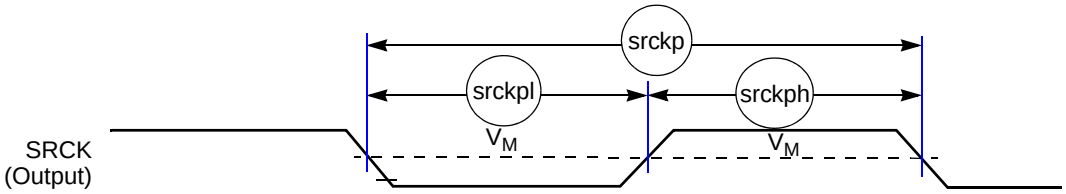

Figure 81. SPDIF Timing Diagram

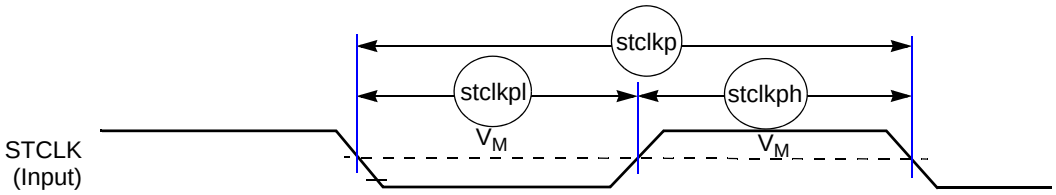

Figure 82. STCLK Timing

4.7.16 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 79.

Table 79. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External AUD3 I/O
AUDMUX port 4	AUD4	External EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).

The SSI timing diagrams use generic signal names wherein the names used in the i.MX53xD reference manual are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

4.7.16.3 SSI Transmitter Timing with External Clock

Figure 85 depicts the SSI transmitter external clock timing and Table 82 lists the timing parameters for the transmitter timing with the external clock.

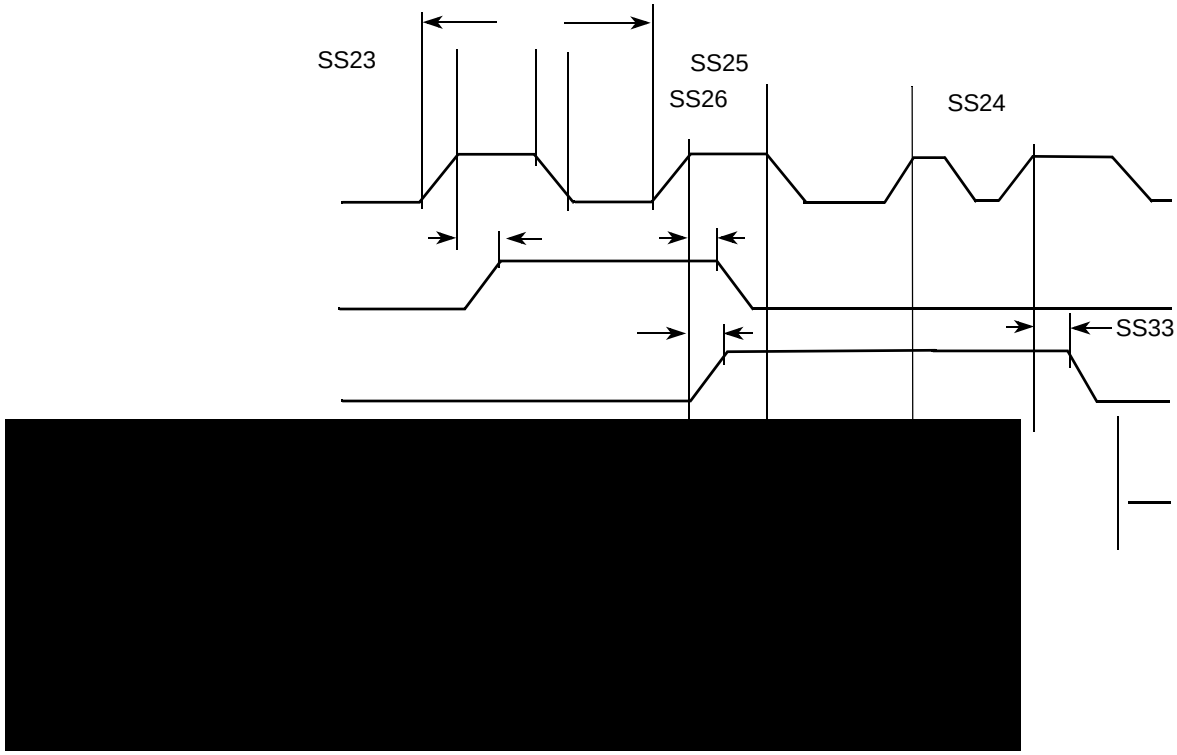

Figure 85. SSI Transmitter External Clock Timing Diagram

Table 82. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4		ns
SS23	(Tx/Rx) CK clock high period	36.0		ns
SS24	(Tx/Rx) CK clock rise time		6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0		ns
SS26	(Tx/Rx) CK clock fall time		6.0	ns
SS27	(Tx) CK high to FS (bl) high	10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0		ns
SS31	(Tx) CK high to FS (wl) high	10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0		ns
SS37	(Tx) CK high to STXD valid from high impedance		15.0	ns
SS38	(Tx) CK high to STXD high/low		15.0	ns

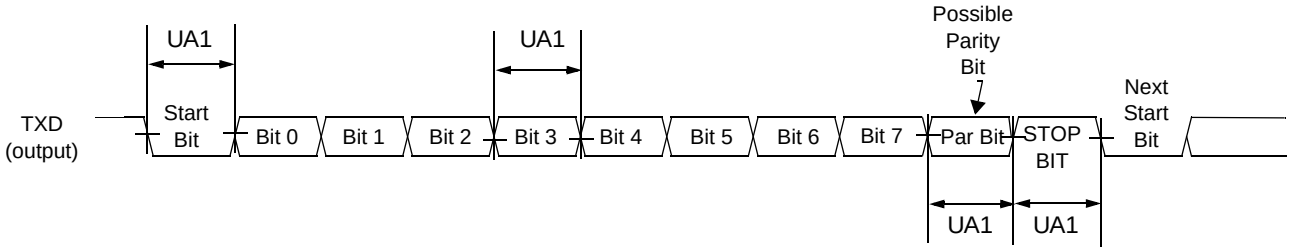

Figure 87. UART RS-232 Serial Mode Transmit Timing Diagram

Table 85. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud_rate}$[1] T_{ref_clk}[2]	$1/F_{baud_rate} + T_{ref_clk}$	

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.7.17.2.2 UART Receiver

Figure 88 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 86 lists serial mode receive timing characteristics.

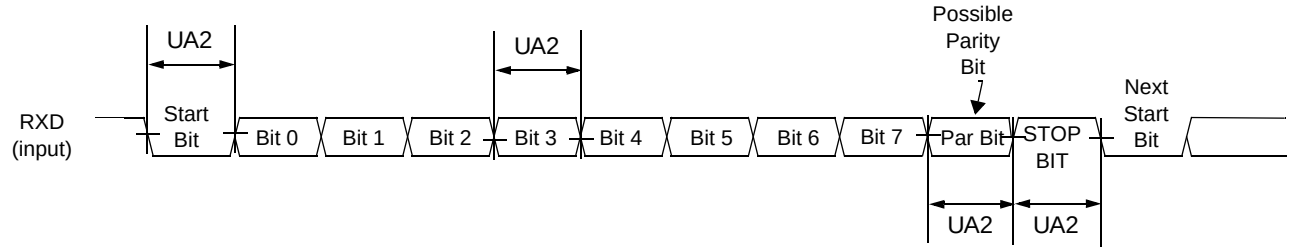

Figure 88. UART RS-232 Serial Mode Receive Timing Diagram

Table 86. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud_rate}$[2] $1/(16*F_{baud_rate})$	$1/F_{baud_rate} + 1/(16*F_{baud_rate})$	

[1] The UART receiver can tolerate $1/(16*F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.7.17.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.7.17.3.3 UART IrDA Mode Transmitter

Figure 89 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 87 lists the transmit timing characteristics.

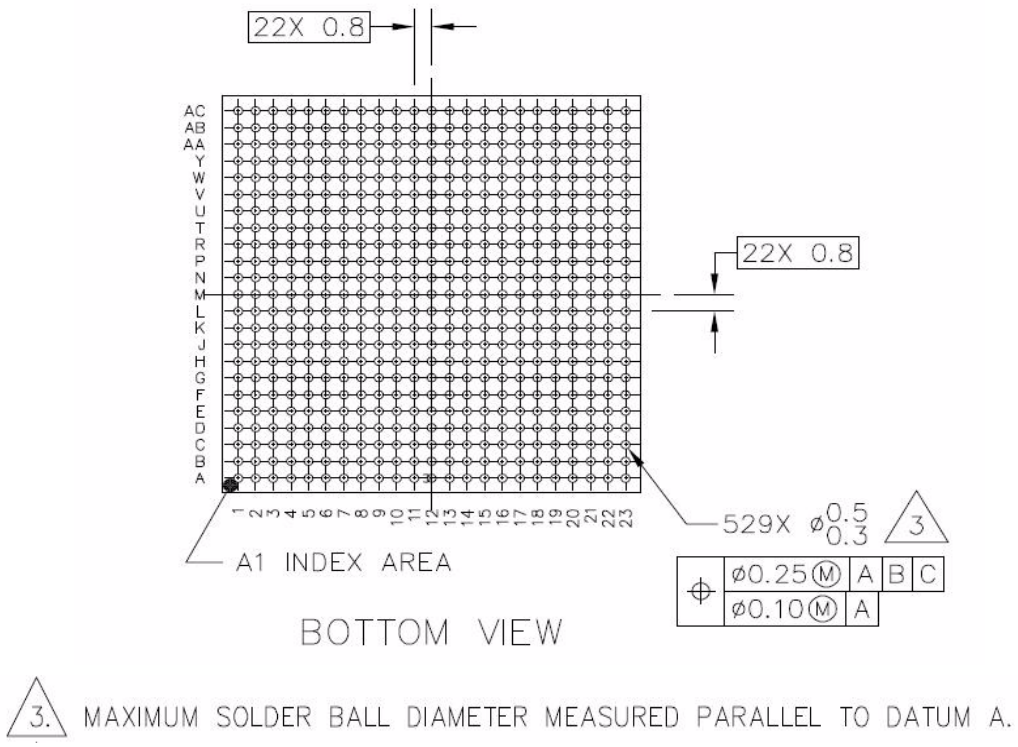

Figure 101. 19 x 19 mm Package, 529 Solder Balls, Bottom View

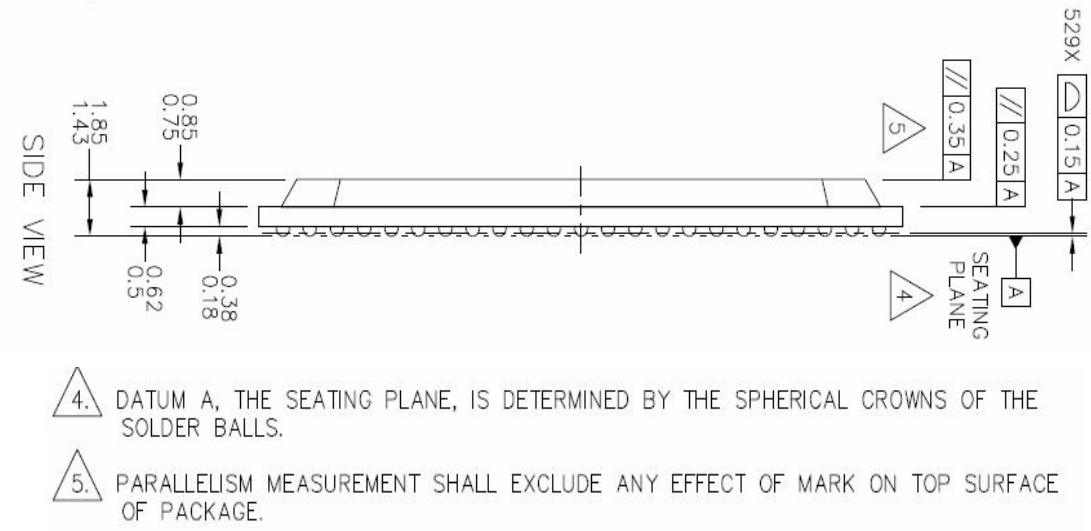

Figure 102. 19 x 19 mm Package Side View

Table 110. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition [1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
DISP0_DAT9	E2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[30]	Input	100 K : PU
DRAM_A0	M19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[0]	Output	Low
DRAM_A1	L21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[1]	Output	Low
DRAM_A10	K19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[10]	Output	Low
DRAM_A11	L22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[11]	Output	Low
DRAM_A12	L20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[12]	Output	Low
DRAM_A13	L23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[13]	Output	Low
DRAM_A14	N18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[14]	Output	Low
DRAM_A15	M18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[15]	Output	Low
DRAM_A2	M20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[2]	Output	Low
DRAM_A3	N20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[3]	Output	Low
DRAM_A4	K20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[4]	Output	Low
DRAM_A5	N21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[5]	Output	Low
DRAM_A6	M22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[6]	Output	Low
DRAM_A7	N22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[7]	Output	Low
DRAM_A8	N23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[8]	Output	Low
DRAM_A9	M21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[9]	Output	Low
DRAM_CALIBRATION	M23	NVCC_EMI_DRAM	special			(used in DRAM driver calibration. See Special Signal Considerations {add xref} above)	Input	
DRAM_CAS	L18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CAS	Output	High
DRAM_CS0	K18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CS[0]	Output	High
DRAM_CS1	P19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CS[1]	Output	High

Table 110. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Package Pin Name	Package Pin Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition [1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config./ Value
DRAM_D26	Y21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[26]	Output	High
DRAM_D27	W22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[27]	Output	High
DRAM_D28	AA23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[28]	Output	High
DRAM_D29	V23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[29]	Output	High
DRAM_D3	G20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[3]	Output	High
DRAM_D30	AA22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[30]	Output	High
DRAM_D31	W23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[31]	Output	High
DRAM_D4	J23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[4]	Output	High
DRAM_D5	G23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[5]	Output	High
DRAM_D6	J22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[6]	Output	High
DRAM_D7	G22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[7]	Output	High
DRAM_D8	E21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[8]	Output	High
DRAM_D9	D21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[9]	Output	High
DRAM_DQM0	H21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[0]	Output	Low
DRAM_DQM1	E20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[1]	Output	Low
DRAM_DQM2	T20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[2]	Output	Low
DRAM_DQM3	W20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[3]	Output	Low
DRAM_RAS	J19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_RAS	Output	High
DRAM_RESET	P18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_RESET	Output	Low
DRAM_SDBA0	R19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDBA[0]	Output	Low
DRAM_SDBA1	P20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDBA[1]	Output	Low

6.3.2.1 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments

Table 112 and Table 113 show the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 112. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
DDR_VREF	U23
GND	A1, A2, A28, A29, B1, B2, B28, B29, C17, L14, L15, L16, M14, M15, M16, N14, N15, N16, P11,P12, P13, P17, P18, P19, R11, R12, R13, R17, R18, R19, T11,T12, T13, T17, T18, T19, U14, U15, U16, V14, V15, V16, W14,W15, W16, AH1, AH15, AH29, AJ1, AJ2, AJ15, AJ28, AJ29
NVCC_CKIH	AD22
NVCC_CSI	J6
NVCC_EIM_MAIN	G9
NVCC_EIM_SEC	G6
NVCC_EMI_DRAM	F24, G24, H24, K24, L24, N24, P24, R24, U24, V24, W24, AC24, AD24
NVCC_EMI_DRAM_2P5	K23,Y24
NVCC_FEC	AC14
NVCC_GPIO	AD9
NVCC_JTAG	AD11
NVCC_KEYPAD	AD6
NVCC_LCD	W7, Y7
NVCC_LVDS	F19
NVCC_LVDS_BG	F18
NVCC_NANDF	G12
NVCC_PATA	N6
NVCC_RESET	AD18
NVCC_SD1	AC20
NVCC_SD2	AC16
NVCC_SRTC_POW	F13
NVCC_XTAL	F14
POP_VACC	AG14
POP_VCCMM	C8, L3
POP_VCCQMM	C11
POP_VCCQMM1	H3
POP_VDD1	C3, C13, C26, T3, T27, AG6, AG26

Table 114. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	PoP Bottom Package Contact Assignment	PoP Top Package Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition [1]			
					Alt. Mode	Function	Direction	Config./ Value
EIM_DA14	J2	G1	NVCC_EIM_MAIN	UHVIO	ALT0	emi_NAND_EIM_DA[14]	Input	100 K : PU
EIM_DA15	K2	H1	NVCC_EIM_MAIN	UHVIO	ALT0	emi_NAND_EIM_DA[15]	Input	100 K : PU
EIM_DA2	F10		NVCC_EIM_MAIN	UHVIO	ALT0	emi_NAND_EIM_DA[2]	Input[2]	100 K : PU
EIM_DA3	A8		NVCC_EIM_MAIN	UHVIO	ALT0	emi_NAND_EIM_DA[3]	Input[2]	100 K : PU
EIM_DA4	E3	D2	NVCC_EIM_MAIN	UHVIO	ALT0	emi_NAND_EIM_DA[4]	Input[2]	100 K : PU
EIM_DA5	F3	E2	NVCC_EIM_MAIN	UHVIO	ALT0	emi_NAND_EIM_DA[5]	Input[2]	100 K : PU
EIM_DA6	J3	G2	NVCC_EIM_MAIN	UHVIO	ALT0	emi_NAND_EIM_DA[6]	Input[2]	100 K : PU
EIM_DA7	K3	H2	NVCC_EIM_MAIN	UHVIO	ALT0	emi_NAND_EIM_DA[7]	Input[2]	100 K : PU
EIM_DA8	A10		NVCC_EIM_MAIN	UHVIO	ALT0	emi_NAND_EIM_DA[8]	Input[2]	100 K : PU
EIM_DA9	K6		NVCC_EIM_MAIN	UHVIO	ALT0	emi_NAND_EIM_DA[9]	Input[2]	100 K : PU
EIM_EB0	J1		NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_EB[0]	Output[2]	
EIM_EB1	G7		NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_EB[1]	Output[2]	
EIM_EB2	J7		NVCC_EIM_MAIN	UHVIO	ALT1	gpio2_GPIO[30]	Input	100 K : PU
EIM_EB3	F6		NVCC_EIM_MAIN	UHVIO	ALT1	gpio2_GPIO[31]	Input	100 K : PU
EIM_LBA	A5		NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_LBA	Output[2]	
EIM_OE	A9		NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_OE	Output	
EIM_RW	H7		NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_RW	Output	
EIM_WAIT	L6		NVCC_EIM_MAIN	UHVIO	ALT0	emi_EIM_WAIT	Output	
EXTAL	G15		NVCC_XTAL	ANALOG	EXTAL			
FASTR_ANA	AD29		NVCC_CKIH	ANALOG	FASTR_ANA			
FASTR_DIG	AD28		NVCC_CKIH	ANALOG	FASTR_DIG			
FEC_CRS_DV	Y27		NVCC_FEC	UHVIO	ALT1	gpio1_GPIO[25]	Input	100 K : PU

Table 115. PoP 12 u12 mm, 0.4 Pitch Top Ball Map (continued)

	R	P	N	M	L	K	J	
1	GND	POP_ZQ	NANDF_WP_B	NANDF_CS0	PATA_DA_0	NANDF_WE_B	POP_VCCMM	1
2	POP_VDD2	DDR_VREF	POP_VDD1	GND	NANDF_ALE	NANDF_RE_B	GND	2
3	NC	NC	NC	NC	NC	NC	NC	3
4	NC	NC	NC	NC	NC	NC	NC	4
5	NC	NC	NC	NC	NC	NC	NC	5
6	NC	NC	NC	NC	NC	NC	NC	6
7	NC	NC	NC	NC	NC	NC	NC	7
8	NC	NC	NC	NC	NC	NC	NC	8
9	NC	NC	NC	NC	NC	NC	NC	9
10	NC	NC	NC	NC	NC	NC	NC	10
11	NC	NC	NC	NC	NC	NC	NC	11
12	NC	NC	NC	NC	NC	NC	NC	12
13	NC	NC	NC	NC	NC	NC	NC	13
14	NC	NC	NC	NC	NC	NC	NC	14
15	NC	NC	NC	NC	NC	NC	NC	15
16	NC	NC	NC	NC	NC	NC	NC	16
17	NC	NC	NC	NC	NC	NC	NC	17
18	NC	NC	NC	NC	NC	NC	NC	18
19	NC	NC	NC	NC	NC	NC	NC	19
20	NC	NC	NC	NC	NC	NC	NC	20
21	NC	NC	NC	NC	NC	NC	NC	21
22	POP_VDDQ	DRAM_SDQS0_B	POP_VDD1	DDR_VREF	POP_VDD2	POP_VDDQ	DRAM_SDQS2	22
23	DRAM_SDQS0	GND	DRAM_DQM0	GND	DRAM_DQM2	DRAM_SDQS2_B	GND	23
	R	P	N	M	L	K	J	