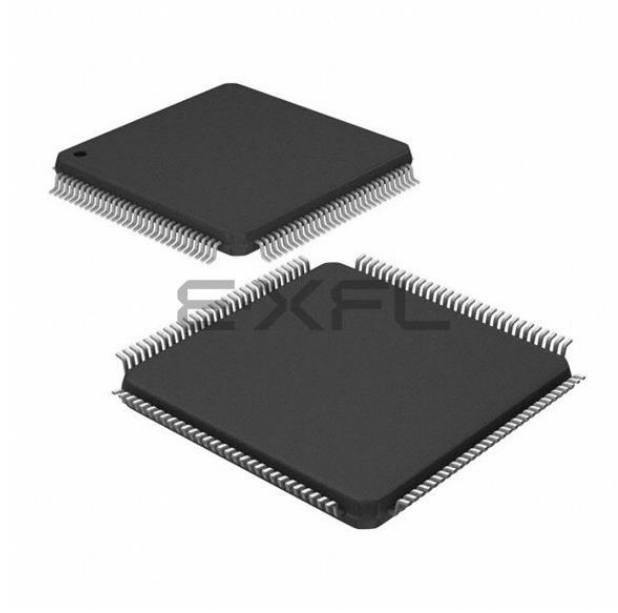
Infineon Technologies - MB96F653RBPMC-GSE2 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	101
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 29x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f653rbpmc-gse2

MB96650 Series

F²MC-16FX 16-bit Microcontroller

MB96650 series is based on Cypress's advanced F²MC-16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established F²MC-16LX family thus allowing for easy migration of F²MC-16LX Software to the new F²MC-16FX products. F²MC-16FX product improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time. For high processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 32MHz operation frequency from an external 4MHz to 8MHz resonator. The result is a minimum instruction cycle time of 31.2ns going together with excellent EMI behavior. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows selecting suitable operation frequencies for peripheral resources independent of the CPU speed.

Features

Technology

0.18µm CMOS

CPU

- F²MC-16FX CPU
- Optimized instruction set for controller applications (bit, byte, word and long-word data types, 23 different addressing modes, barrel shift, variety of pointers)
- 8-byte instruction queue
- Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available

System clock

- On-chip PLL clock multiplier (×1 to ×8, ×1 when PLL stop)
- 4MHz to 8MHz crystal oscillator (maximum frequency when using ceramic resonator depends on Q-factor)
- Up to 8MHz external clock for devices with fast clock input feature
- 32.768kHz subsystem quartz clock
- 100kHz/2MHz internal RC clock for quick and safe startup, clock stop detection function, watchdog
- Clock source selectable from mainclock oscillator, subclock oscillator and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals
- The subclock oscillator is enabled by the Boot ROM program controlled by a configuration marker after a Power or External reset
- Low Power Consumption - 13 operating modes (different Run, Sleep, Timer, Stop modes)

On-chip voltage regulator

Internal voltage regulator supports a wide MCU supply voltage range (Min=2.7V), offering low power consumption

Low voltage detection function

Reset is generated when supply voltage falls below programmable reference voltage

Code Security

Protects Flash Memory content from unintended read-out

DMA

Automatic transfer function independent of CPU, can be assigned freely to resources

Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1Mbps
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

USART

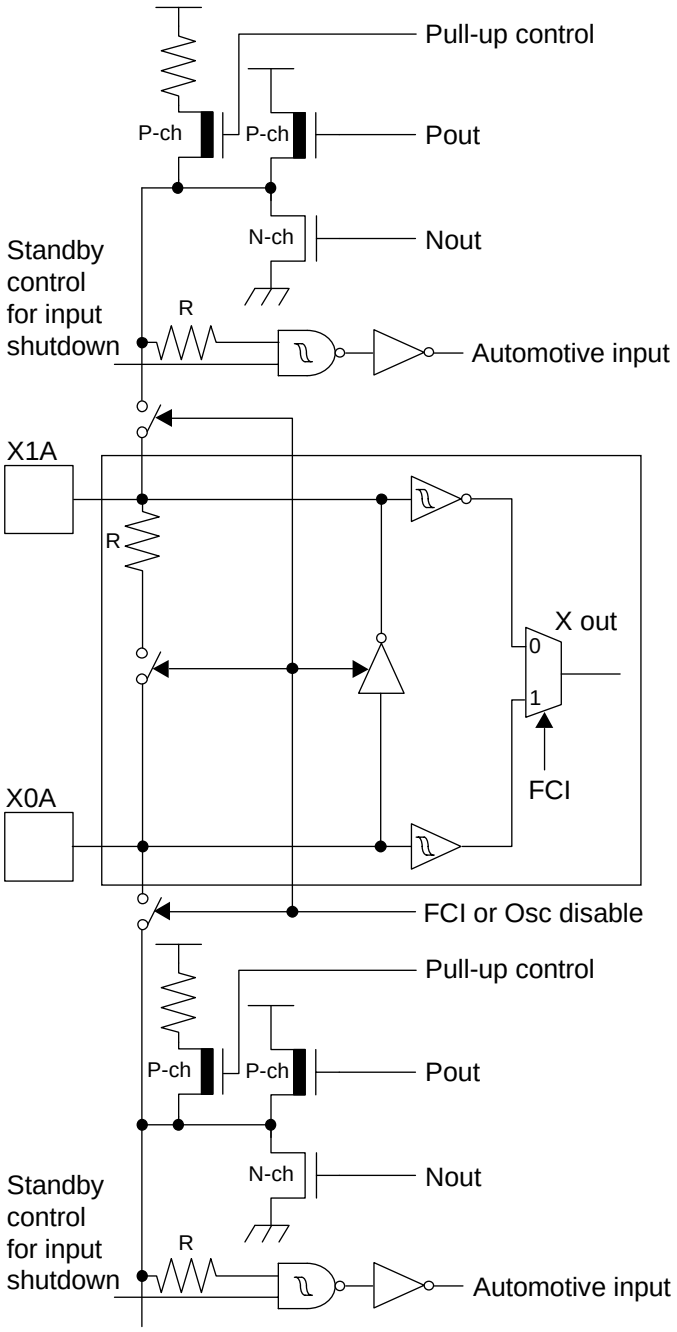
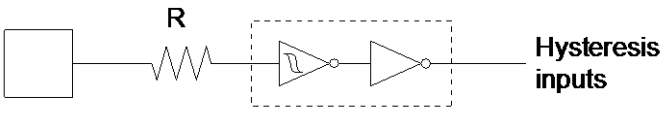
- Full duplex USARTs (SCI/LIN)

Contents

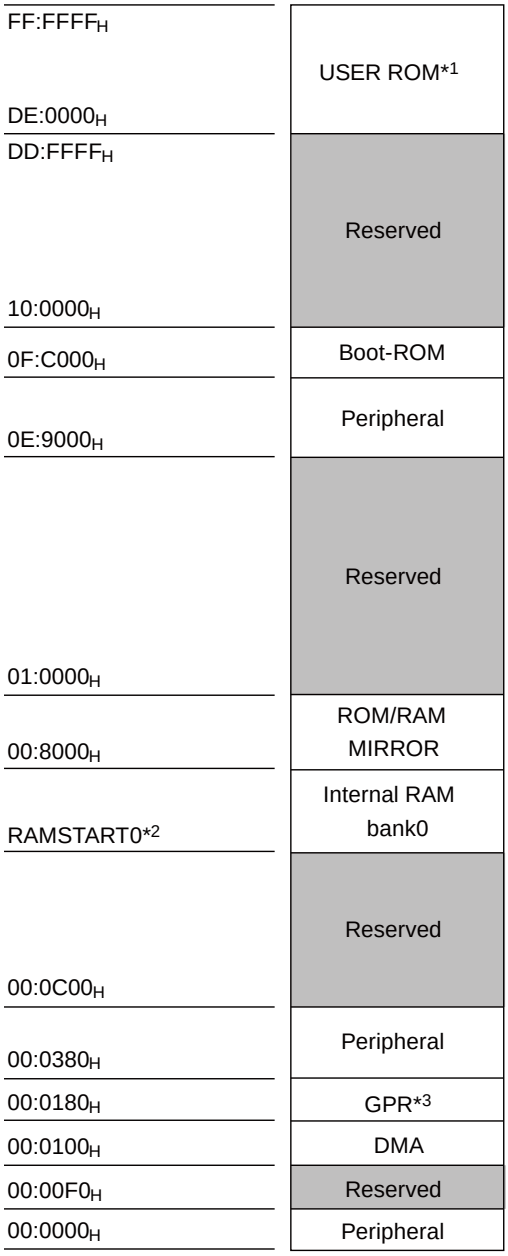
1. Product Lineup

Features			MB96650	Remark
Product Type			Flash Memory Product	
Subclock			Subclock can be set by software	
Dual Operation Flash Memory		RAM	-	
64.5KB + 32KB		10KB	MB96F653R, MB96F653A	Product Options R: MCU with CAN A: MCU without CAN
128.5KB + 32KB		16KB	MB96F655R, MB96F655A	
256.5KB + 32KB		24KB	MB96F656R	
384.5KB + 32KB		28KB	MB96F657R	
Package			LQFP-120: LQM120	
DMA			4ch	
USART			6ch	LIN-USART 0 to 2/4/5/7
	with automatic LIN-Header transmission/reception		Yes (only 1ch)	LIN-USART 0
	with 16 byte RX- and TX-FIFO		No	
I^2C			2ch	I^2C 0/1
8/10-bit A/D Converter			29ch	AN 0 to 28
	with Data Buffer		No	
	with Range Comparator		Yes	
	with Scan Disable		Yes	
	with ADC Pulse Detection		No	
16-bit Reload Timer (RLT)			5ch	RLT 0 to 3/6
16-bit Free-Running Timer (FRT)			3ch	FRT 0 to 2
16-bit Input Capture Unit (ICU)			7ch (1 channel for LIN-USART)	ICU 0/1/4 to 7/9 ICU 9 for LIN-USART
16-bit Output Compare Unit (OCU)			7ch	OCU 0 to 4/6/7 (OCU 4 for FRT clear)
8/16-bit Programmable Pulse Generator (PPG)			16ch (16-bit) / 32ch (8-bit)	PPG 0 to 15
	with Timing point capture		Yes	
	with Start delay		Yes	
	with Ramp		No	
Quadrature Position/Revolution Counter (QPRC)			2ch	QPRC 0/1
CAN Interface			1ch	CAN 0 32 Message Buffers
External Interrupts (INT)			16ch	INT 0 to 15
Non-Maskable Interrupt (NMI)			1ch	
Real Time Clock (RTC)			1ch	
I/O Ports			99 (Dual clock mode) 101 (Single clock mode)	
Clock Calibration Unit (CAL)			1ch	
Clock Output Function			2ch	
Low Voltage Detection Function			Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer			Yes	
On-chip RC-oscillator			Yes	
On-chip Debugger			Yes	

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.
It is necessary to use the port relocate function of the general I/O port according to your function use.

Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: ■Feedback resistor = approx. 5.0MΩ ■GPIO functionality selectable (CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)
C		CMOS hysteresis input pin

7. Memory Map



*1: For details about USER ROM area, see "USER ROM MEMORY MAP FOR FLASH DEVICES" on the following pages.

*2: For RAMSTART addresses, see the table on the next page.

*3: Unused GPR banks can be used as RAM area.
GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
121	218_H	-	-	121	Reserved
122	214_H	-	-	122	Reserved
123	210_H	-	-	123	Reserved
124	$20C_H$	-	-	124	Reserved
125	208_H	-	-	125	Reserved
126	204_H	-	-	126	Reserved
127	200_H	-	-	127	Reserved
128	$1FC_H$	-	-	128	Reserved
129	$1F8_H$	-	-	129	Reserved
130	$1F4_H$	-	-	130	Reserved
131	$1F0_H$	-	-	131	Reserved
132	$1EC_H$	-	-	132	Reserved
133	$1E8_H$	FLASHA	Yes	133	Flash memory A interrupt
134	$1E4_H$	-	-	134	Reserved
135	$1E0_H$	-	-	135	Reserved
136	$1DC_H$	-	-	136	Reserved
137	$1D8_H$	QPRC0	Yes	137	Quad Position/Revolution counter 0
138	$1D4_H$	QPRC1	Yes	138	Quad Position/Revolution counter 1
139	$1D0_H$	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	$1CC_H$	-	-	140	Reserved
141	$1C8_H$	-	-	141	Reserved
142	$1C4_H$	-	-	142	Reserved
143	$1C0_H$	-	-	143	Reserved

14.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	C_S	0.5	1.0 to 3.9	4.7	µF	1.0µF (Allowance within ± 50%) 3.9µF (Allowance within ± 20%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V_{CC} must use the one of a capacity value that is larger than C_S.

WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Stop mode*3	I_{CCH}	Vcc	-	-	20	60	µA	T_A = +25°C
				-	-	880	µA	T_A = +105°C
				-	-	1845	µA	T_A = +125°C
Flash Power Down current	$I_{CCFLASHPD}$		-	-	36	70	µA	
Power supply current for active Low Voltage detector*4	I_{CCLVD}		Low voltage detector enabled	-	5	-	µA	T_A = +25°C
				-	-	12.5	µA	T_A = +125°C
Flash Write/ Erase current*5	$I_{CCFLASH}$		-	-	12.5	-	mA	T_A = +25°C
				-	-	20	mA	T_A = +125°C

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

*2: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

*3: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

*4: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

*5: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

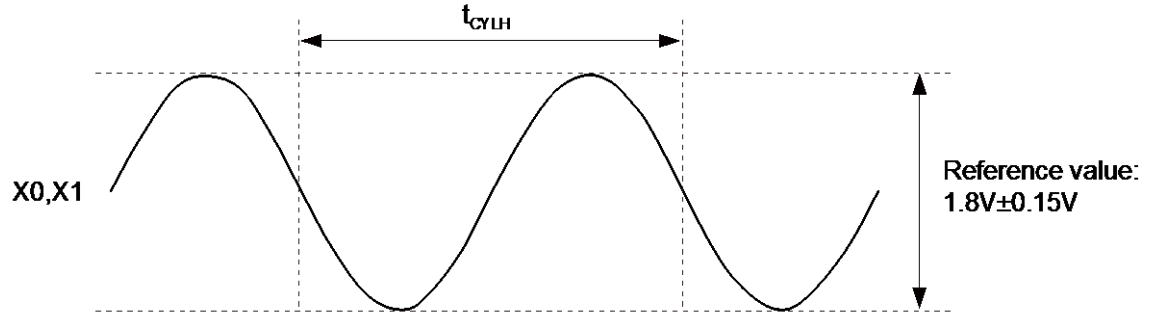
14.4 AC Characteristics

14.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, VD=1.8V±0.15V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

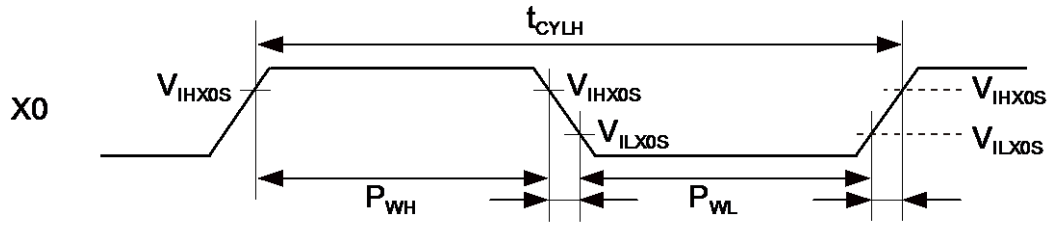
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_C	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	8	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL off
			4	-	8	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL on
Input clock cycle	t_{CYLH}	-	125	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	55	-	-	ns	

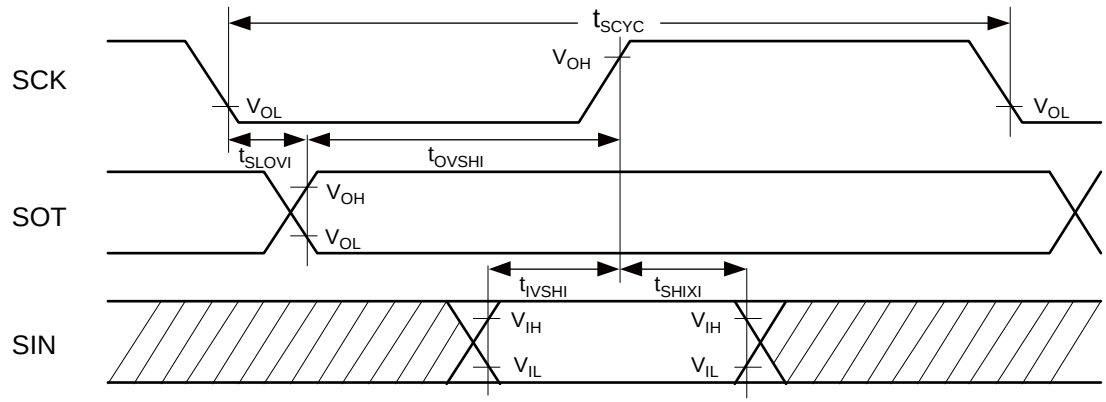
When using the crystal oscillator



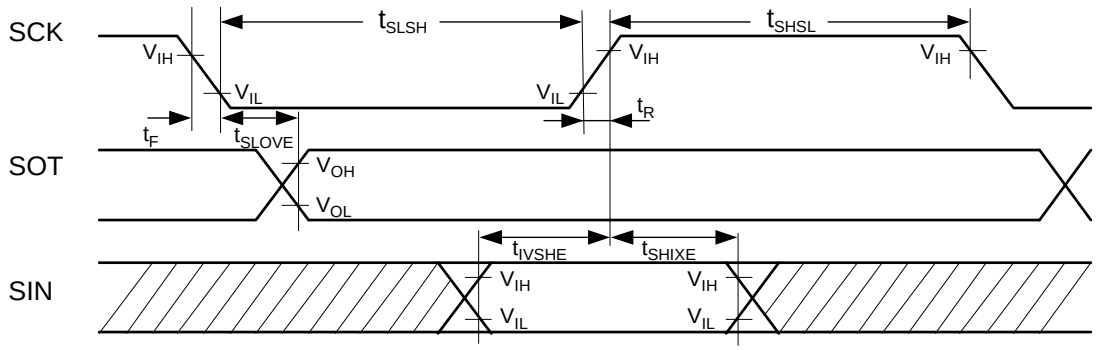
The amplitude changes by resistance, capacity which added outside or the difference of the device.

When using the external clock





Internal shift clock mode



External shift clock mode

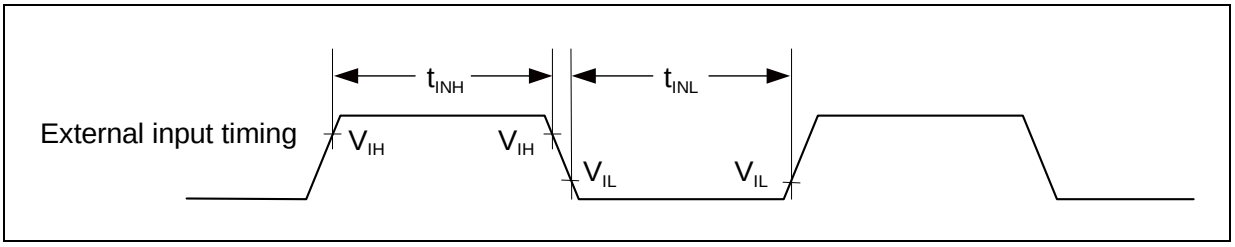
-

14.4.9 External Input Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH}, t_{INL}	Pnn_m	$2t_{CLKP1}$ +200 (t_{CLKP1}= $1/f_{CLKP1}$)*	-	ns	General Purpose I/O
		ADTG				A/D Converter trigger input
		TINn, TINn_R				Reload Timer
		TTGn				PPG trigger input
		FRCKn, FRCKn_R				Free-Running Timer input clock
		INn, INn_R				Input Capture
		AINn, BINn, ZINn				Quadrature Position/Revolution Counter
		INTn, INTn_R	200	-	ns	External Interrupt
		NMI				Non-Maskable Interrupt

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



14.4.10 I²C Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	C_L = 50pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs
Bus free time between "STOP condition" and "START condition"	t_{BUS}		4.7	-	1.3	-	µs
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	-	0	(1-1.5) × t_{CLKP1}*5	0	(1-1.5) × t_{CLKP1}*5	ns

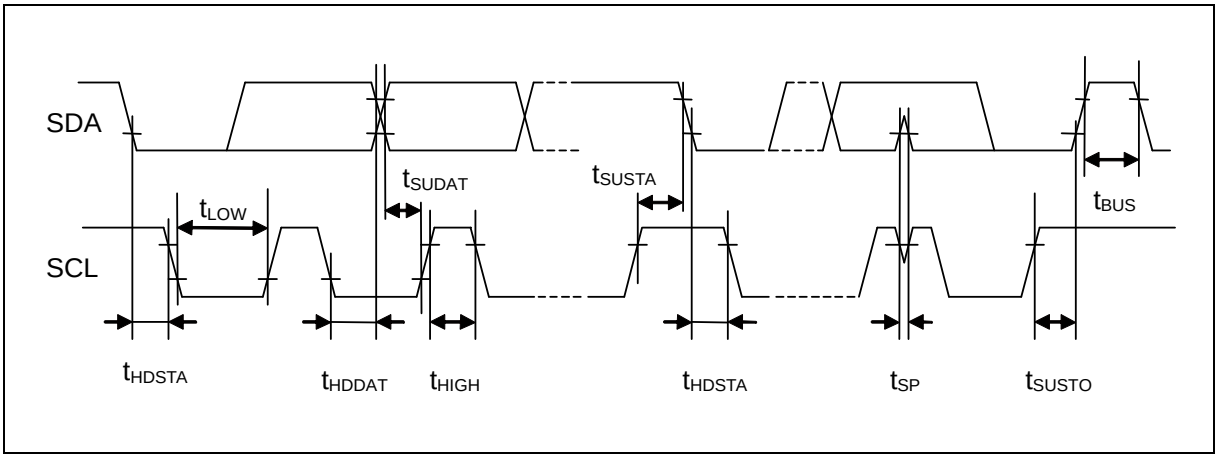
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250ns".

*4: For use at over 100kHz, set the peripheral clock1 (CLKP1) to at least 6MHz.

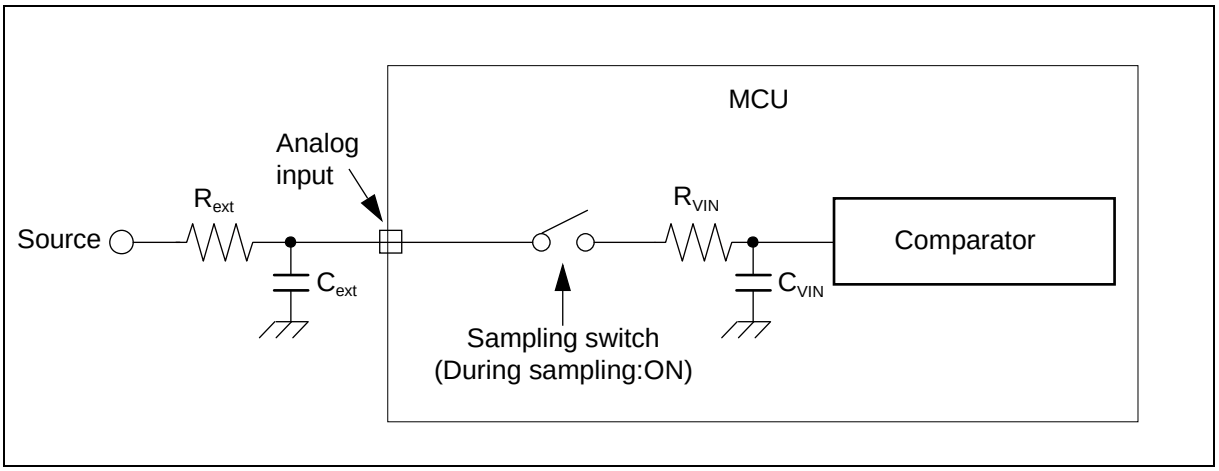
*5: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time.



14.5.2 Accuracy and Setting of the A/D Converter Sampling Time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (Tsamp) depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



R_{ext}: External driving impedance

C_{ext}: Capacitance of PCB at A/D converter input

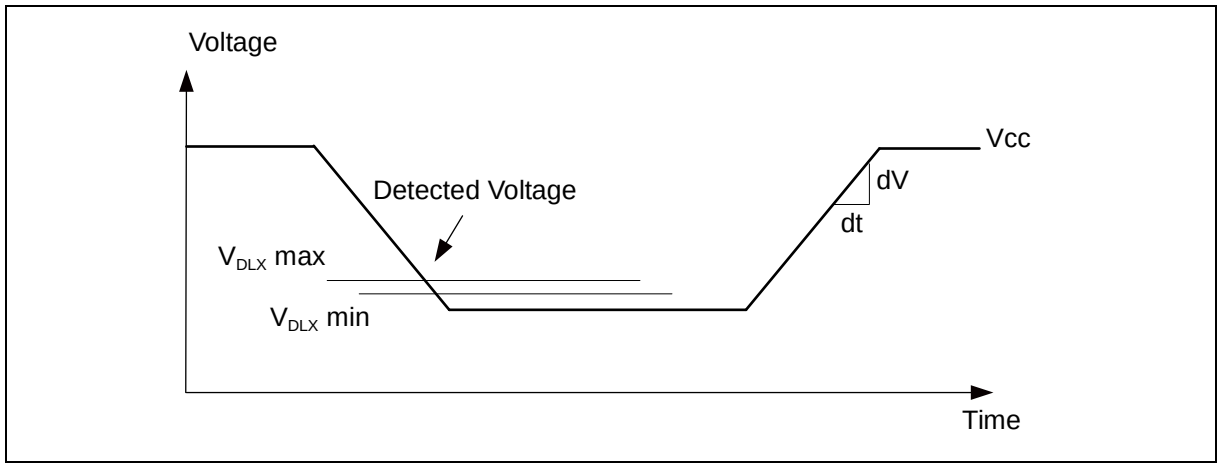
C_{VIN}: Analog input capacity (I/O, analog switch and ADC are contained)

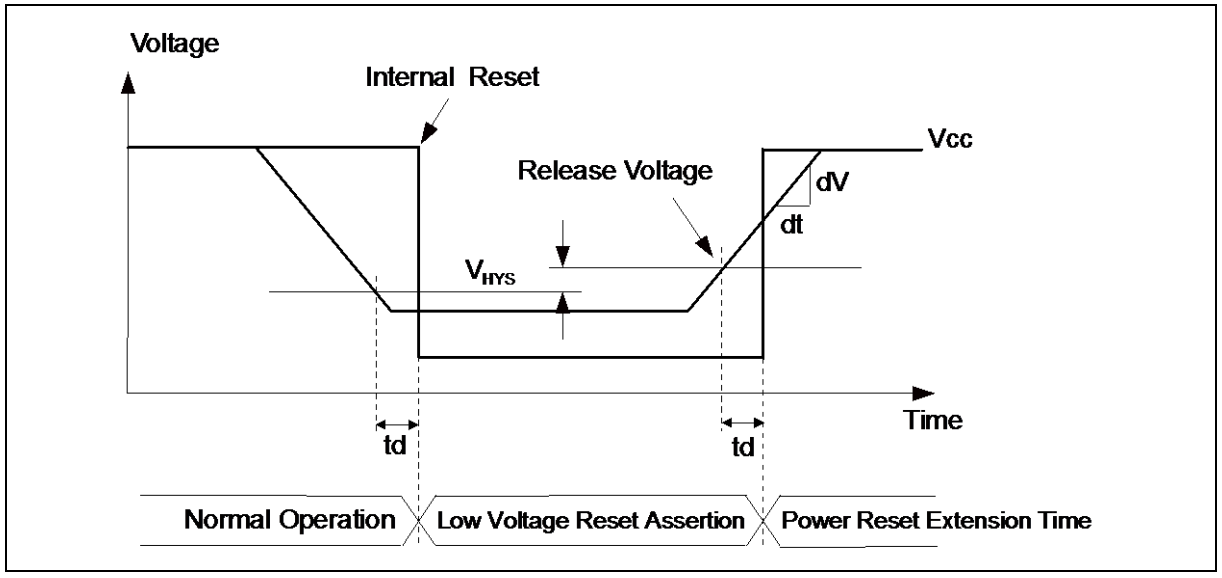
R_{VIN}: Analog input impedance (I/O, analog switch and ADC are contained)

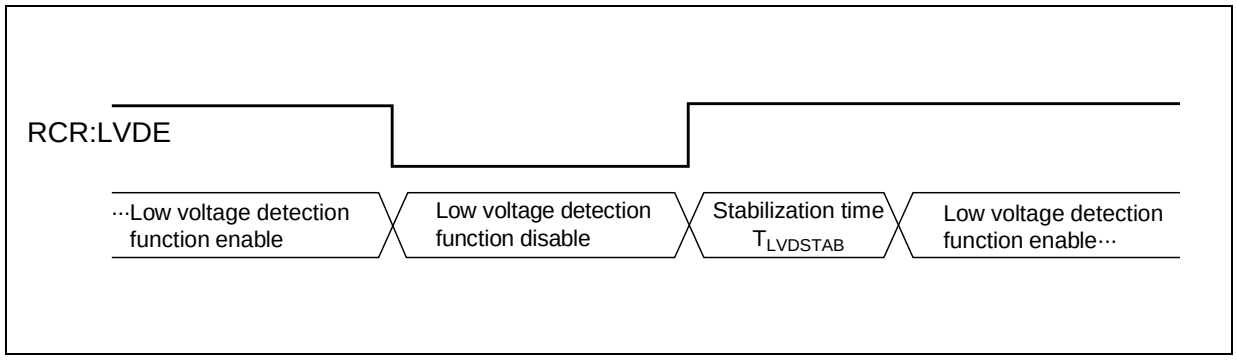
The following approximation formula for the replacement model above can be used:

$$Tsamp = 7.62 \times (Rext \times Cext + (Rext + R_{VIN}) \times C_{VIN})$$

- Do not select a sampling time below the absolute minimum permitted value. (0.5µs for $4.5V \le AV_{CC} \le 5.5V$, 1.2µs for $2.7V \le AV_{CC} < 4.5V$)
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1µF to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as |AVRH - AVRL| becomes smaller.


Voltage
Vcc
Detected Voltage
dV
dt
V_{DLX} max
V_{DLX} min
Time


Voltage
Internal Reset
Vcc
Release Voltage
dV
dt
V_{HYS}
Time
td
td
Normal Operation
Low Voltage Reset Assertion
Power Reset Extension Time


RCR:LVDE
···Low voltage detection function enable
Low voltage detection function disable
Stabilization time $T_{LVDSTAB}$
Low voltage detection function enable···

14.7 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	$T_A \leq$ + 105°C	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	$T_A \leq$ + 105°C	-	25	400	µs	Not including system-level overhead time.
	Small Sector	-	-	25	400	µs	
Chip erase time		$T_A \leq$ + 105°C	-	11.51	55.05	s	Includes write time prior to internal erase.

Note: While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.
To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})*1.

Write/Erase cycles and data hold time

Write/Erase cycles (cycle)	Data hold time (year)
1,000	20 *2
10,000	10 *2
100,000	5 *2

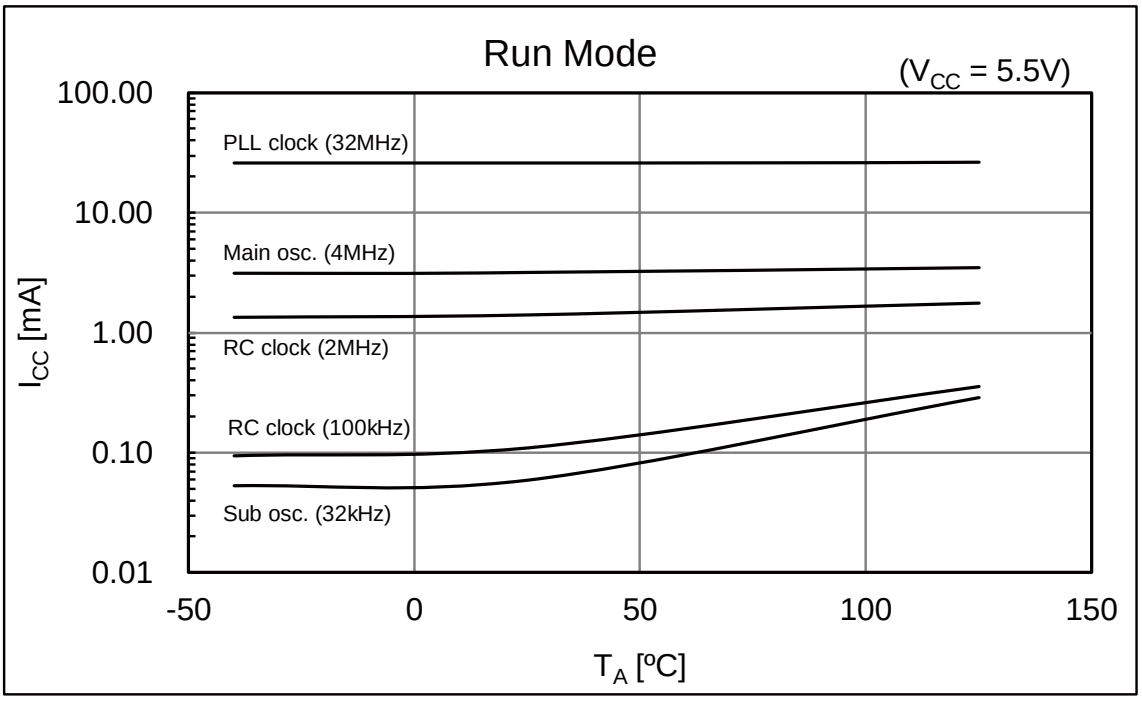
*1: See "6. Low Voltage Detection Function Characteristics".

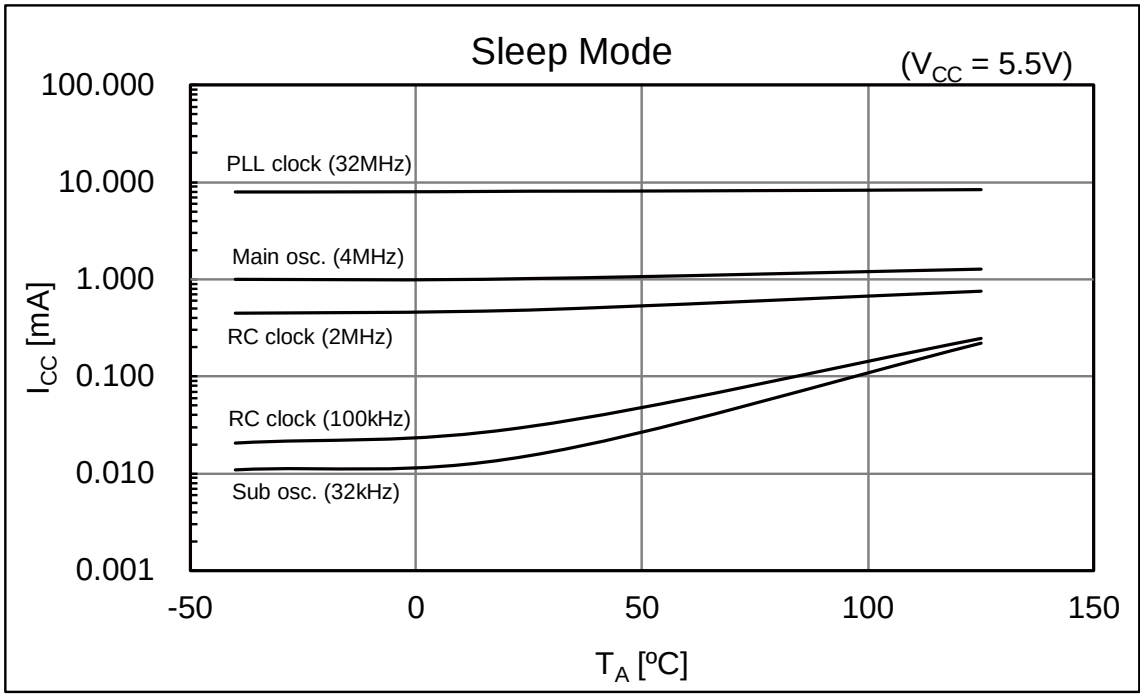
*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

15. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

■MB96F657





■Used setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

18. Major Changes

Spansion Publication Number: MB96650_DS704-00003

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
39	Electrical Characteristics DC Characteristics Current Rating	Changed the Value of “Power supply current in Timer modes” I_{CCTPLL} Typ: 2485µA → 1800µA (T_A = +25°C) Max: 2715µA → 2250µA (T_A = +25°C) Max: 4095µA → 3220µA (T_A = +105°C) Max: 5065µA → 4205µA (T_A = +125°C)
Revision 2.1		
-	-	Company name and layout design change

NOTE: Please see “Document History” about later revised information.

Page	Section	Change Results
Revision *B		
5, 7, 62, 63	1. Product Lineup 3. Pin Assignment 16. Ordering Information 17. Package Dimension	Package description modified to JEDEC description. FPT-120P-M21 → LQM120

Document History

Document Title: MB96650 Series, F2MC-16FX 16-bit Microcontroller
Document Number: 002-04707

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	KSUN	01/31/2014	Migrated to Cypress and assigned document number 002-04707. No change to document contents or format.
*A	5164895	KSUN	03/14/2016	Updated to Cypress template
*B	6005555	KSUN	01/09/2018	Updated the Cypress logo, Sales information and legal. Refer to 18. Major Changes.