Infineon Technologies - MB96F655ABPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	101
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 29x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f655abpmc-gse2

MB96650 Series

F²MC-16FX 16-bit Microcontroller

MB96650 series is based on Cypress's advanced F²MC-16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established F²MC-16LX family thus allowing for easy migration of F²MC-16LX Software to the new F²MC-16FX products. F²MC-16FX product improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time. For high processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 32MHz operation frequency from an external 4MHz to 8MHz resonator. The result is a minimum instruction cycle time of 31.2ns going together with excellent EMI behavior. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows selecting suitable operation frequencies for peripheral resources independent of the CPU speed.

Features

Technology

0.18µm CMOS

CPU

- F²MC-16FX CPU
- Optimized instruction set for controller applications (bit, byte, word and long-word data types, 23 different addressing modes, barrel shift, variety of pointers)
- 8-byte instruction queue
- Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available

System clock

- On-chip PLL clock multiplier (×1 to ×8, ×1 when PLL stop)
- 4MHz to 8MHz crystal oscillator (maximum frequency when using ceramic resonator depends on Q-factor)
- Up to 8MHz external clock for devices with fast clock input feature
- 32.768kHz subsystem quartz clock
- 100kHz/2MHz internal RC clock for quick and safe startup, clock stop detection function, watchdog
- Clock source selectable from mainclock oscillator, subclock oscillator and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals
- The subclock oscillator is enabled by the Boot ROM program controlled by a configuration marker after a Power or External reset
- Low Power Consumption - 13 operating modes (different Run, Sleep, Timer, Stop modes)

On-chip voltage regulator

Internal voltage regulator supports a wide MCU supply voltage range (Min=2.7V), offering low power consumption

Low voltage detection function

Reset is generated when supply voltage falls below programmable reference voltage

Code Security

Protects Flash Memory content from unintended read-out

DMA

Automatic transfer function independent of CPU, can be assigned freely to resources

Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1Mbps
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

USART

- Full duplex USARTs (SCI/LIN)

Non Maskable Interrupt

- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, can not be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

I/O Ports

- Most of the external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I^2C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GPIO-pin (either Automotive or CMOS hysteresis)
- Bit-wise programmable pull-up resistor

Built-in On Chip Debugger (OCD)

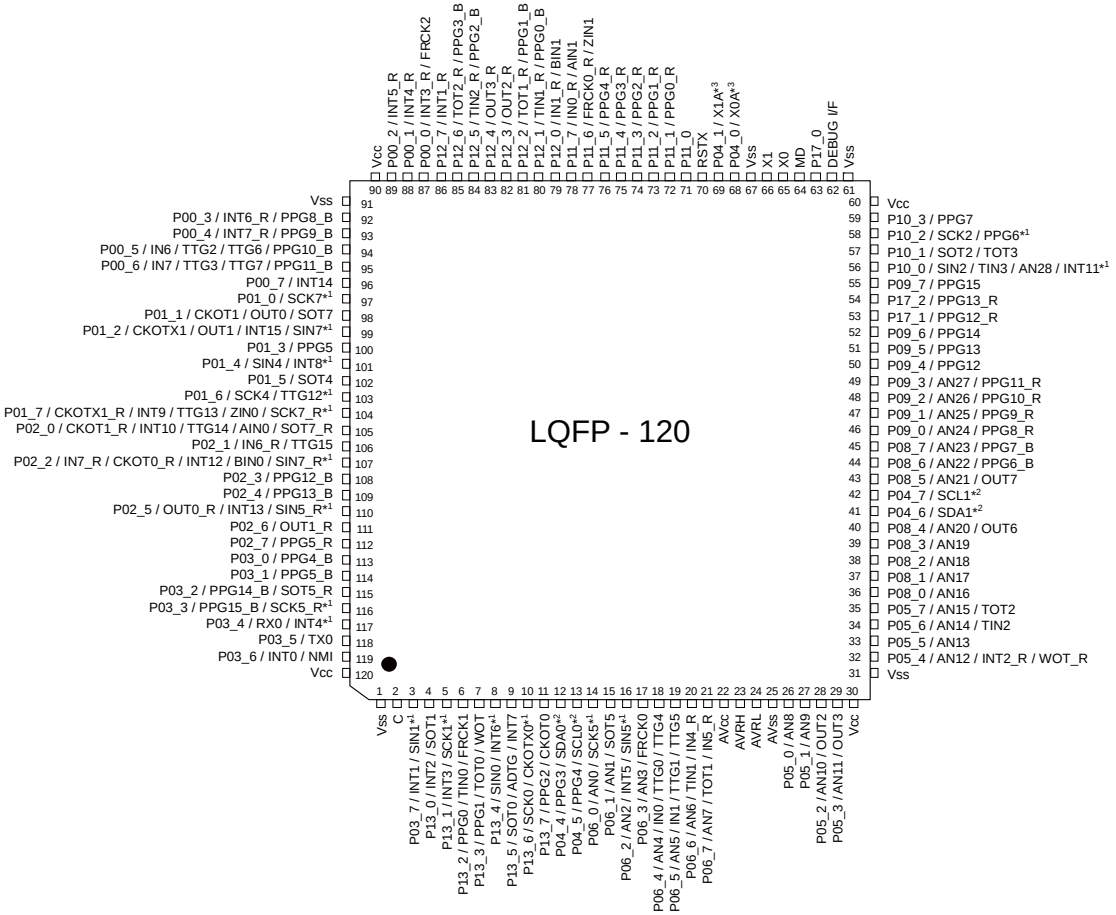
- One-wire debug tool interface
- Break function:
  - Hardware break: 6 points (shared with code event)
  - -Software break: 4096 points
- Event function
  - Code event: 6 points (shared with hardware break)
  - -Data event: 6 points
  - Event sequencer: 2 levels + reset
- Execution time measurement function
- Trace function: 42 branches
- Security function

Flash Memory

- Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
- Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the automatic algorithm
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase or write

3. Pin Assignment

(Top view)



(LQM120)

*1: CMOS input level only

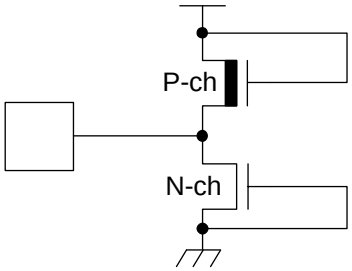
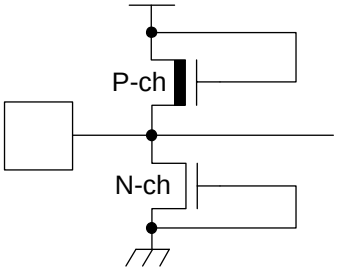
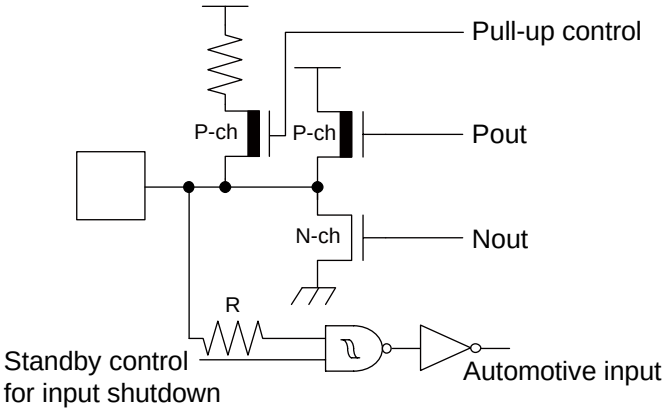
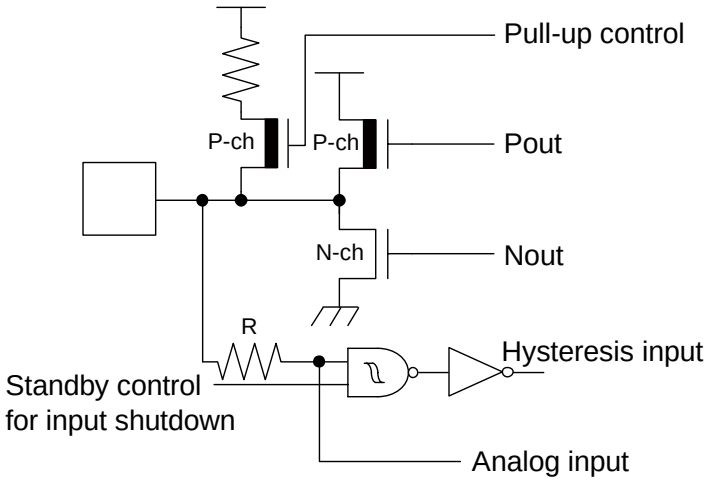
*2: CMOS input level only for I^2C

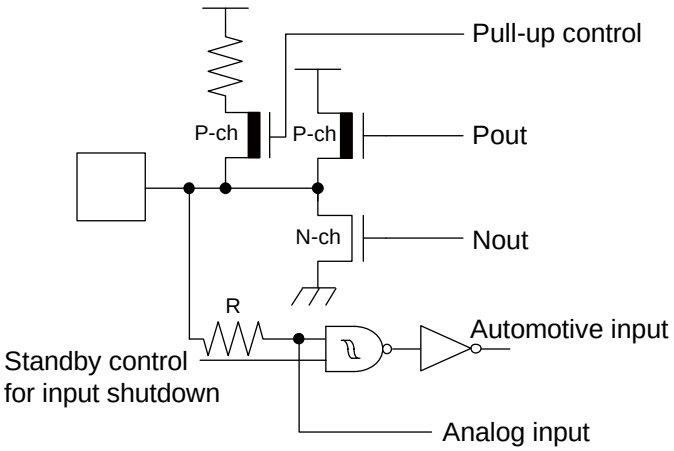
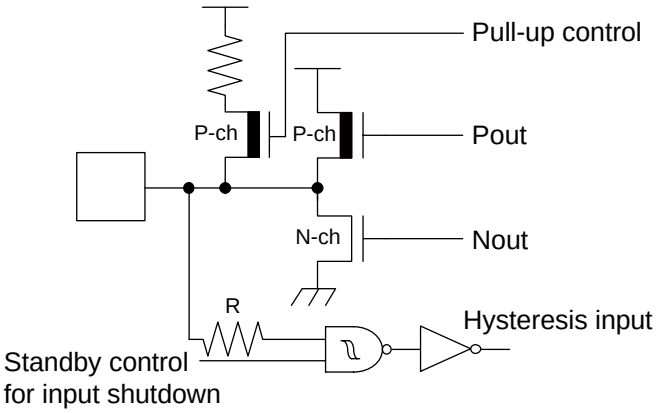
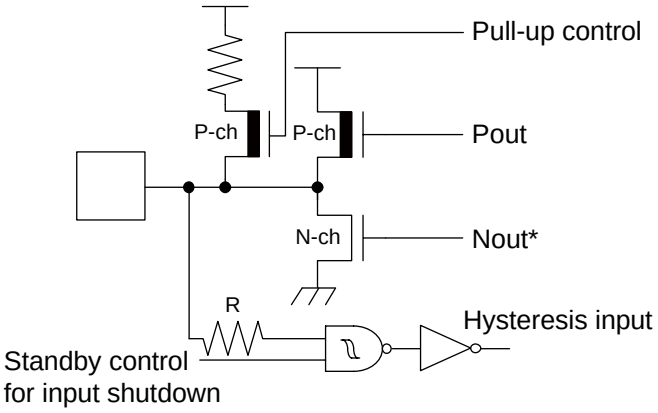
*3: Please set ROM Configuration Block (RCB) to use the subclock.

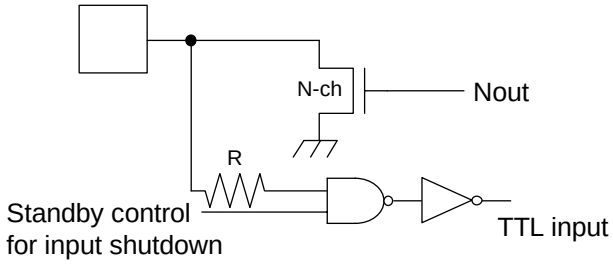
Other than those above, general-purpose pins have only Automotive input level.

Pin no.	I/O circuit type*	Pin name
115	H	P03_2 / PPG14_B / SOT5_R
116	M	P03_3 / PPG15_B / SCK5_R
117	M	P03_4 / RX0 / INT4
118	H	P03_5 / TX0
119	H	P03_6 / INT0 / NMI
120	Supply	Vcc

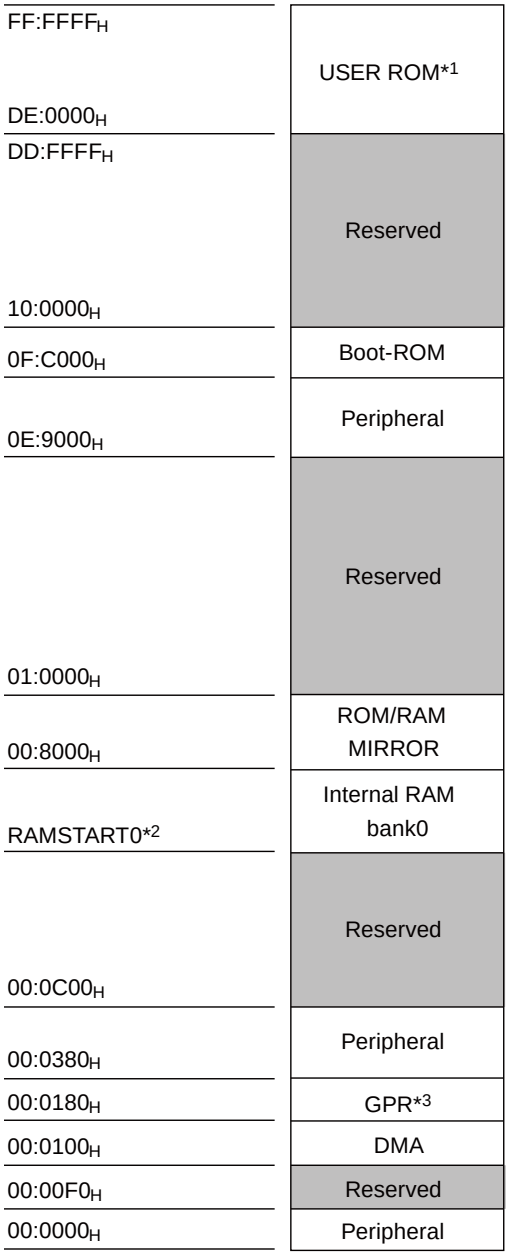
*: See “ I/O circuit type” for details on the I/O circuit types.

Type	Circuit	Remarks
F		Power supply input protection circuit
G		■A/D converter ref+ (AVRH)/ ref- (AVRL) power supply input pin with protection circuit ■Without protection circuit against V_{CC} for pins AVRH/AVRL
H		■CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■Automotive input with input shutdown function ■Programmable pull-up resistor
I		■CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■CMOS hysteresis input with input shutdown function ■Programmable pull-up resistor ■Analog input

Type	Circuit	Remarks
K		■CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■Automotive input with input shutdown function ■Programmable pull-up resistor ■Analog input
M		■CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■CMOS hysteresis input with input shutdown function ■Programmable pull-up resistor
N		■CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) ■CMOS hysteresis input with input shutdown function ■Programmable pull-up resistor *: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage.

Type	Circuit	Remarks
O		■Open-drain I/O ■Output 25mA, Vcc = 2.7V ■TTL input

7. Memory Map



*1: For details about USER ROM area, see "USER ROM MEMORY MAP FOR FLASH DEVICES" on the following pages.

*2: For RAMSTART addresses, see the table on the next page.

*3: Unused GPR banks can be used as RAM area.
GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

9. User ROM Memory Map for Flash Devices

CPU mode address	Flash memory mode address	MB96F653 Flash size 64.5KB + 32KB	MB96F655 Flash size 128.5KB + 32KB	MB96F656 Flash size 256.5KB + 32KB	MB96F657 Flash size 384.5KB + 32KB	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	Reserved	SA38 - 64KB	SA38 - 64KB	SA38 - 64KB	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$		Reserved	SA37 - 64KB	SA37 - 64KB	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$			SA36 - 64KB	SA36 - 64KB	
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$			Reserved	SA35 - 64KB	
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$				SA34 - 64KB	
F9:FFFF$_H$ DF:A000$_H$					Reserved	
DF:9FFF$_H$ DF:8000$_H$	1F:9FFF$_H$ 1F:8000$_H$	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	Bank B of Flash A
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SAS - 512B*	SAS - 512B*	SAS - 512B*	SAS - 512B*	Bank A of Flash A
DE:FFFF$_H$ DE:0000$_H$		Reserved	Reserved	Reserved	Reserved	

*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for E^{2}PROM emulation.

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

MB96650		
Pin Number	**USART Number**	**Normal Function**
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
56	USART2	SIN2
57		SOT2
58		SCK2
101	USART4	SIN4
102		SOT4
103		SCK4

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
40	$35C_H$	PPG2	Yes	40	Programmable Pulse Generator 2
41	358_H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354_H	PPG4	Yes	42	Programmable Pulse Generator 4
43	350_H	PPG5	Yes	43	Programmable Pulse Generator 5
44	$34C_H$	PPG6	Yes	44	Programmable Pulse Generator 6
45	348_H	PPG7	Yes	45	Programmable Pulse Generator 7
46	344_H	PPG8	Yes	46	Programmable Pulse Generator 8
47	340_H	PPG9	Yes	47	Programmable Pulse Generator 9
48	$33C_H$	PPG10	Yes	48	Programmable Pulse Generator 10
49	338_H	PPG11	Yes	49	Programmable Pulse Generator 11
50	334_H	PPG12	Yes	50	Programmable Pulse Generator 12
51	330_H	PPG13	Yes	51	Programmable Pulse Generator 13
52	$32C_H$	PPG14	Yes	52	Programmable Pulse Generator 14
53	328_H	PPG15	Yes	53	Programmable Pulse Generator 15
54	324_H	-	-	54	Reserved
55	320_H	-	-	55	Reserved
56	$31C_H$	-	-	56	Reserved
57	318_H	-	-	57	Reserved
58	314_H	RLT0	Yes	58	Reload Timer 0
59	310_H	RLT1	Yes	59	Reload Timer 1
60	$30C_H$	RLT2	Yes	60	Reload Timer 2
61	308_H	RLT3	Yes	61	Reload Timer 3
62	304_H	-	-	62	Reserved
63	300_H	-	-	63	Reserved
64	$2FC_H$	RLT6	Yes	64	Reload Timer 6
65	$2F8_H$	ICU0	Yes	65	Input Capture Unit 0
66	$2F4_H$	ICU1	Yes	66	Input Capture Unit 1
67	$2F0_H$	-	-	67	Reserved
68	$2EC_H$	-	-	68	Reserved
69	$2E8_H$	ICU4	Yes	69	Input Capture Unit 4
70	$2E4_H$	ICU5	Yes	70	Input Capture Unit 5
71	$2E0_H$	ICU6	Yes	71	Input Capture Unit 6
72	$2DC_H$	ICU7	Yes	72	Input Capture Unit 7
73	$2D8_H$	-	-	73	Reserved
74	$2D4_H$	ICU9	Yes	74	Input Capture Unit 9
75	$2D0_H$	-	-	75	Reserved
76	$2CC_H$	-	-	76	Reserved
77	$2C8_H$	OCU0	Yes	77	Output Compare Unit 0
78	$2C4_H$	OCU1	Yes	78	Output Compare Unit 1
79	$2C0_H$	OCU2	Yes	79	Output Compare Unit 2
80	$2BC_H$	OCU3	Yes	80	Output Compare Unit 3

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
121	218_H	-	-	121	Reserved
122	214_H	-	-	122	Reserved
123	210_H	-	-	123	Reserved
124	$20C_H$	-	-	124	Reserved
125	208_H	-	-	125	Reserved
126	204_H	-	-	126	Reserved
127	200_H	-	-	127	Reserved
128	$1FC_H$	-	-	128	Reserved
129	$1F8_H$	-	-	129	Reserved
130	$1F4_H$	-	-	130	Reserved
131	$1F0_H$	-	-	131	Reserved
132	$1EC_H$	-	-	132	Reserved
133	$1E8_H$	FLASHA	Yes	133	Flash memory A interrupt
134	$1E4_H$	-	-	134	Reserved
135	$1E0_H$	-	-	135	Reserved
136	$1DC_H$	-	-	136	Reserved
137	$1D8_H$	QPRC0	Yes	137	Quad Position/Revolution counter 0
138	$1D4_H$	QPRC1	Yes	138	Quad Position/Revolution counter 1
139	$1D0_H$	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	$1CC_H$	-	-	140	Reserved
141	$1C8_H$	-	-	141	Reserved
142	$1C4_H$	-	-	142	Reserved
143	$1C0_H$	-	-	143	Reserved

12. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

12.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

■Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

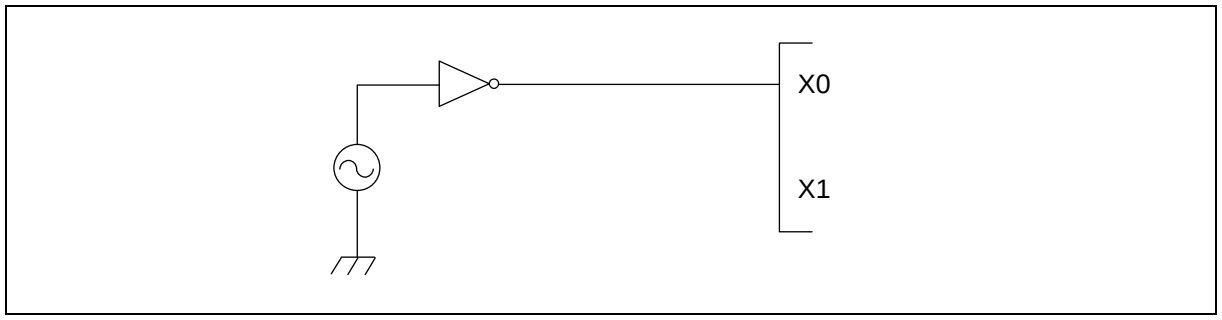
3. External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration.

See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

(1) Single phase external clock for Main oscillator

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open. And supply 1.8V power to the external clock.

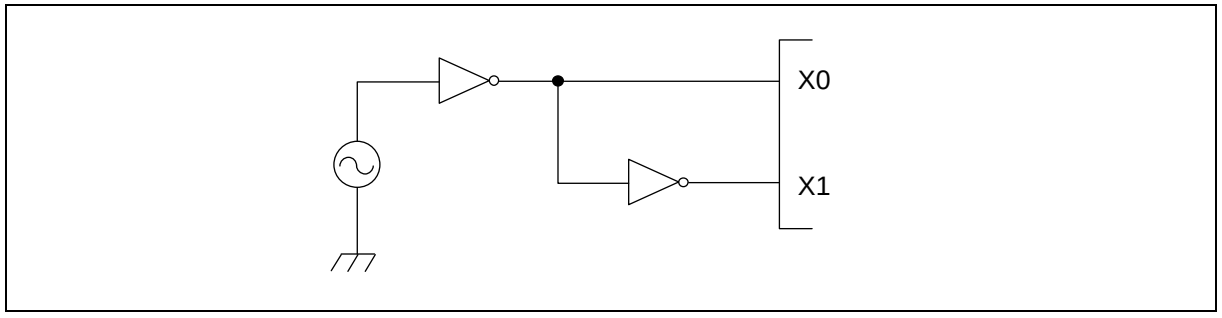


(2) Single phase external clock for Sub oscillator

When using a single phase external clock for the Sub oscillator, “External clock mode” must be selected and X0A/P04_0 pin must be driven. X1A/P04_1 pin can be configured as GPIO.

(3) Opposite phase external clock

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.



4. Notes on PLL clock mode operation

If the microcontroller is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

5. Power supply pins (Vcc/Vss)

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

Vcc and Vss pins must be connected to the device from the power supply with lowest possible impedance.

The smoothing capacitor at Vcc pin must use the one of a capacity value that is larger than Cs.

Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1μF between Vcc and Vss pins as close as possible to Vcc and Vss pins.

6. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

7. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed AV_{CC} . Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

8. Pin handling when not using the A/D converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH =AVRL = V_{SS}.

9. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

10. Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

11. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

12. Mode Pin (MD)

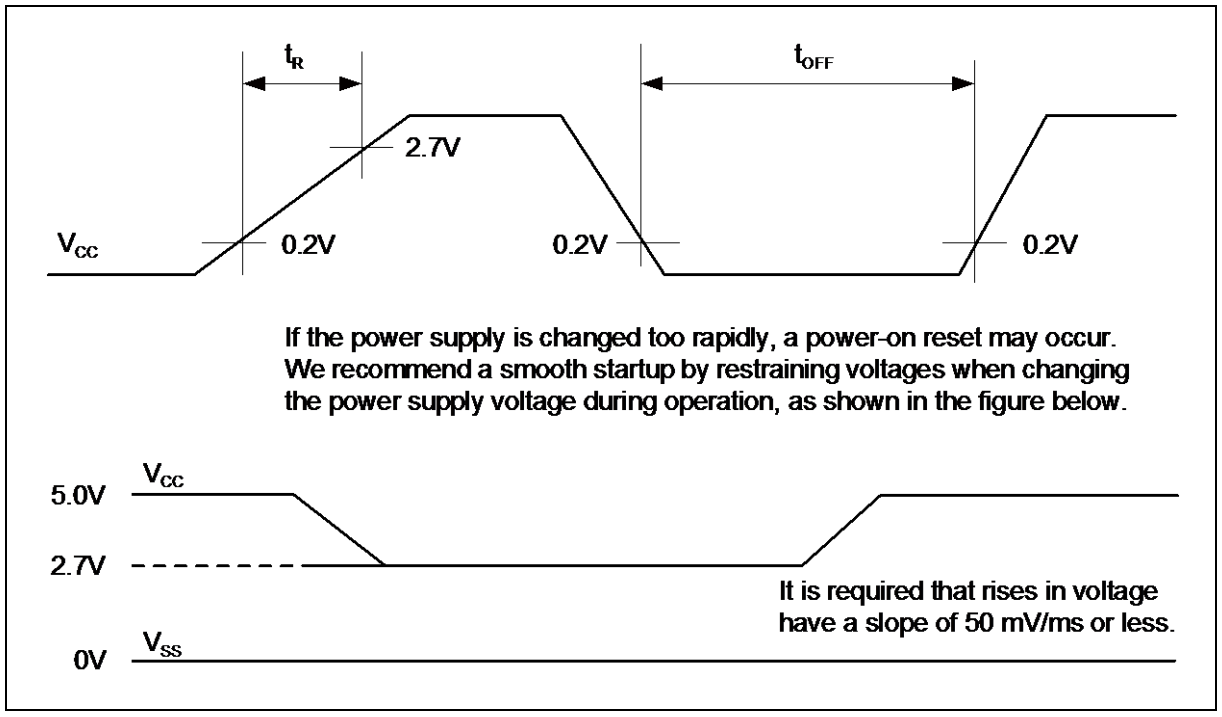
Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to Vcc or Vss pin and provide a low-impedance connection.

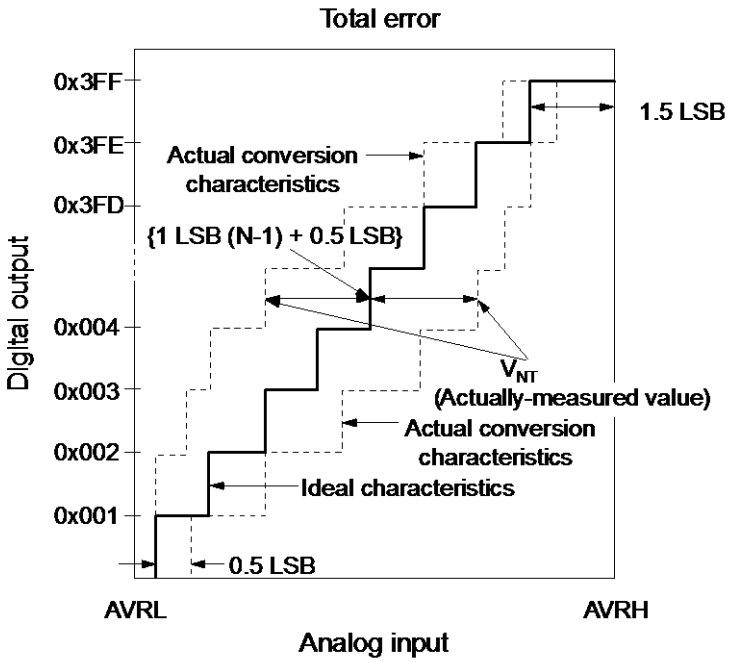
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH4}	4mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OH} = -4mA$ $2.7V \le V_{CC} < 4.5V$ $I_{OH} = -1.5mA$	V_{CC} - 0.5	-	V_{CC}	V	
	V_{OH3}	3mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OH} = -3mA$ $2.7V \le V_{CC} < 4.5V$ $I_{OH} = -1.5mA$	V_{CC} - 0.5	-	V_{CC}	V	
"L" level output voltage	V_{OL4}	4mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OL} = +4mA$ $2.7V \le V_{CC} < 4.5V$ $I_{OL} = +1.7mA$	-	-	0.4	V	
	V_{OL3}	3mA type	$2.7V \le V_{CC} < 5.5V$ $I_{OL} = +3mA$	-	-	0.4	V	
	V_{OLD}	DEBUG I/F	$V_{CC} = 2.7V$ $I_{OL} = +25mA$	0	-	0.25	V	
Input leak current	I_{IL}	Pnn_m	$V_{SS} < V_I < V_{CC}$ AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	- 1	-	+ 1	µA	
Pull-up resistance value	R_{PU}	Pnn_m	$V_{CC} = 5.0V \pm 10\%$	25	50	100	kΩ	
Input capacitance	C_{IN}	Other than C, Vcc, Vss, AVcc, AVss, AVRH, AVRL	-	-	5	15	pF	

14.4.7 Power-on Reset Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	Vcc	0.05	-	30	ms
Power off time	t_{OFF}	Vcc	1	-	-	ms





$$1LSB\ (Ideal\ value) = \frac{AVRH - AVRL}{1024}\ [V]$$

$$Total\ error\ of\ digital\ output\ N = \frac{V_{NT} - \{1LSB \times (N - 1) + 0.5LSB\}}{1LSB}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from 0x(N + 1) to 0xN.
V_{OT} (Ideal value) = AVRL + 0.5LSB[V]
V_{FST} (Ideal value) = AVRH - 1.5LSB[V]

14.7 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	$T_A \leq$ + 105°C	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	$T_A \leq$ + 105°C	-	25	400	µs	Not including system-level overhead time.
	Small Sector	-	-	25	400	µs	
Chip erase time		$T_A \leq$ + 105°C	-	11.51	55.05	s	Includes write time prior to internal erase.

Note: While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.
To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})*1.

Write/Erase cycles and data hold time

Write/Erase cycles (cycle)	Data hold time (year)
1,000	20 *2
10,000	10 *2
100,000	5 *2

*1: See "6. Low Voltage Detection Function Characteristics".

*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

18. Major Changes

Spansion Publication Number: MB96650_DS704-00003

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
39	Electrical Characteristics DC Characteristics Current Rating	Changed the Value of “Power supply current in Timer modes” I_{CCTPLL} Typ: 2485µA → 1800µA (T_A = +25°C) Max: 2715µA → 2250µA (T_A = +25°C) Max: 4095µA → 3220µA (T_A = +105°C) Max: 5065µA → 4205µA (T_A = +125°C)
Revision 2.1		
-	-	Company name and layout design change

NOTE: Please see “Document History” about later revised information.

Page	Section	Change Results
Revision *B		
5, 7, 62, 63	1. Product Lineup 3. Pin Assignment 16. Ordering Information 17. Package Dimension	Package description modified to JEDEC description. FPT-120P-M21 → LQM120