Infineon Technologies - MB96F657RBPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	101
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	28K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 29x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f657rbpmc-gse1

Non Maskable Interrupt

- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, can not be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

I/O Ports

- Most of the external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I^2C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GPIO-pin (either Automotive or CMOS hysteresis)
- Bit-wise programmable pull-up resistor

Built-in On Chip Debugger (OCD)

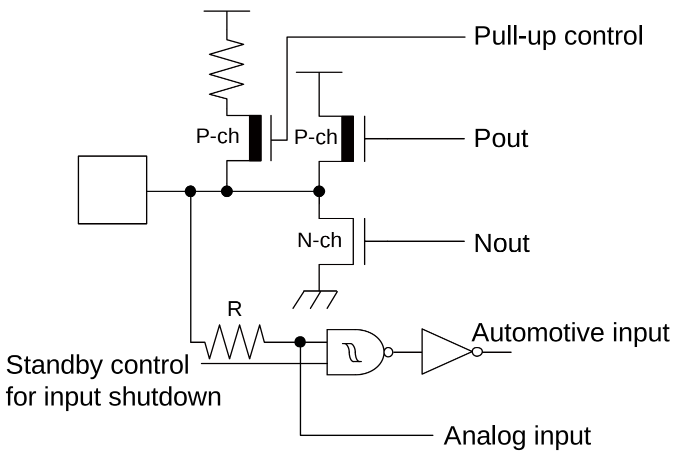
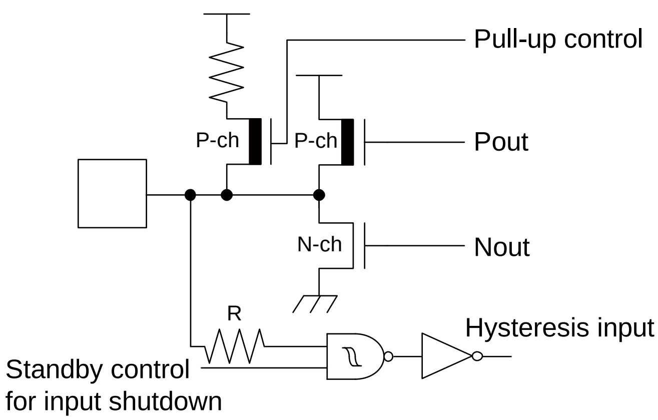
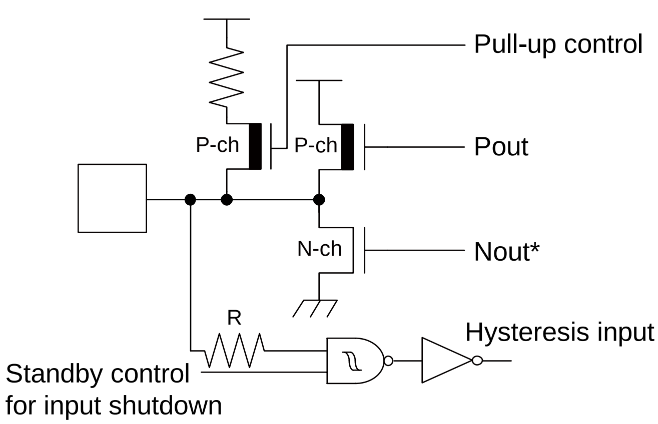
- One-wire debug tool interface
- Break function:
  - Hardware break: 6 points (shared with code event)
  - -Software break: 4096 points
- Event function
  - Code event: 6 points (shared with hardware break)
  - -Data event: 6 points
  - Event sequencer: 2 levels + reset
- Execution time measurement function
- Trace function: 42 branches
- Security function

Flash Memory

- Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
- Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the automatic algorithm
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase or write

5. Pin Circuit Type

Pin no.	I/O circuit type*	Pin name
1	Supply	Vss
2	F	C
3	M	P03_7 / INT1 / SIN1
4	H	P13_0 / INT2 / SOT1
5	M	P13_1 / INT3 / SCK1
6	H	P13_2 / PPG0 / TIN0 / FRCK1
7	H	P13_3 / PPG1 / TOT0 / WOT
8	M	P13_4 / SIN0 / INT6
9	H	P13_5 / SOT0 / ADTG / INT7
10	M	P13_6 / SCK0 / CKOTX0
11	H	P13_7 / PPG2 / CKOT0
12	N	P04_4 / PPG3 / SDA0
13	N	P04_5 / PPG4 / SCL0
14	I	P06_0 / AN0 / SCK5
15	K	P06_1 / AN1 / SOT5
16	I	P06_2 / AN2 / INT5 / SIN5
17	K	P06_3 / AN3 / FRCK0
18	K	P06_4 / AN4 / IN0 / TTG0 / TTG4
19	K	P06_5 / AN5 / IN1 / TTG1 / TTG5
20	K	P06_6 / AN6 / TIN1 / IN4_R
21	K	P06_7 / AN7 / TOT1 / IN5_R
22	Supply	AVcc
23	G	AVRH
24	G	AVRL
25	Supply	AVss
26	K	P05_0 / AN8
27	K	P05_1 / AN9
28	K	P05_2 / AN10 / OUT2
29	K	P05_3 / AN11 / OUT3
30	Supply	Vcc
31	Supply	Vss
32	K	P05_4 / AN12 / INT2_R / WOT_R
33	K	P05_5 / AN13
34	K	P05_6 / AN14 / TIN2
35	K	P05_7 / AN15 / TOT2
36	K	P08_0 / AN16

Type	Circuit	Remarks
K		■CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■Automotive input with input shutdown function ■Programmable pull-up resistor ■Analog input
M		■CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■CMOS hysteresis input with input shutdown function ■Programmable pull-up resistor
N		■CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) ■CMOS hysteresis input with input shutdown function ■Programmable pull-up resistor *: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage.

9. User ROM Memory Map for Flash Devices

CPU mode address	Flash memory mode address	MB96F653 Flash size 64.5KB + 32KB	MB96F655 Flash size 128.5KB + 32KB	MB96F656 Flash size 256.5KB + 32KB	MB96F657 Flash size 384.5KB + 32KB	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	Reserved	SA38 - 64KB	SA38 - 64KB	SA38 - 64KB	Bank A of Flash A
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$	Reserved	Reserved	SA37 - 64KB	SA37 - 64KB	Bank A of Flash A
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$	Reserved	Reserved	SA36 - 64KB	SA36 - 64KB	Bank A of Flash A
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$	Reserved	Reserved	Reserved	SA35 - 64KB	Bank A of Flash A
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$	Reserved	Reserved	Reserved	SA34 - 64KB	Bank A of Flash A
F9:FFFF$_H$ DF:A000$_H$		Reserved	Reserved	Reserved	Reserved	
DF:9FFF$_H$ DF:8000$_H$	1F:9FFF$_H$ 1F:8000$_H$	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	Bank B of Flash A
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	Bank B of Flash A
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	Bank B of Flash A
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	Bank B of Flash A
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SAS - 512B*	SAS - 512B*	SAS - 512B*	SAS - 512B*	Bank A of Flash A
DE:FFFF$_H$ DE:0000$_H$		Reserved	Reserved	Reserved	Reserved	

*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for E^2PROM emulation.

11. Interrupt Vector Table

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	$3FC_H$	CALLV0	No	-	CALLV instruction
1	$3F8_H$	CALLV1	No	-	CALLV instruction
2	$3F4_H$	CALLV2	No	-	CALLV instruction
3	$3F0_H$	CALLV3	No	-	CALLV instruction
4	$3EC_H$	CALLV4	No	-	CALLV instruction
5	$3E8_H$	CALLV5	No	-	CALLV instruction
6	$3E4_H$	CALLV6	No	-	CALLV instruction
7	$3E0_H$	CALLV7	No	-	CALLV instruction
8	$3DC_H$	RESET	No	-	Reset vector
9	$3D8_H$	INT9	No	-	INT9 instruction
10	$3D4_H$	EXCEPTION	No	-	Undefined instruction execution
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Clock Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	LVDI	No	16	Low Voltage Detector
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	EXTINT1	Yes	18	External Interrupt 1
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	EXTINT5	Yes	22	External Interrupt 5
23	$3A0_H$	EXTINT6	Yes	23	External Interrupt 6
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9
27	390_H	EXTINT10	Yes	27	External Interrupt 10
28	$38C_H$	EXTINT11	Yes	28	External Interrupt 11
29	388_H	EXTINT12	Yes	29	External Interrupt 12
30	384_H	EXTINT13	Yes	30	External Interrupt 13
31	380_H	EXTINT14	Yes	31	External Interrupt 14
32	$37C_H$	EXTINT15	Yes	32	External Interrupt 15
33	378_H	CAN0	No	33	CAN Controller 0
34	374_H	-	-	34	Reserved
35	370_H	-	-	35	Reserved
36	$36C_H$	-	-	36	Reserved
37	368_H	-	-	37	Reserved
38	364_H	PPG0	Yes	38	Programmable Pulse Generator 0
39	360_H	PPG1	Yes	39	Programmable Pulse Generator 1

12. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

12.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

■Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

12.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

■Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.

When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

Condition: 125°C/24 h

■Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

12.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. **Crystal oscillator and ceramic resonator circuit**
   Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

   It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

   It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

7. **Turn on sequence of power supply to A/D converter and analog inputs**
   It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

   It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed AV_{CC} . Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

8. **Pin handling when not using the A/D converter**
   If the A/D converter is not used, the power supply pins for A/D converter should be connected such as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH =AVRL = V_{SS}.

9. **Notes on Power-on**
   To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50μs from 0.2V to 2.7V.

10. **Stabilization of power supply voltage**
    If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/μs or less in instantaneous fluctuation for power supply switching.

11. **Serial communication**
    There is a possibility to receive wrong data due to noise or other causes on the serial communication.

    Therefore, design a printed circuit board so as to avoid noise.

    Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

12. **Mode Pin (MD)**
    Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to Vcc or Vss pin and provide a low-impedance connection.

14.3 DC Characteristics

14.3.1 Current Rating

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes[*1]	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz Flash 0 wait (CLKRC and CLKSC stopped)	-	27	-	mA	T_A = +25°C
				-	-	37	mA	T_A = +105°C
				-	-	38.5	mA	T_A = +125°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL, CLKSC and CLKRC stopped)	-	3.5	-	mA	T_A = +25°C
				-	-	8	mA	T_A = +105°C
				-	-	9.5	mA	T_A = +125°C
	I_{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	1.8	-	mA	T_A = +25°C
				-	-	6	mA	T_A = +105°C
				-	-	7.5	mA	T_A = +125°C
	I_{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	0.16	-	mA	T_A = +25°C
				-	-	3.5	mA	T_A = +105°C
				-	-	5	mA	T_A = +125°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz Flash 0 wait (CLKMC, CLKPLL and CLKRC stopped)	-	0.1	-	mA	T_A = +25°C
				-	-	3.3	mA	T_A = +105°C
				-	-	4.8	mA	T_A = +125°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes*2	I_{CCTPLL}	Vcc	PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped)	-	1800	2250	μA	T_A = +25°C
				-	-	3220	μA	T_A = +105°C
				-	-	4205	μA	T_A = +125°C
	$I_{CCTMAIN}$		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	330	μA	T_A = +25°C
				-	-	1195	μA	T_A = +105°C
				-	-	2165	μA	T_A = +125°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	215	μA	T_A = +25°C
				-	-	1095	μA	T_A = +105°C
				-	-	2075	μA	T_A = +125°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)	-	35	75	μA	T_A = +25°C
				-	-	905	μA	T_A = +105°C
				-	-	1880	μA	T_A = +125°C
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	65	μA	T_A = +25°C
				-	-	885	μA	T_A = +105°C
				-	-	1850	μA	T_A = +125°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Stop mode*3	I_{CCH}	Vcc	-	-	20	60	μA	T_A = +25°C
				-	-	880	μA	T_A = +105°C
				-	-	1845	μA	T_A = +125°C
Flash Power Down current	$I_{CCFLASHPD}$		-	-	36	70	μA	
Power supply current for active Low Voltage detector*4	I_{CCLVD}		Low voltage detector enabled	-	5	-	μA	T_A = +25°C
				-	-	12.5	μA	T_A = +125°C
Flash Write/ Erase current*5	$I_{CCFLASH}$		-	-	12.5	-	mA	T_A = +25°C
				-	-	20	mA	T_A = +125°C

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

*2: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

*3: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

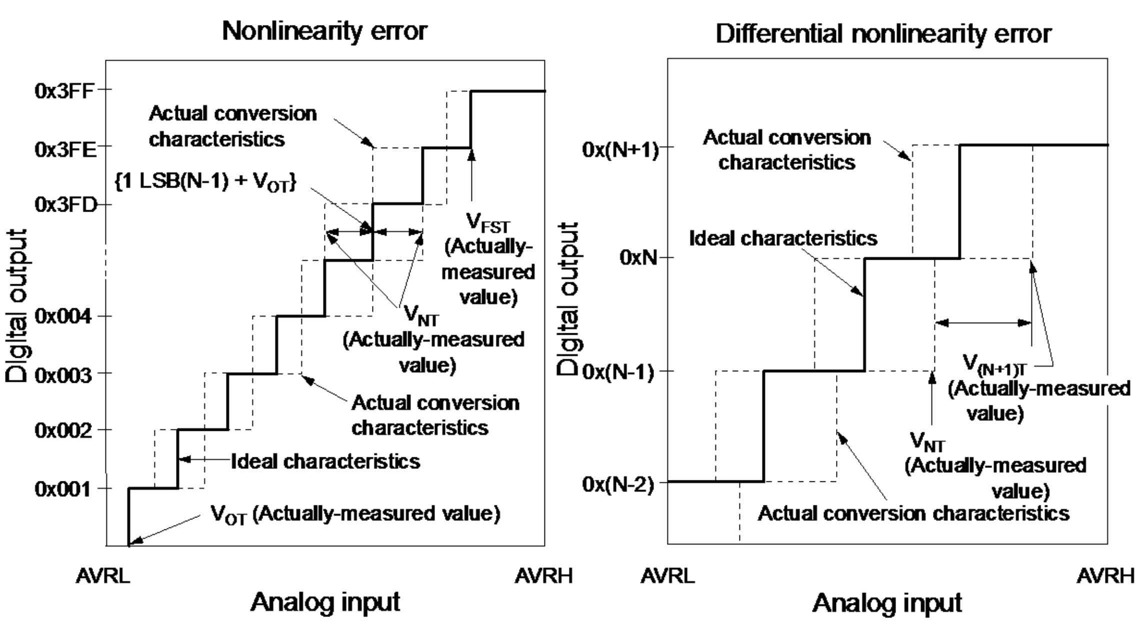
*4: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

*5: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH4}	4mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OH} = -4mA$ $2.7V \le V_{CC} < 4.5V$ $I_{OH} = -1.5mA$	V_{CC} - 0.5	-	V_{CC}	V	
	V_{OH3}	3mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OH} = -3mA$ $2.7V \le V_{CC} < 4.5V$ $I_{OH} = -1.5mA$	V_{CC} - 0.5	-	V_{CC}	V	
"L" level output voltage	V_{OL4}	4mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OL} = +4mA$ $2.7V \le V_{CC} < 4.5V$ $I_{OL} = +1.7mA$	-	-	0.4	V	
	V_{OL3}	3mA type	$2.7V \le V_{CC} < 5.5V$ $I_{OL} = +3mA$	-	-	0.4	V	
	V_{OLD}	DEBUG I/F	$V_{CC} = 2.7V$ $I_{OL} = +25mA$	0	-	0.25	V	
Input leak current	I_{IL}	Pnn_m	$V_{SS} < V_I < V_{CC}$ AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	- 1	-	+ 1	μA	
Pull-up resistance value	R_{PU}	Pnn_m	V_{CC} = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C_{IN}	Other than C, Vcc, Vss, AVcc, AVss, AVRH, AVRL	-	-	5	15	pF	

14.5.3 *Definition of A/D Converter Terms*

Resolution : Analog variation that is recognized by an A/D converter.
Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ←→ 0b0000000001) to the full-scale transition point (0b1111111110 ←→ 0b1111111111).
Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
Zero transition voltage: Input voltage which results in the minimum conversion value.
Full scale transition voltage: Input voltage which results in the maximum conversion value.

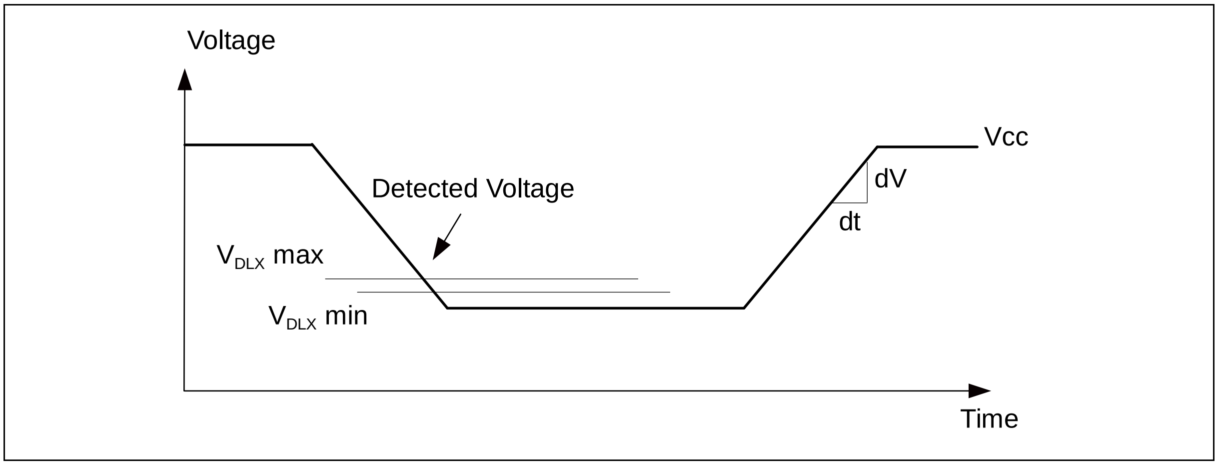


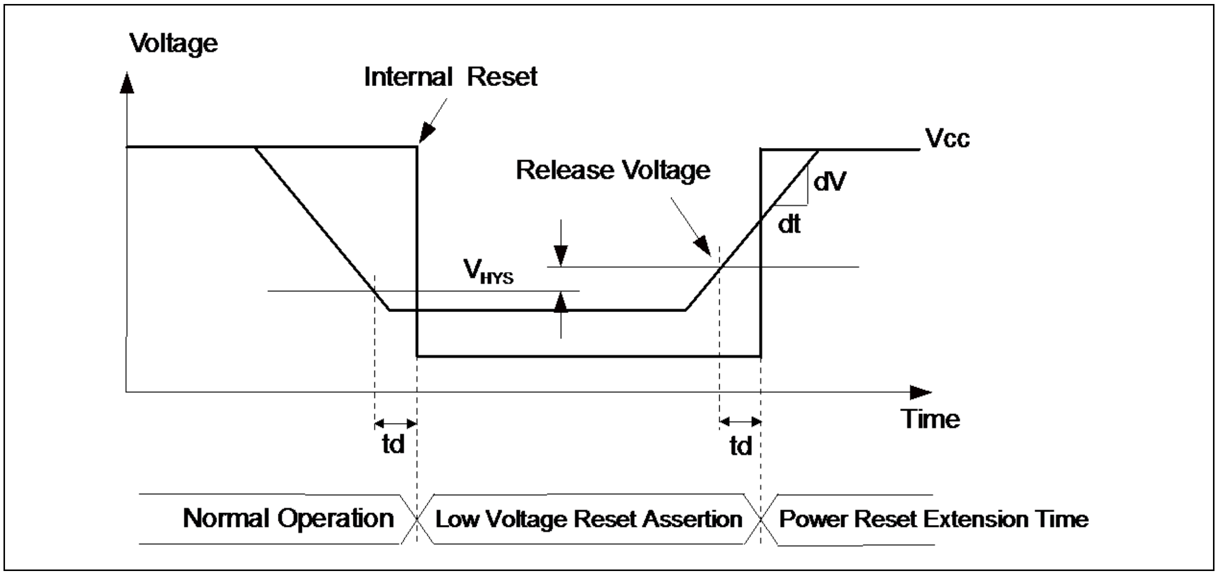
Nonlinearity error of digital output N = $\dfrac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB}$ [LSB]

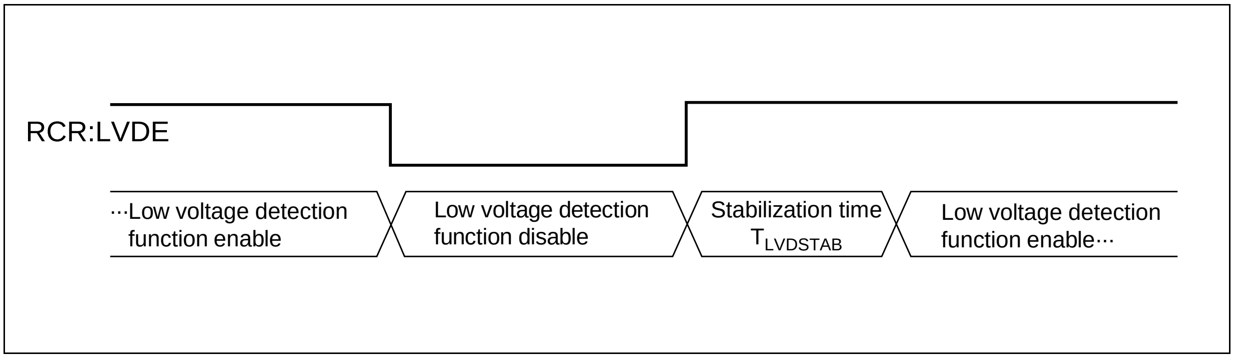
Differential nonlinearity error of digital output N = $\dfrac{V_{(N+1)T} - V_{NT}}{1LSB} - 1$ [LSB]

$1LSB = \dfrac{V_{FST} - V_{OT}}{1022}$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.


Voltage
Vcc
Detected Voltage
dV
dt
V_{DLX} max
V_{DLX} min
Time


Voltage
Internal Reset
Vcc
Release Voltage
dV
dt
V_{HYS}
Time
td
td
Normal Operation
Low Voltage Reset Assertion
Power Reset Extension Time


RCR:LVDE
···Low voltage detection function enable
Low voltage detection function disable
Stabilization time $T_{LVDSTAB}$
Low voltage detection function enable···

14.7 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	$T_A \leq$ + 105°C	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	$T_A \leq$ + 105°C	-	25	400	µs	Not including system-level overhead time.
	Small Sector	-	-	25	400	µs	
Chip erase time		$T_A \leq$ + 105°C	-	11.51	55.05	s	Includes write time prior to internal erase.

Note: While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.
To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})[*1].

Write/Erase cycles and data hold time

Write/Erase cycles (cycle)	Data hold time (year)
1,000	20 [*2]
10,000	10 [*2]
100,000	5 [*2]

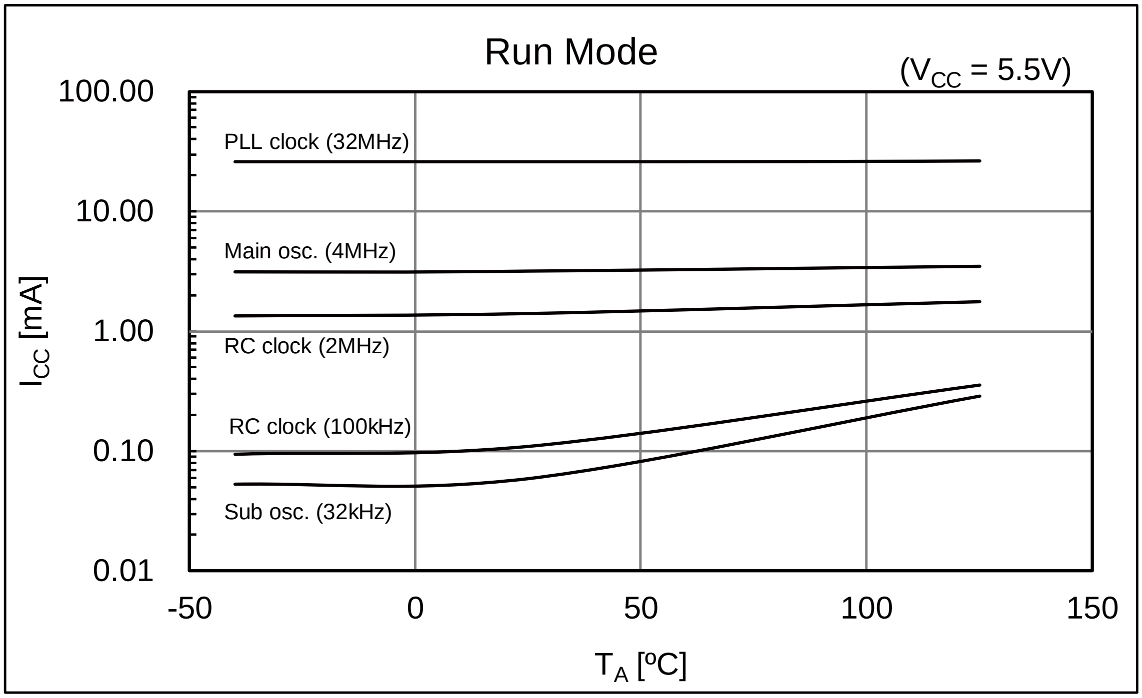
*1: See "6. Low Voltage Detection Function Characteristics".

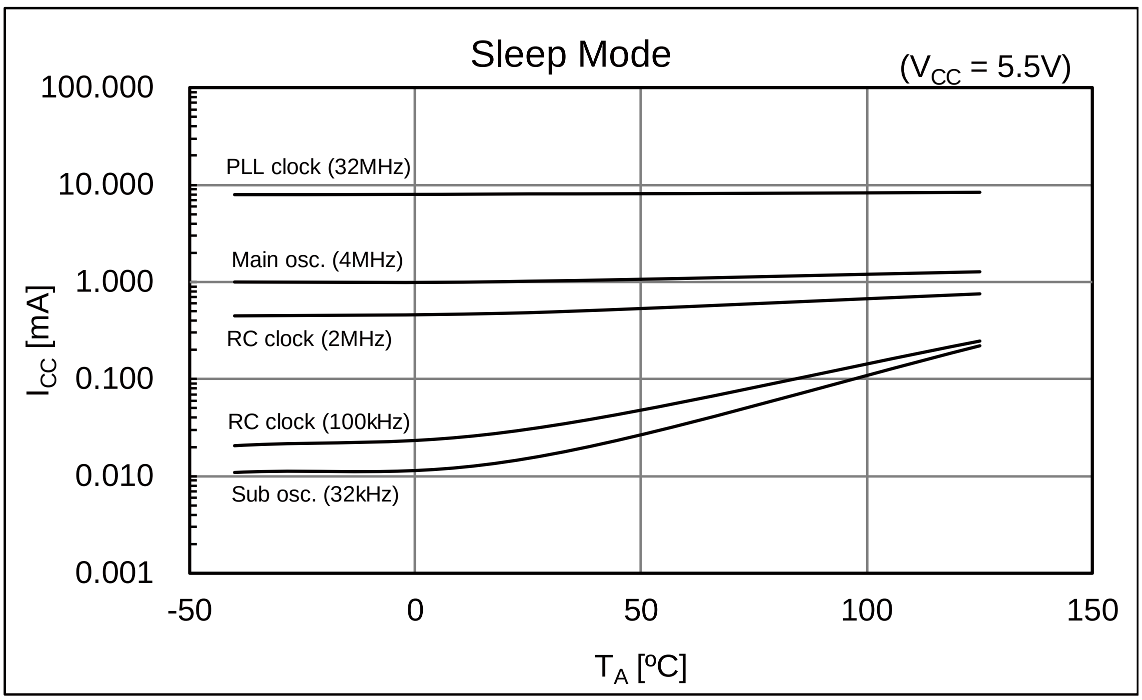
*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

15. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

■MB96F657





16. Ordering Information

MCU with CAN controller

Part number	Flash memory	Package*
MB96F653RBPMC-GSE1	Flash A (96.5KB)	120-pin plastic LQFP (LQM120)
MB96F653RBPMC-GSE2		
MB96F655RBPMC-GSE1	Flash A (160.5KB)	120-pin plastic LQFP (LQM120)
MB96F655RBPMC-GSE2		
MB96F656RBPMC-GSE1	Flash A (288.5KB)	120-pin plastic LQFP (LQM120)
MB96F656RBPMC-GSE2		
MB96F657RBPMC-GSE1	Flash A (416.5KB)	120-pin plastic LQFP (LQM120)
MB96F657RBPMC-GSE2		

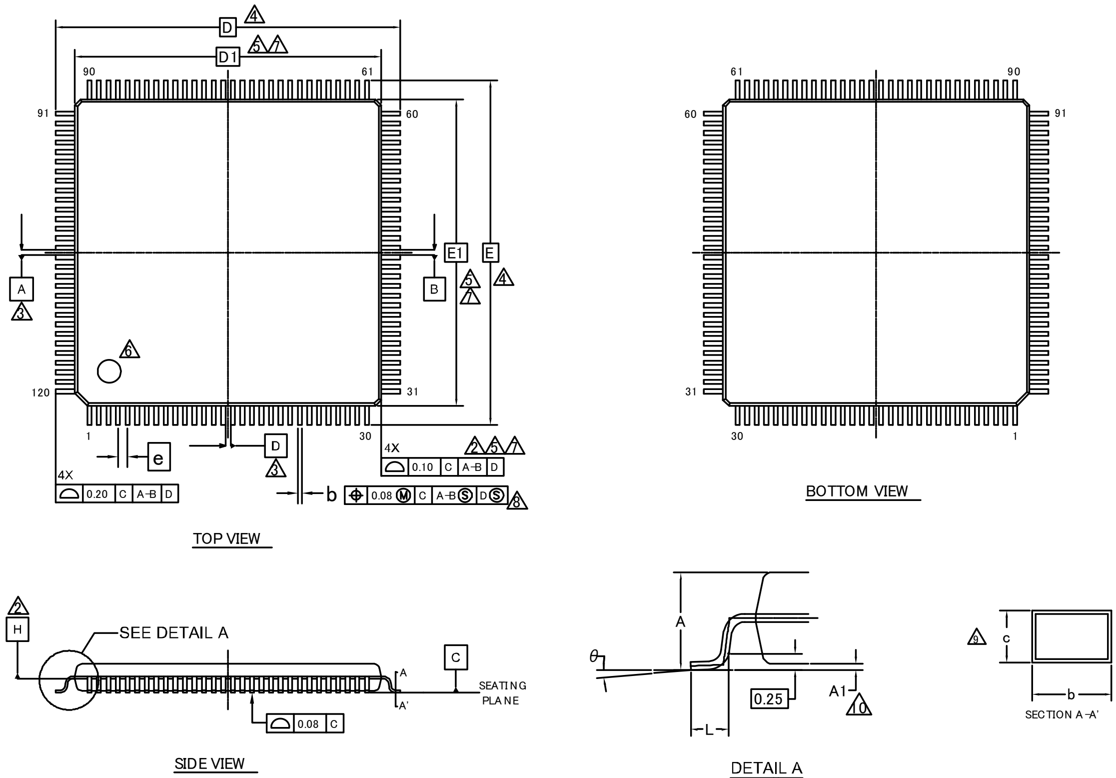
*: For details about package, see "Package Dimension".

MCU without CAN controller

Part number	Flash memory	Package*
MB96F653ABPMC-GSE1	Flash A (96.5KB)	120-pin plastic LQFP (LQM120)
MB96F653ABPMC-GSE2		
MB96F655ABPMC-GSE1	Flash A (160.5KB)	120-pin plastic LQFP (LQM120)
MB96F655ABPMC-GSE2		

*: For details about package, see "Package Dimension".

17. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D	18.00 BSC		
D1	16.00 BSC		
e	0.50 BSC		
E	18.00 BSC		
E1	16.00 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

002-16172 **

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	KSUN	01/31/2014	Migrated to Cypress and assigned document number 002-04707. No change to document contents or format.
*A	5164895	KSUN	03/14/2016	Updated to Cypress template
*B	6005555	KSUN	01/09/2018	Updated the Cypress logo, Sales information and legal. Refer to 18. Major Changes.