Infineon Technologies - MB96F657RBPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

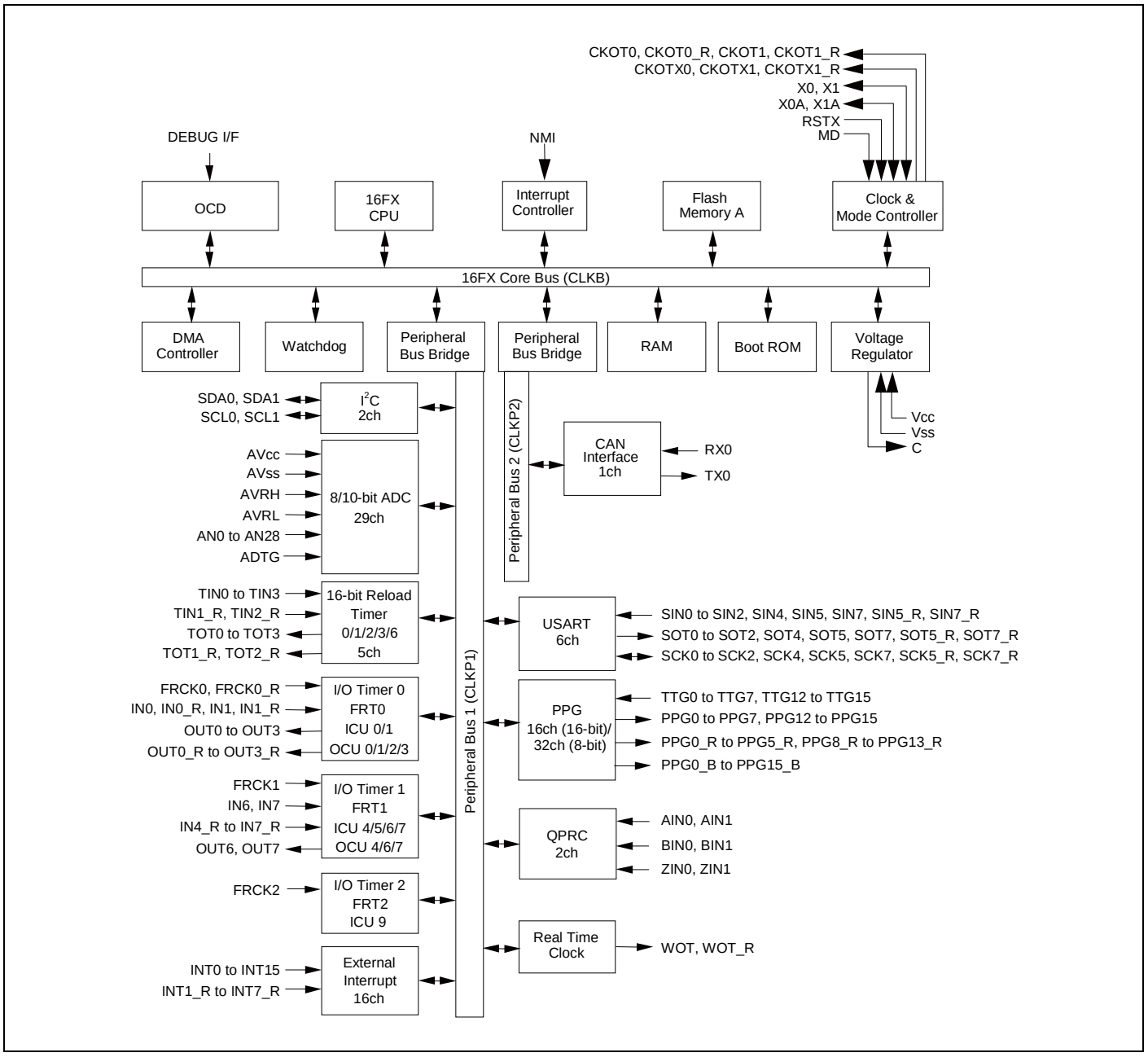
Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	101
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	28K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 29x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f657rbpmc-gse2

1. Product Lineup

Features			MB96650	Remark
Product Type			Flash Memory Product	
Subclock			Subclock can be set by software	
Dual Operation Flash Memory		RAM	-	
64.5KB + 32KB		10KB	MB96F653R, MB96F653A	Product Options R: MCU with CAN A: MCU without CAN
128.5KB + 32KB		16KB	MB96F655R, MB96F655A	
256.5KB + 32KB		24KB	MB96F656R	
384.5KB + 32KB		28KB	MB96F657R	
Package			LQFP-120: LQM120	
DMA			4ch	
USART			6ch	LIN-USART 0 to 2/4/5/7
	with automatic LIN-Header transmission/reception		Yes (only 1ch)	LIN-USART 0
	with 16 byte RX- and TX-FIFO		No	
I^2C			2ch	I^2C 0/1
8/10-bit A/D Converter			29ch	AN 0 to 28
	with Data Buffer		No	
	with Range Comparator		Yes	
	with Scan Disable		Yes	
	with ADC Pulse Detection		No	
16-bit Reload Timer (RLT)			5ch	RLT 0 to 3/6
16-bit Free-Running Timer (FRT)			3ch	FRT 0 to 2
16-bit Input Capture Unit (ICU)			7ch (1 channel for LIN-USART)	ICU 0/1/4 to 7/9 ICU 9 for LIN-USART
16-bit Output Compare Unit (OCU)			7ch	OCU 0 to 4/6/7 (OCU 4 for FRT clear)
8/16-bit Programmable Pulse Generator (PPG)			16ch (16-bit) / 32ch (8-bit)	PPG 0 to 15
	with Timing point capture		Yes	
	with Start delay		Yes	
	with Ramp		No	
Quadrature Position/Revolution Counter (QPRC)			2ch	QPRC 0/1
CAN Interface			1ch	CAN 0 32 Message Buffers
External Interrupts (INT)			16ch	INT 0 to 15
Non-Maskable Interrupt (NMI)			1ch	
Real Time Clock (RTC)			1ch	
I/O Ports			99 (Dual clock mode) 101 (Single clock mode)	
Clock Calibration Unit (CAL)			1ch	
Clock Output Function			2ch	
Low Voltage Detection Function			Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer			Yes	
On-chip RC-oscillator			Yes	
On-chip Debugger			Yes	

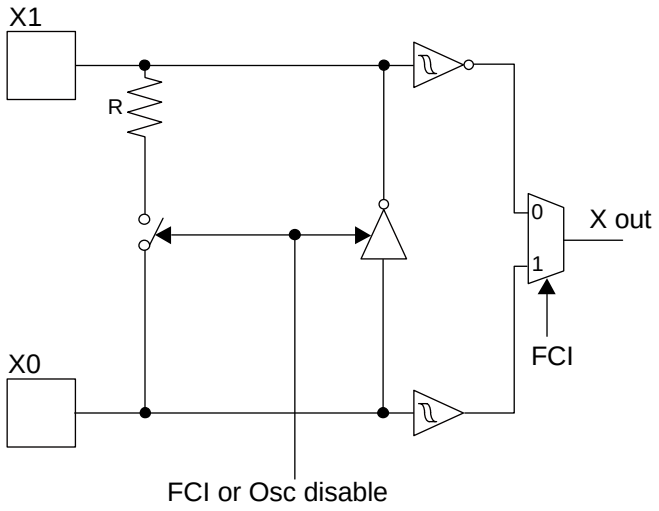
Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.
It is necessary to use the port relocate function of the general I/O port according to your function use.

2. Block Diagram

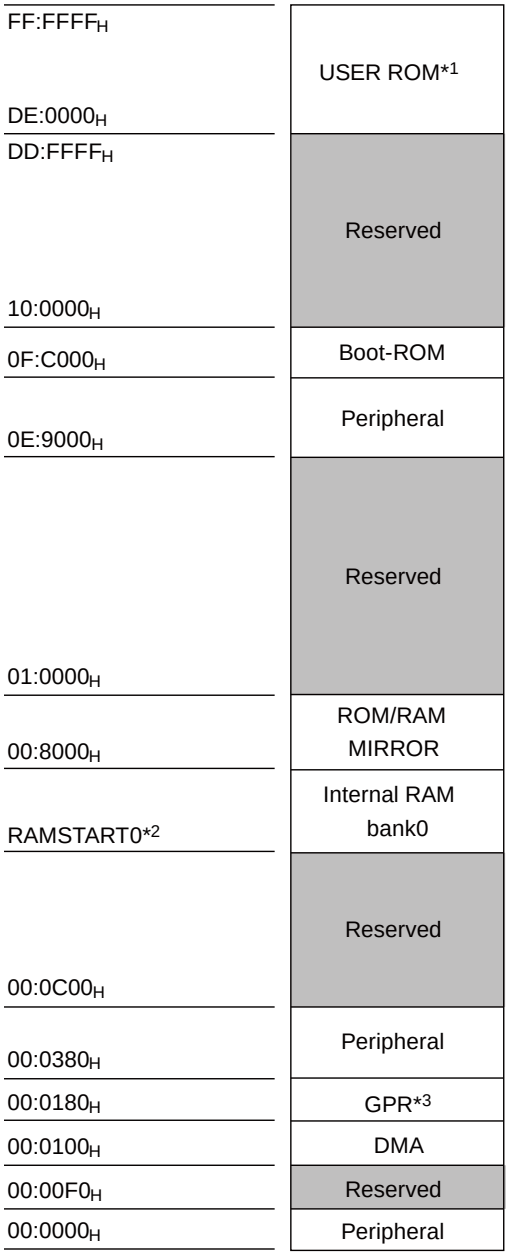


Pin no.	I/O circuit type*	Pin name
37	K	P08_1 / AN17
38	K	P08_2 / AN18
39	K	P08_3 / AN19
40	K	P08_4 / AN20 / OUT6
41	N	P04_6 / SDA1
42	N	P04_7 / SCL1
43	K	P08_5 / AN21 / OUT7
44	K	P08_6 / AN22 / PPG6_B
45	K	P08_7 / AN23 / PPG7_B
46	K	P09_0 / AN24 / PPG8_R
47	K	P09_1 / AN25 / PPG9_R
48	K	P09_2 / AN26 / PPG10_R
49	K	P09_3 / AN27 / PPG11_R
50	H	P09_4 / PPG12
51	H	P09_5 / PPG13
52	H	P09_6 / PPG14
53	H	P17_1 / PPG12_R
54	H	P17_2 / PPG13_R
55	H	P09_7 / PPG15
56	I	P10_0 / SIN2 / TIN3 / AN28 / INT11
57	H	P10_1 / SOT2 / TOT3
58	M	P10_2 / SCK2 / PPG6
59	H	P10_3 / PPG7
60	Supply	Vcc
61	Supply	Vss
62	O	DEBUG I/F
63	H	P17_0
64	C	MD
65	A	X0
66	A	X1
67	Supply	Vss
68	B	P04_0 / X0A
69	B	P04_1 / X1A
70	C	RSTX
71	H	P11_0
72	H	P11_1 / PPG0_R
73	H	P11_2 / PPG1_R
74	H	P11_3 / PPG2_R
75	H	P11_4 / PPG3_R

6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Feedback resistor = approx. 1.0MΩ ■ The amplitude: 1.8V±0.15V to operate by the internal supply voltage

7. Memory Map



*1: For details about USER ROM area, see "USER ROM MEMORY MAP FOR FLASH DEVICES" on the following pages.

*2: For RAMSTART addresses, see the table on the next page.

*3: Unused GPR banks can be used as RAM area.
GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

8. Ramstart Addresses

Devices	Bank 0 RAM size	RAMSTART0
MB96F653	10KB	$00:5A00_H$
MB96F655	16KB	$00:4200_H$
MB96F656	24KB	$00:2200_H$
MB96F657	28KB	$00:1200_H$

9. User ROM Memory Map for Flash Devices

CPU mode address	Flash memory mode address	MB96F653 Flash size 64.5KB + 32KB	MB96F655 Flash size 128.5KB + 32KB	MB96F656 Flash size 256.5KB + 32KB	MB96F657 Flash size 384.5KB + 32KB	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	Reserved	SA38 - 64KB	SA38 - 64KB	SA38 - 64KB	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$		Reserved	SA37 - 64KB	SA37 - 64KB	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$			SA36 - 64KB	SA36 - 64KB	
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$			Reserved	SA35 - 64KB	
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$				SA34 - 64KB	
F9:FFFF$_H$ DF:A000$_H$					Reserved	
DF:9FFF$_H$ DF:8000$_H$	1F:9FFF$_H$ 1F:8000$_H$	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	Bank B of Flash A
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SAS - 512B*	SAS - 512B*	SAS - 512B*	SAS - 512B*	Bank A of Flash A
DE:FFFF$_H$ DE:0000$_H$		Reserved	Reserved	Reserved	Reserved	

*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for E^{2}PROM emulation.

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
40	$35C_H$	PPG2	Yes	40	Programmable Pulse Generator 2
41	358_H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354_H	PPG4	Yes	42	Programmable Pulse Generator 4
43	350_H	PPG5	Yes	43	Programmable Pulse Generator 5
44	$34C_H$	PPG6	Yes	44	Programmable Pulse Generator 6
45	348_H	PPG7	Yes	45	Programmable Pulse Generator 7
46	344_H	PPG8	Yes	46	Programmable Pulse Generator 8
47	340_H	PPG9	Yes	47	Programmable Pulse Generator 9
48	$33C_H$	PPG10	Yes	48	Programmable Pulse Generator 10
49	338_H	PPG11	Yes	49	Programmable Pulse Generator 11
50	334_H	PPG12	Yes	50	Programmable Pulse Generator 12
51	330_H	PPG13	Yes	51	Programmable Pulse Generator 13
52	$32C_H$	PPG14	Yes	52	Programmable Pulse Generator 14
53	328_H	PPG15	Yes	53	Programmable Pulse Generator 15
54	324_H	-	-	54	Reserved
55	320_H	-	-	55	Reserved
56	$31C_H$	-	-	56	Reserved
57	318_H	-	-	57	Reserved
58	314_H	RLT0	Yes	58	Reload Timer 0
59	310_H	RLT1	Yes	59	Reload Timer 1
60	$30C_H$	RLT2	Yes	60	Reload Timer 2
61	308_H	RLT3	Yes	61	Reload Timer 3
62	304_H	-	-	62	Reserved
63	300_H	-	-	63	Reserved
64	$2FC_H$	RLT6	Yes	64	Reload Timer 6
65	$2F8_H$	ICU0	Yes	65	Input Capture Unit 0
66	$2F4_H$	ICU1	Yes	66	Input Capture Unit 1
67	$2F0_H$	-	-	67	Reserved
68	$2EC_H$	-	-	68	Reserved
69	$2E8_H$	ICU4	Yes	69	Input Capture Unit 4
70	$2E4_H$	ICU5	Yes	70	Input Capture Unit 5
71	$2E0_H$	ICU6	Yes	71	Input Capture Unit 6
72	$2DC_H$	ICU7	Yes	72	Input Capture Unit 7
73	$2D8_H$	-	-	73	Reserved
74	$2D4_H$	ICU9	Yes	74	Input Capture Unit 9
75	$2D0_H$	-	-	75	Reserved
76	$2CC_H$	-	-	76	Reserved
77	$2C8_H$	OCU0	Yes	77	Output Compare Unit 0
78	$2C4_H$	OCU1	Yes	78	Output Compare Unit 1
79	$2C0_H$	OCU2	Yes	79	Output Compare Unit 2
80	$2BC_H$	OCU3	Yes	80	Output Compare Unit 3

■Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

12.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

■Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.

When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

Condition: 125°C/24 h

6. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

7. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed AV_{CC} . Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

8. Pin handling when not using the A/D converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH =AVRL = V_{SS}.

9. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

10. Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

11. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

12. Mode Pin (MD)

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to Vcc or Vss pin and provide a low-impedance connection.

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Stop mode*3	I_{CCH}	Vcc	-	-	20	60	µA	T_A = +25°C
				-	-	880	µA	T_A = +105°C
				-	-	1845	µA	T_A = +125°C
Flash Power Down current	$I_{CCFLASHPD}$		-	-	36	70	µA	
Power supply current for active Low Voltage detector*4	I_{CCLVD}		Low voltage detector enabled	-	5	-	µA	T_A = +25°C
				-	-	12.5	µA	T_A = +125°C
Flash Write/ Erase current*5	$I_{CCFLASH}$		-	-	12.5	-	mA	T_A = +25°C
				-	-	20	mA	T_A = +125°C

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

*2: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

*3: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

*4: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

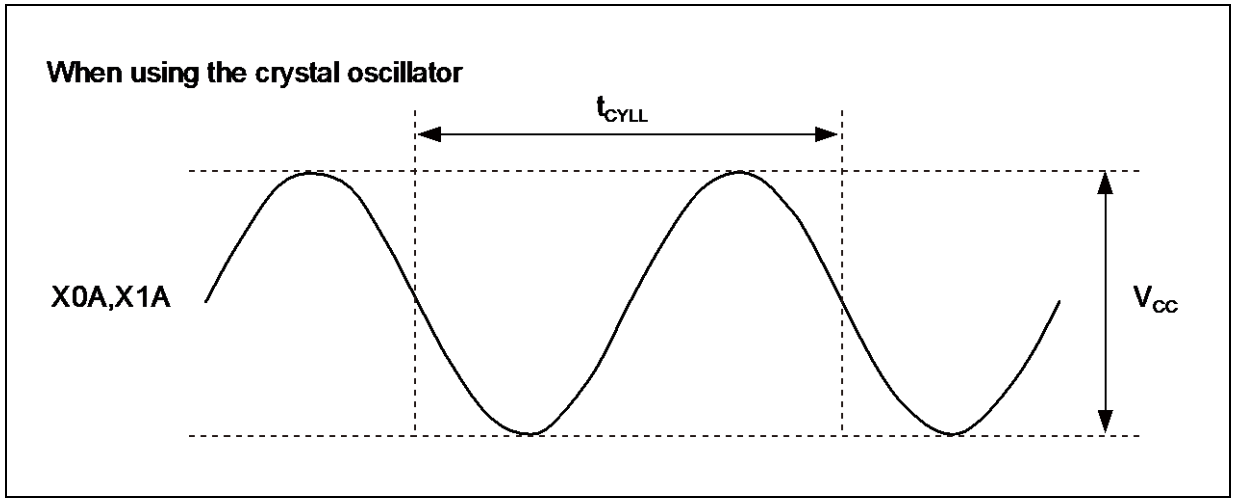
*5: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

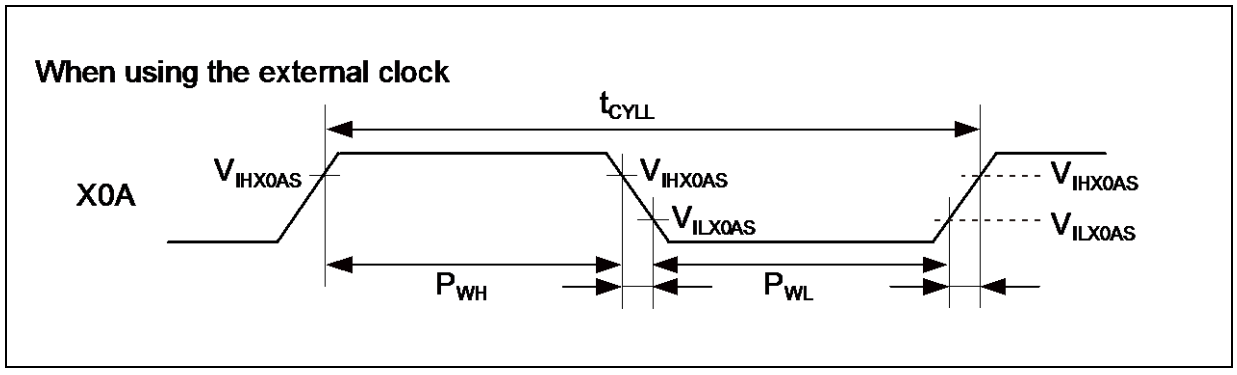
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH4}	4mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OH} = -4mA$ $2.7V \le V_{CC} < 4.5V$ $I_{OH} = -1.5mA$	V_{CC} - 0.5	-	V_{CC}	V	
	V_{OH3}	3mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OH} = -3mA$ $2.7V \le V_{CC} < 4.5V$ $I_{OH} = -1.5mA$	V_{CC} - 0.5	-	V_{CC}	V	
"L" level output voltage	V_{OL4}	4mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OL} = +4mA$ $2.7V \le V_{CC} < 4.5V$ $I_{OL} = +1.7mA$	-	-	0.4	V	
	V_{OL3}	3mA type	$2.7V \le V_{CC} < 5.5V$ $I_{OL} = +3mA$	-	-	0.4	V	
	V_{OLD}	DEBUG I/F	$V_{CC} = 2.7V$ $I_{OL} = +25mA$	0	-	0.25	V	
Input leak current	I_{IL}	Pnn_m	$V_{SS} < V_I < V_{CC}$ AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	- 1	-	+ 1	µA	
Pull-up resistance value	R_{PU}	Pnn_m	$V_{CC} = 5.0V \pm 10\%$	25	50	100	kΩ	
Input capacitance	C_{IN}	Other than C, Vcc, Vss, AVcc, AVss, AVRH, AVRL	-	-	5	15	pF	

14.4.2 Sub Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	





14.4.3 Built-in RC Oscillation Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	µs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	µs	When using fast frequency of RC oscillator (256 RC clock cycles)

14.4.4 Internal Clock Timing

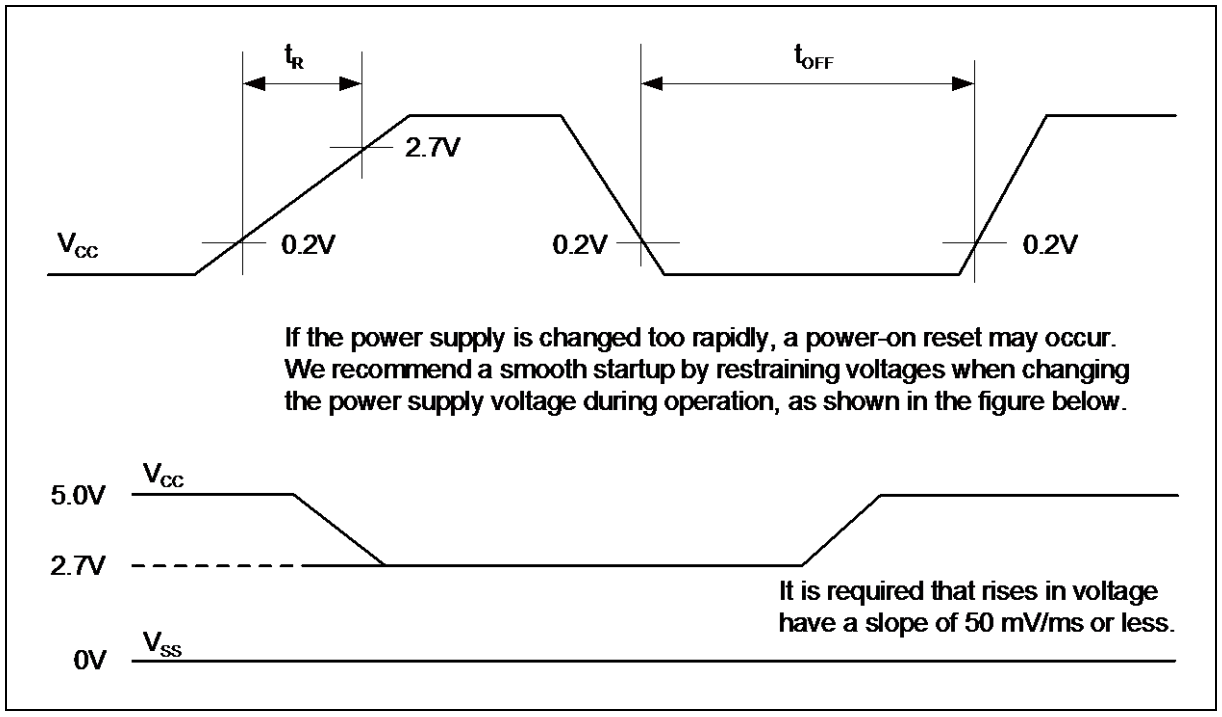
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

14.4.7 Power-on Reset Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	Vcc	0.05	-	30	ms
Power off time	t_{OFF}	Vcc	1	-	-	ms



14.5.3 Definition of A/D Converter Terms

Resolution : Analog variation that is recognized by an A/D converter.

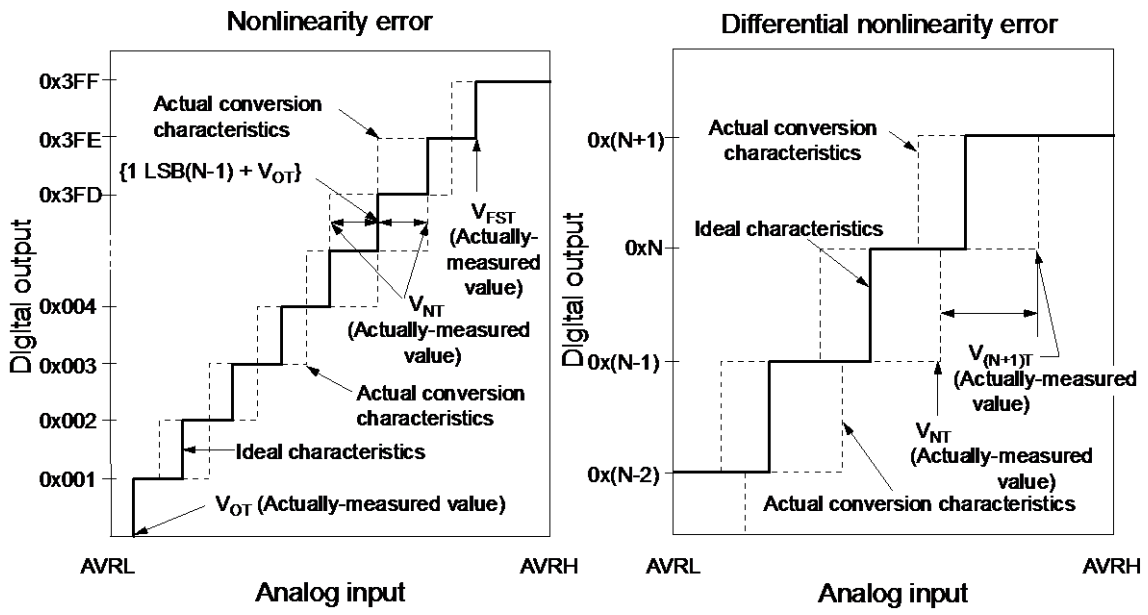
Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).

Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.

Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

Zero transition voltage: Input voltage which results in the minimum conversion value.

Full scale transition voltage: Input voltage which results in the maximum conversion value.



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.

V_{OT} : Voltage at which the digital output changes from 0x000 to 0x001.

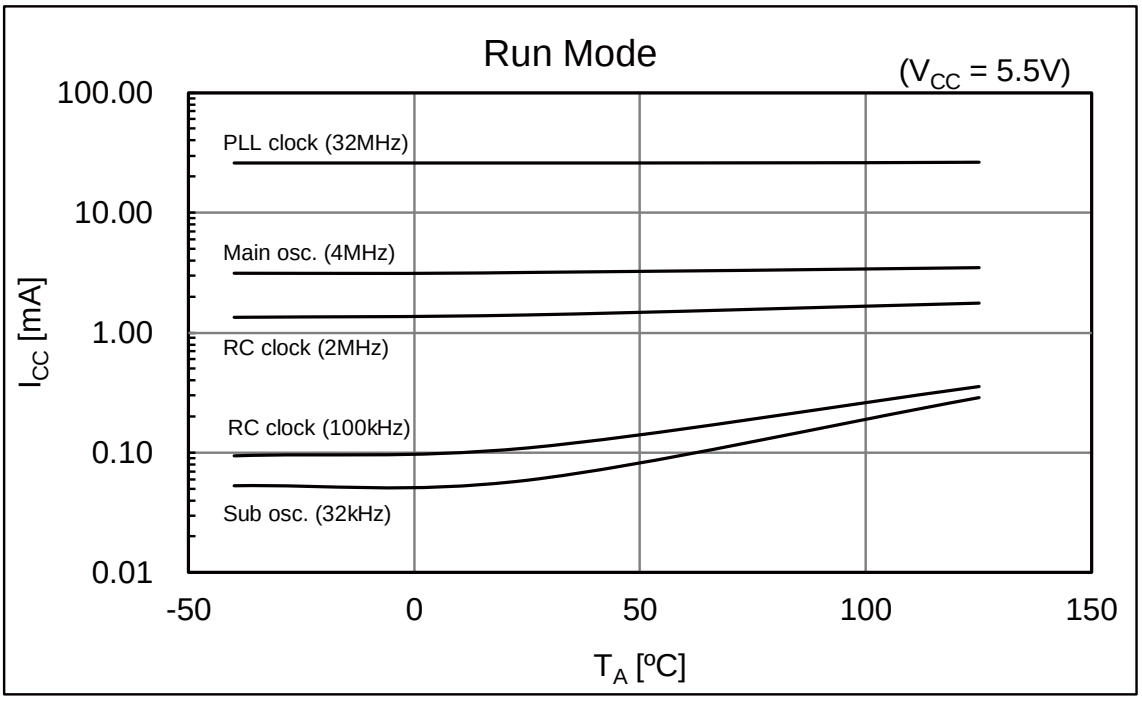
V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.

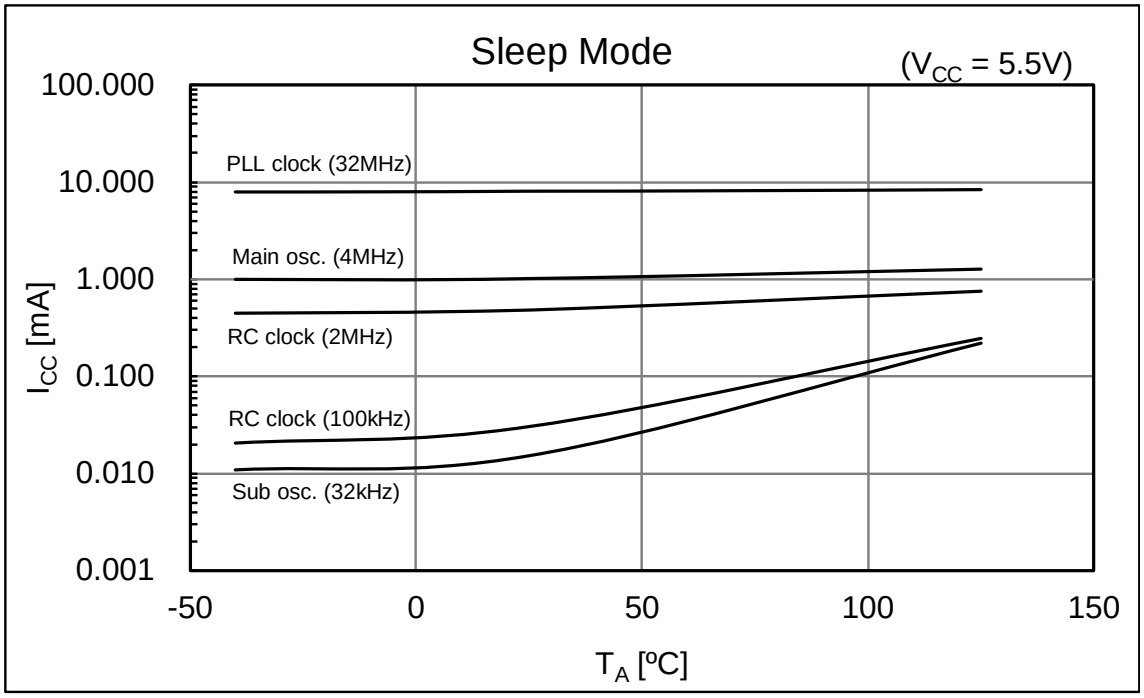
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

15. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

■MB96F657

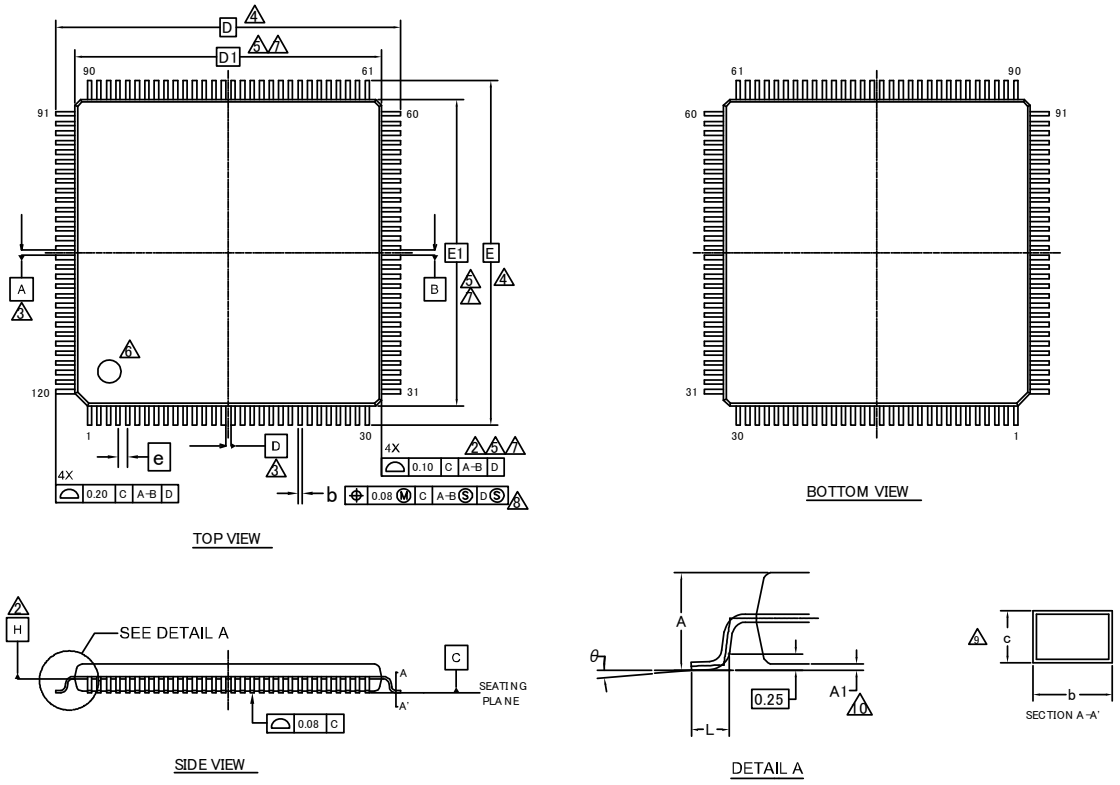




■Used setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

17. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D		18.00 BSC	
D1		16.00 BSC	
e		0.50 BSC	
E		18.00 BSC	
E1		16.00 BSC	
L	0.45	0.60	0.75
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

002-16172 **

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**

Document History

Document Title: MB96650 Series, F2MC-16FX 16-bit Microcontroller
Document Number: 002-04707

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	KSUN	01/31/2014	Migrated to Cypress and assigned document number 002-04707. No change to document contents or format.
*A	5164895	KSUN	03/14/2016	Updated to Cypress template
*B	6005555	KSUN	01/09/2018	Updated the Cypress logo, Sales information and legal. Refer to 18. Major Changes.